Designing Microwave PCBs for Successful Manufacture — Getting it Right the First Time

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Teledyne Labtech

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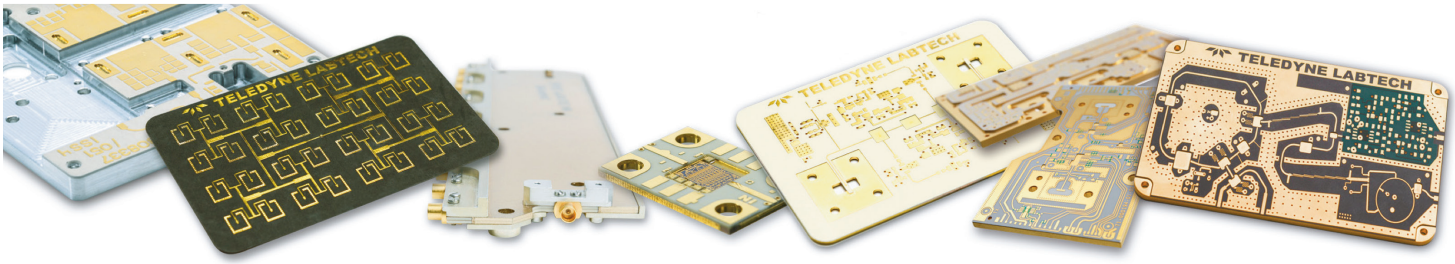

Designing Microwave PCBs for Successful Manufacture – Getting it Right the First Time

Introduction

With improvements in processor speed and model accuracy, it is more and more common for microwave circuit simulations to bear close approximation to their eventual real world performance. However, not all pitfalls present in the successful manufacture of a complex microwave circuit are captured in simulations. This paper looks at some common mistakes we see every day, and how to adjust your design to avoid them, as well as covering some other useful points.

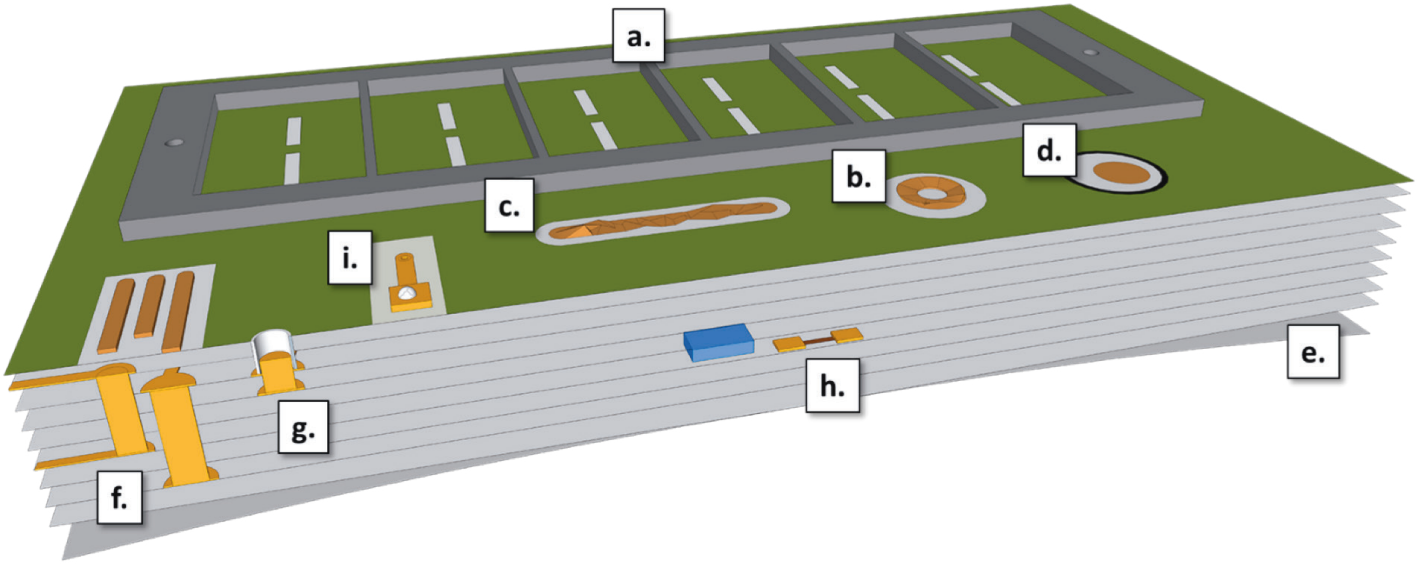

Figure 1: Some common issues on a stylized microwave PCB that we'll look at in more detail in following sections

In stylized and exaggerated form, Figure 1 shows some common issues we'll cover in the following sections. These include:

a. Misalignment through choice of material with insufficient dimensional stability for the application
b. Pad lift
c. Peeling traces
d. Thermoplastic movement of features
e. Extreme bowing because of coefficient of thermal expansion mismatch between materials
f. Impossible to produce blind vias
g. Accidental stub antennas
h. Printed embedded resistors with too little area to maintain value accuracy
i. Poor solder joint due to gold embrittlement

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As a reminder, modern microwave printed circuit boards (PCBs) are made from layers of material pressed and bonded together. Typical layers ('base laminates') start off completely covered top and bottom with copper ('copper foils'), the majority of which are selectively removed during processing steps, leaving only the desired traces, ground planes etc. Plated-through holes (PTH) are constructed to connect traces on different layers together, and commonly components such as resistors can be embedded inside the layer stack, or created from the selective laying down of resistive material. Typically top and bottom layers will have the majority of the desired electrical components mounted on them, with connections made between component and trace achieved with soldering or wire bonding. The composition of the underlying layers greatly affects the microwave performance, as well as the physical behavior in the expected environment.

With this in mind we will walk through the different stages, as shown in Figure 2:

1. Base laminate material, which greatly affects performance at frequency through factors such as dielectric coefficient (Dk) and loss tangent (Df)
2. Choice of copper foils supplied with the base laminate
3. Bond films that glue the stack together
4. Buildup of the multi-layer stack
5. Via types and spans
6. Embedded resistors
7. Surface finish

This paper considers the primary factors considered for Design for Manufacture (DFM) for RF/ Microwave PCBs and does not attempt to be an exhaustive guide for all RF PCBs.

One question frequently asked is what the primary cost drivers are, and what can be done to reduce the cost. This is never a straightforward question because invariably there are good reasons for the multiple via stacks or tight tolerances specified, but we will look at some trade-offs.

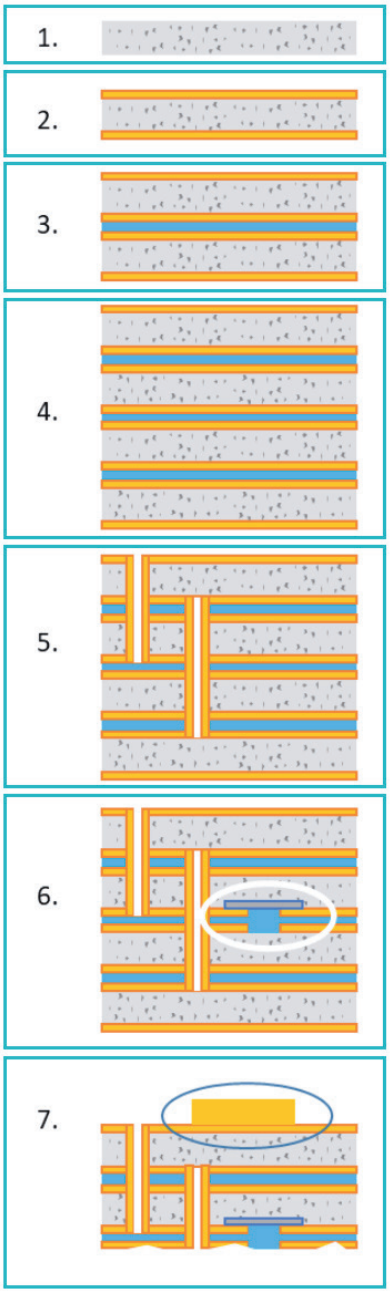

Figure 2: Order of discussion

1) Base Laminates

Choice of base laminate materials is one of the earliest design decisions, affecting performance and cost. A table of common materials we work with is given in Appendix 1, with salient performance characteristics listed.

There are many different materials available; from the RF / microwave designer's point of view Dk and Df will be paramount. The type of copper foil will also factor into the losses within the circuit with low profile coppers often being selected where losses need to be minimized. Below is a list of considerations from a manufacturing point of view:

a) Dimensional stability
b) Metal backed (pre-bonded) – type of backing: copper, brass or aluminium
c) Coefficient of Thermal Expansion (CTE) is especially important for multilayer circuits
d) Glass Transition Temperature (Tg) or melt point for thermoplastics
e) Type and percentage of filler within substrate

Dimensional stability can be a major issue, especially for larger circuits, and although dimensional changes during processing (usually shrinkage) can be allowed for by scaling, consistency is key to successful production with high yields. Generally materials with some type of reinforcement (e.g. woven glass) give more consistent results (see Comments column in Appendix 1). So where can this bite you? For a material with poor and unpredictable dimensional stability, scaling does not solve the issue as the dimensional change varies from piece to piece. It is common for us to make very large phased array antennas, with sizes up to 1.2m by 1.2m, where alignment relies upon accurate distances from physical mounting holes. If you imagine radiating elements on the board matching up to precise apertures in a machined metal piece as shown in Figure 3, as the placement of the elements wanders off relative to the metal (from correct placement at '(i)', to significantly offset in '(ii)'), loss and efficiency of the antennas will suffer.

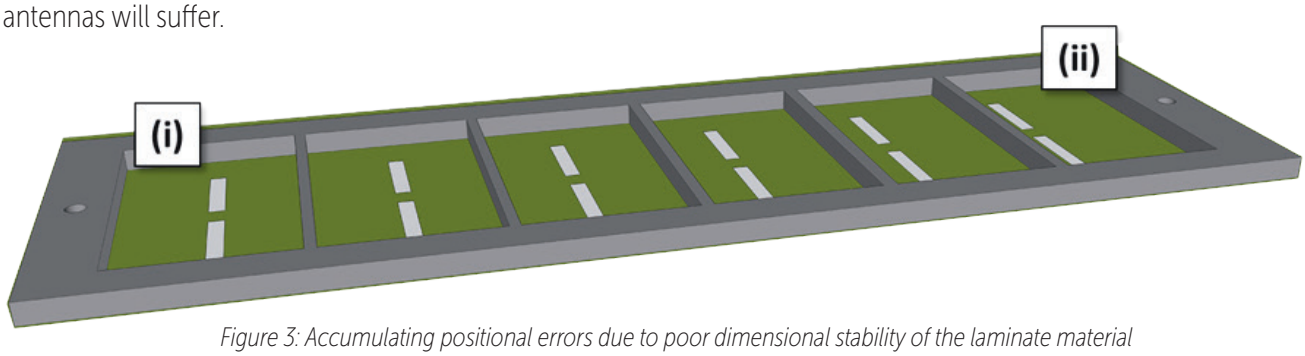

Figure 3: Accumulating positional errors due to poor dimensional stability of the laminate material

A different but common issue is designers using dimensionally stable materials, but specifying extremely tight tolerances in the belief that this will insulate them from issues resulting from process tolerances. While this may be necessary in some designs, it pushes up cost and increases scrap. Often, using expanding tolerances in modeling tools shows that some aspects of the design are less sensitive than might be assumed, and relaxation will greatly aid manufacturability.

Metal backed circuits can present challenges in terms of overall thickness for processing. The applications are usually for high power RF so backings of >6mm are commonplace. The maximum total thickness for our standard processes is 8mm and we can plate aluminium for through holes, blind vias and final finishing of exposed aluminium.

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The CTE of a material is an important consideration for both the end use and throughout manufacture of the PCBs. Mismatches can lead to stresses within the structure that can result in bowing; they can also lead to stresses in solder joints where the CTE of components is significantly different to the overall CTE of the PCB, sowing the seeds for poor reliability for later. It is safest to use the same materials throughout the stack whenever possible. Frequently designs will combine microwave circuits with digital logic control circuits, using lower cost FR4 for the latter to save cost; this sets up likely CTE issues unless designs are symmetrical, with distribution of CTEs balanced across the board.

Another consideration is the Tg. For FR4 this is typically between 120 and 140°C. For high quality microwave materials Tg is typically >170°C, and most high reliability applications call for high Tg materials. It is an important consideration as CTE generally makes a step change when the Tg is exceeded, sometimes changing by a factor of 3 or 4. Given that lead-free soldering calls for temperatures of the order of 230°C, increased CTE above Tg can mean increased stresses on features such as PTH vias, pads etc., particularly in the z-direction, leading to pad-lift after cooling. Conceptually this is shown in Figure 4 (i) from our conceptual sketch of Figure 1. (ii) and magnified in (iii) show a cross sectional photo of a real example of pad-lift.

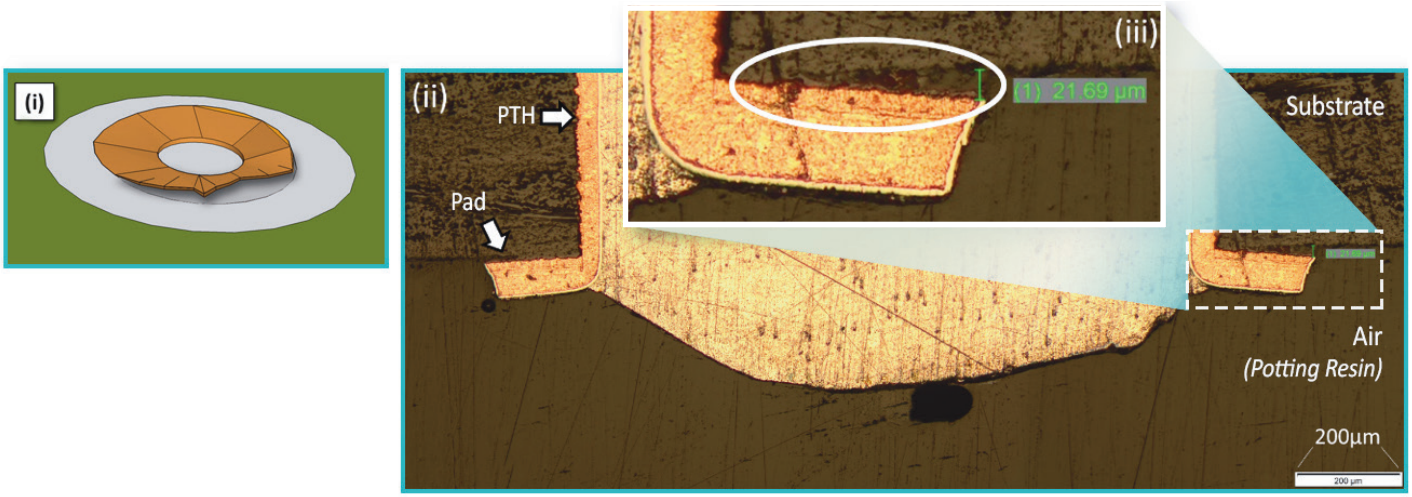

Figure 4: Example of pad lift that can occur after thermal stress (288°C solder float for 10 seconds). Note in (ii) the via hole is filled with solder as a result of the solder float test. Pad lift/ land lift (magnified in (iii)) occurs due the Z axis CTE of the substrate being much higher than the copper of the hole wall and the PCB is taken through an elevated temperature cycle, especially if the Tg of the substrate is exceeded.

Materials with higher Dks usually have high filler contents that can be very abrasive to drills and cutters. While in itself this is not an issue, processing costs will be increased because of use of a greater number of drills and cutters for each circuit.

2) Copper Foils

Laminate layers are available with a variety of copper foils. The most common is Electro Deposited. The type of copper foil used will have an impact on the RF performance especially at higher frequencies. Typically the types of copper foil available and associated backside surface roughness are:

- Electro Deposited (ED) – 1.5µm RMS but can be as high as 3.0µm RMS
- Reverse Treated (RT) – 0.7µm RMS
- Rolled Annealed (RA) – 0.3µm RMS

How does this impact? As examples:

- For 0.020" RO3003 with 0.5oz RA copper versus the same substrate with 0.5oz ED copper at 25GHz the loss is about 0.1dB/in greater for ED compared with RA copper.
- For 0.005" RO3003 with 0.5oz RA copper versus the same substrate with 0.5oz ED copper at 25GHz the loss is about 0.35dB/in greater for ED compared with RA copper.

Clearly increased surface roughness will lead to increased transmission losses (dB/mm). The losses will increase with higher frequencies and increase with a reduction in substrate thickness. These become particularly important for long trace runs on large substrates. However, this is a trade-off on two fronts:

1. Smoother surfaces take more steps to process, as it is harder to bond subsequent layers, increasing cost.
2. Similarly, the peel strength of the copper will be lower, making scrap more likely and rework harder or impossible; indeed, some materials like Rogers 4000 are not available with RA copper.

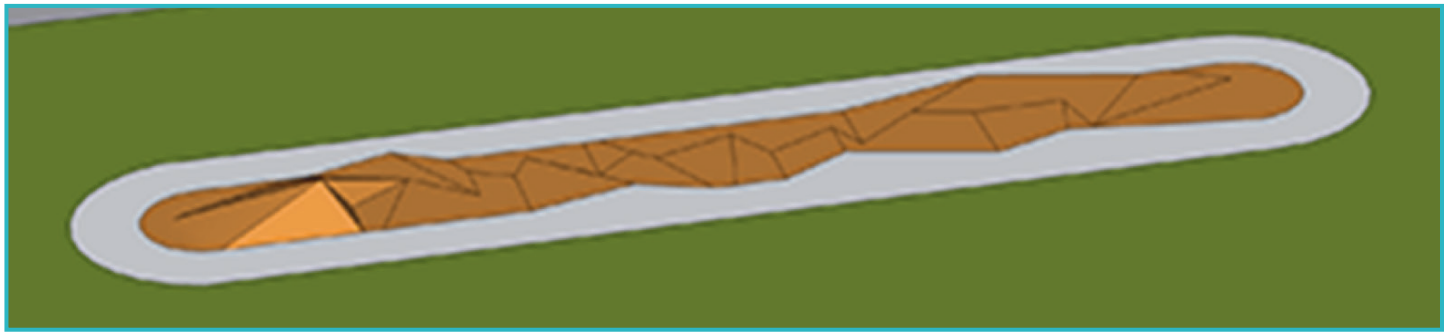

Figure 5: Peeling of traces is more likely after rework if the back side of the copper was smoother initially – the trade-off between lower loss, and lower adhesion

3) Bond Films

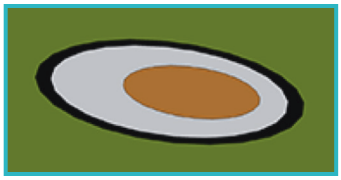

Figure 6: Illustration of PTH via having moved relative to top level artwork due to flow of thermoplastic material in later stage at too high temperature

With so many different prepreg's[1] and bond films available there is a lot to consider. For manufacture we need to consider the following criteria to assist selecting different categories of bond films as well as ensuring the electrical properties are appropriate:

a) Thermoset or thermoplastic?

b) Bonding temperature. Will all the materials within the build withstand the bonding temperature? E.g. base laminates, plugging paste, embedded components, solder, silver epoxy etc.

c) Will the bond film withstand any subsequent assembly stages? SMT assembly or hand assembly?

d) Are there multiple bond stages? If there are, thermoset bond films/ prepregs tend to make life easier but it is not always essential. Thermoplastics can still be an option if bond films are used with different melt points and the bond film with the lowest melt point used last.

e) Are there filled vias? Within a sequential build there is often the requirement to fill buried via holes. Depending on the number and size of vias and the prepreg used, one option is to fill these with resin flow from the prepreg during bonding. However if the volume to be filled is too great then holes must be filled using a high solids content plug paste.

f) If there are internal cut outs where resin flow needs to be controlled, no or low flow prepregs must be used.

Thermoset materials don't re-melt, whereas thermoplastics will soften; thus circuits composed with thermoplastic materials will tend to move or come apart if you go above a set temperature. This can be ok if you sequential bond, but it is important to start off with the highest temperature thermoplastic materials first, then work down with lower temperature ones in subsequent steps so the earlier ones do not re-melt. For example, if a board were to have PTH vias running through it, and were to be heated such that thermoplastic films softened, they could 'swim' and melt in subsequent bonding steps; unless everything were to be perfectly flat, features would wander off in a direction.

4) Multilayer Build-Up

Applying simple basic rules where possible can go a long way to help aid manufacturing and these can be applied right from the outset. When considering the initial build-up, we recommend applying these 3 rules to help maintain flatness.

a) The minimum risk is to use the same material and bond film throughout the build.

b) Where different materials must be used we recommend keeping the build-up of laminates and bond films symmetrical.

c) Where neither of the above options are possible we would recommend using a 1: >2.5 rule if an asymmetric design is required so that there is a significant difference between materials used within the build. This will help to minimize the effects of mismatched CTEs between the materials by making one material dominant.

[1] Pre-preg is a fibreglass cloth impregnated with a "B" staged resin (dried but not cured). When heated under pressure it flows and bonds the layers together, hardening when fully cured to form a laminate.

When a circuit is constructed as sub-boards i.e. multiple bonding stages it is obviously important that scaling of the sub-boards match, and in this case asymmetry within a sub-board stack can cause issues in manufacture. For example, if sub-boards are significantly bowed due to CTE mismatch of materials it can be extremely difficult to process even if ultimately the final build is symmetrical once all the parts are brought together.

An example of extreme bowing is shown in Figure 8. Here board layers were removed from a press on a leader board; upon release of pressure, the two bowed layers rolled up like scrolls, as can be seen in the left hand photo. Subsequent unrolling shows evidence of distortions arising from CTE mismatch stresses.

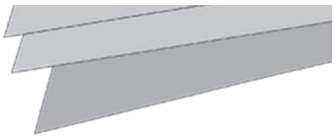

Figure 7: Illustration of layer bowing

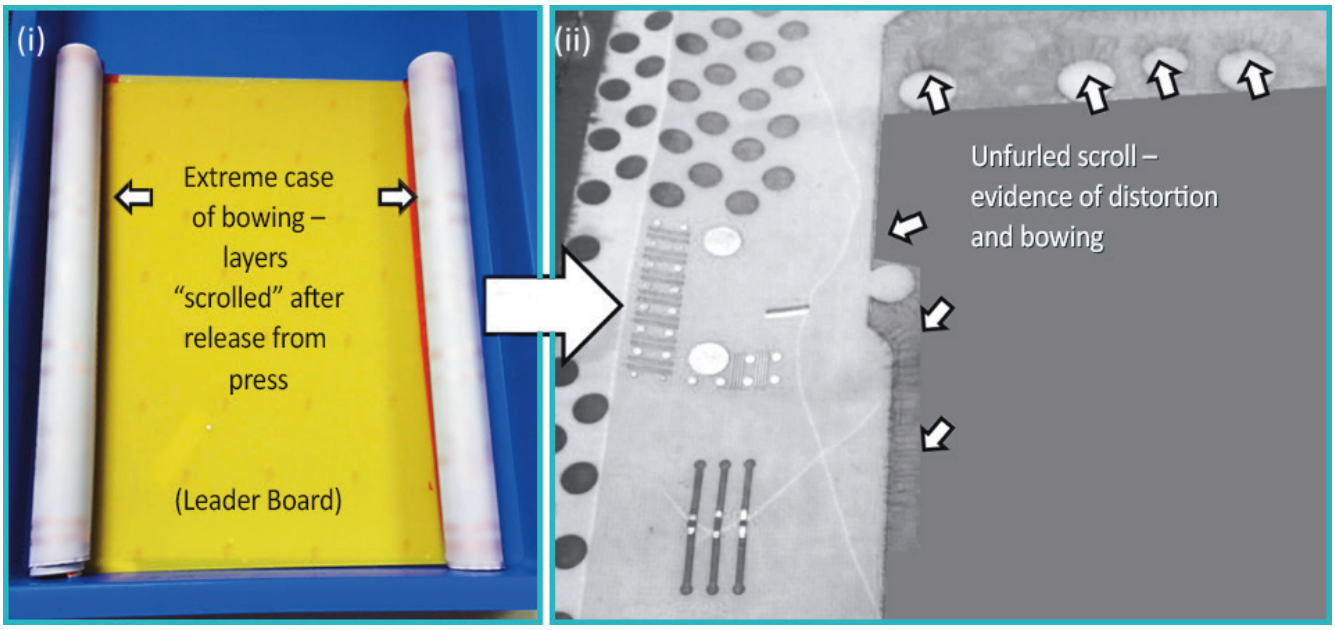

Figure 8: Example of extreme bowing

5) Via Types and Spans

Traditionally connections are made via plated through holes running through the complete stack. As complexity has increased it has become necessary to have multiple different via spans, with a real example shown in Figure 9 (i). Figure 9 (ii) shows a conceptual example where we have via spans and 4 bond stages (B1 to B4). The order and sequence must be considered carefully.

a) L1 to L4 is drilled through sub-board with plated and filled vias[2] (B3)

b) L12 to L13 Laser drilled blind holes may be copper filled (B1).

c) L11 to L15 drilled through sub-board with plated and filled vias (B2)

[2] When vias are to be filled with a higher solids content plug paste the minimum substrate thickness is 0.254mm and must have a woven glass reinforcement to avoid dimensional stability issues.

d) L1 to L10 drilled through entire stack, plated and back drilled from L15 (B4)

e) L1 to L12 drilled through entire stack, plated and back drilled from L15 (B4)

f) L1 to L15 drilled (B4)

Sub-boards allow through-drilling before complete assembly, minimizing the need for blind vias.

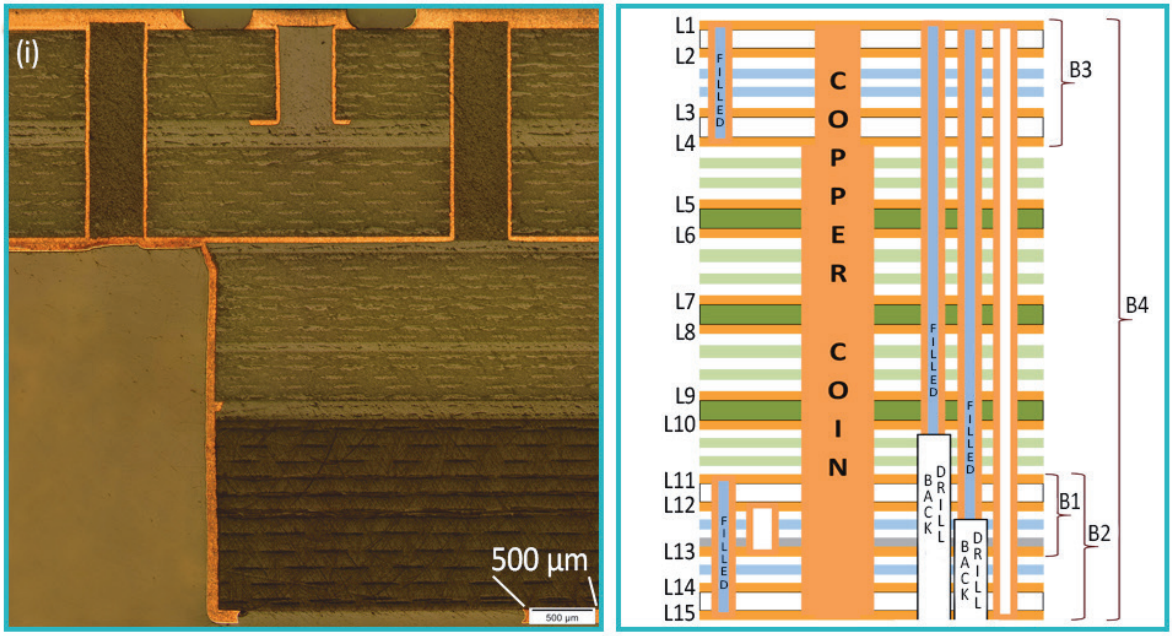

Figure 9: (i) A board with complex via spans. (ii) A hypothetical example stack build-up

The aspect ratio of hole length to diameter must be considered in each case. Holes drilled as blind should have a maximum aspect ratio of 1:1 and through holes not greater than 12:1 aspect ratio. So why the issue with aspect ratios? Particularly with small geometries, aspect ratio can be a big issue, as the plating process involves getting a solution into a small hole, getting air out of it, and getting solution movement within it, with physics and chemistry working against achieving an even and unbroken coating.

While through holes are most desirable, sometimes in complex structures blind vias cannot be avoided. These can be constructed as through-hole vias and then back-drilled. The accuracy of back-drilling is important, as drilling too deeply will cut through the pad, severing the intended electrical connection; drilling too shallow leaves the connections safely intact, but also excess conductor which can act as a stub antenna, radiating unintended microwave energy (Figure 10). Where holes are back drilled the stub that remains before reaching the target layer will nominally be 100µm in length +/-25µm. We recommend that holes to be back drilled are prefilled with a high solids content paste and cured prior to back drilling. This is especially important if PTFE based substrates are being used.

Figure 10: Insufficient back-drilling depth leaving a stub antenna

Note that in some cases blind vias between certain layers, or in certain locations, may not be possible. An example is shown in Figure 11. In (i), placement of logic lines on the top layer deny access for back-drilling to layers below. The case shown in (ii) has layer connections that cannot be built up as through vias from two sub-boards, as the spans overlap.

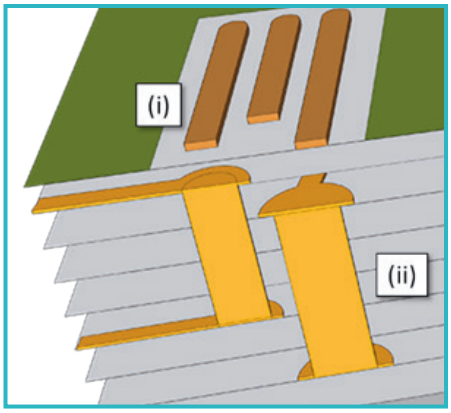

Figure 11: Shows a case where blind vias are not possible as sequential build through vias. Either (i) or (ii) will have to be processed as blind vias with aspect ratio 1:1 or less

6) Embedded Resistors

It is increasingly common to embed discrete components such as resistors inside boards. A typical application will be the formation of a Wilkinson divider in a phased array system, where often two separate layers will support a divider network each. Embedding reduces the overall size of the assembly. Traditionally discrete chip resistors were used, and this still makes sense if the power dissipation of each resistor is greater than 200mW, or the value tolerance must be within tight limits. Otherwise it is more cost-effective to use printed resistors, which are deposited as part of a layer and are particularly beneficial where tens or hundreds of components are required.

Teledyne Labtech can offer the following options:

a) Discrete chip resistors soldered in place

b) Discrete chip resistors attached using conductive (Ag epoxy) adhesive

c) Ohmega-Ply® or Ticer® foil printed resistors

d) Discrete resistors using Ohmega-Ply or Ticer foil

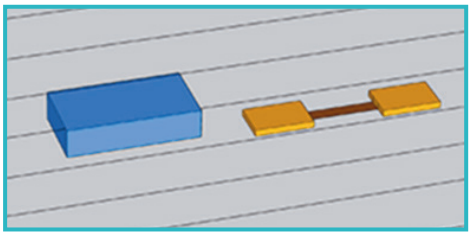

Figure 12: Discrete embedded chip resistor (left) and printed resistor with too little surface area (right)

When discrete embedded chip resistors are to be fitted using solder it is essential that the liquidus temperature of the solder is > 40°C higher than the bonding temperature of the bond film/prepreg. Discrete chip resistors are usually only required when tighter than +/-10% tolerance of resistance values is required and power dissipation is >0.2W although this is dependent upon the area of the resistor element. For 50Ω per square Ohmega-Ply the power versus resistor patch area[3] (with A in mm^2) is ($mW = 173 \times A^{0.35}$). There is a trend towards using printed resistors using Ohmega-Ply or Ticer foil where typically tolerances of +/-10% can be reliably achieved when using 50Ω/ square material. Financially there is a clear benefit using printed resistors when there are many resistor elements per circuit. There is however a need to avoid very small geometries, i.e. not less than 0.2 x 0.2mm for 50Ω/ square, so that manufacturing tolerances do not impact significantly to the final resistor values. To minimise RF losses it is preferred to utilise Ohmega-Ply or Ticer foil as "discrete" resistors that avoid the presence of the resistive layer under the conductors carrying the RF signals. An example of an embedded chip resistor is shown in Figure 13 (i), and a printed embedded resistor formed using Ohmega-Ply is shown in (ii).

[3] Source: Ohmega Technologies. Inc.

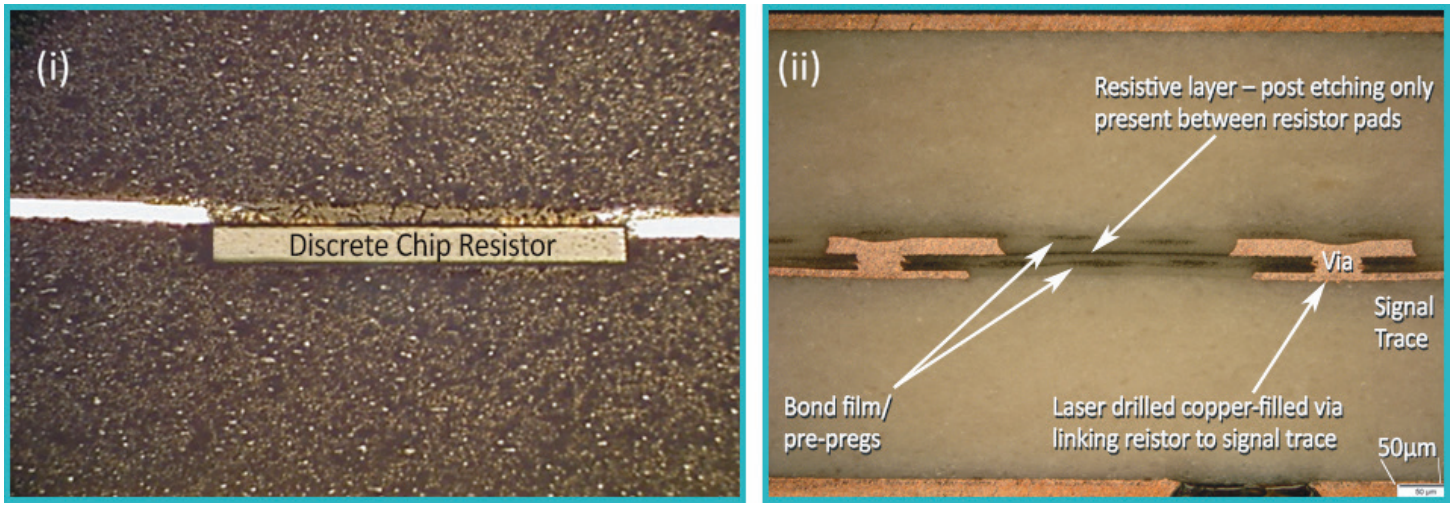

Figure 13: Embedded chip resistor (i), and printed resistor (ii)

7) Surface Finishes

Surface finish of the conductors is important on an RF circuit and can directly impact upon the performance. This does depend on what signal traces are on the outer surfaces of the PCBs. Stripline designs may only have small interface pads on the surface so industry standard Electroless Nickel Immersion Gold (ENiG) finish is acceptable. However, where signal traces are on the surface ENiG is generally accepted to be too lossy, especially if the path lengths are extended beyond a few millimeters.

Most of the available plated finishes are less conductive than copper so will increase the conductor losses. Immersion silver, however, does not have any detrimental impact on performance although it is very sensitive to handling and cannot be readily reworked. The losses due to ENiG rise with increasing frequency and with reduction in substrate thickness. Solder mask should not be applied over RF signal traces as this will increase losses and where necessary be limited to small dams to control solder flow.

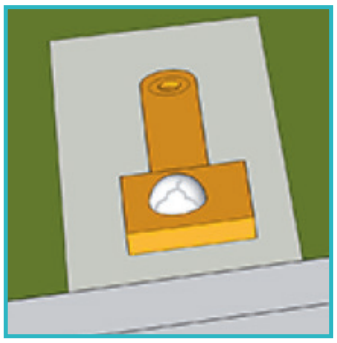

Figure 14: Solder joint on layer of gold which is too thick can lead to solder embrittlement

Electroless Nickel Electroless Palladium Immersion Gold (ENEPiG) is slightly less lossy than ENiG and is favoured for Ka-Band and higher frequencies especially where both SMT assembly and gold wire bonding are required. In all three cases ENiG, Immersion Silver and ENEPiG are electroless/immersion (ion exchange) processes that coat all surfaces of exposed conductors including tracks edges so are relatively straight forward to apply and give a uniform thickness. In terms of cost, immersion silver is the lowest with ENEPiG being the highest, mainly driven by the palladium content.

Pure soft gold 3 to 5µm thick is often called for when wire bonding is to be performed and is usually over a nickel layer 1 to 3µm. If soldering is also required then the gold is plated selectively with wire bonding sites being 3 to 5µm and the rest of traces being kept below 1µm to avoid gold embrittlement issues with solder joints. Generally this type of finish has to be applied prior to etching the track features as it is a galvanic process and requires all features to be connected so the edges of tracks will have exposed copper on finished circuits. Figure 15 shows a typical cross-section of gold over nickel over copper of a track on a high Dk substrate. This finish is more expensive than the electroless/ immersion processes.

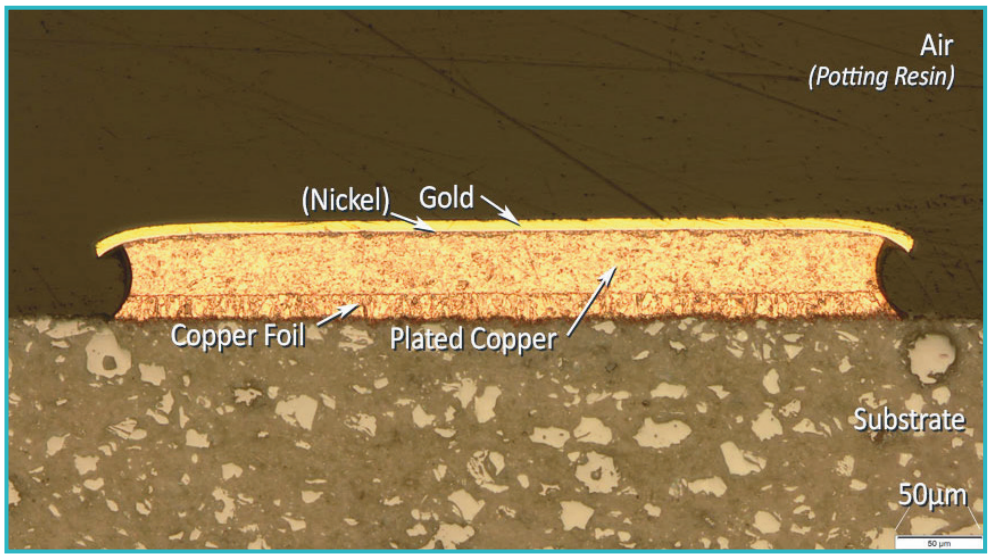

Figure 15: Typical cross-section of gold over nickel over copper of a track on a high Dk substrate. Note the substrate is typical of high Dk materials, where the base material such as PTFE has particles of materials such as alumina trapped within it to raise the overall dielectric coefficient

Where contact pads are required for edge connectors or spring-loaded contacts, hard gold can be selective plated with a nickel under layer to provide a more durable surface.

Summary

Many traps wait to ensnare the microwave board designer, and we've toured a selection of them in this paper. While circuit modeling tools have improved greatly in recent years, they generally do not account for all of the practicalities involved with the successful execution of a board from concept to physical reality. We examined each stage of board production starting with the base laminate and building from there. Many issues relate to choice of materials, and how they react during processing steps – the chemistry and physics – which will impact the performance of the final product, the cost of producing it, or its subsequent reliability. Many issues become tradeoffs rather than black and white, right or wrong answers, and a strong partnership between designer and manufacturer can help find the right balance.

About Teledyne Labtech

Teledyne Labtech specializes in the more challenging projects, with extensive experience in large and complex microwave circuits with applications ranging from commercial in-flight entertainment antennas to ultra-high performance military T/R modules. We are experts where size/weight and power are critical parameters, including where thermal management is key. With over 30 years of experience, we offer practical advice to get your project into production with the minimum of bumps along the way. For more information visit: https://www.teledynedefenseelectronics.com/labtech/

About the Authors

John Priday, Chief Technical Officer of Teledyne Labtech, developed Labtech's microelectronic assembly (chip and wire) facility and oversees all microwave testing services. He started his career with Marconi Radar before moving the Marconi Research Centre in Great Baddow.

John Leafe is Labtech's CAM Manager and leads the New Product Introduction team; in his spare time he likes to participate in sporting activities, and his latest craze is mountain running.

Appendix 1: Common Microwave Materials

The table shows some common example microwave PCB materials, ordered in increasing value of the dielectric constant, Dk.

Dk @ 10GHz	MATERIAL	SUPPLIER	Df @ 10GHz	CTE (ppm/°C) X	CTE (ppm/°C) Y	CTE (ppm/°C) Z	Moisture Absorption (%)	Tg °C	Peel Strength (lbs/in)	Thermal Cond. (W/m/K)	Dk Breakdown (kV/mil)	UL - 94	COMMENTS
1.15-1.35	Foamclad	Arlon	0.002-0.005	25	25		<0.5		7				Polymeric core & polymer film
2.08	NY9208	Neltec	0.0006	25	35	260							Woven glass PTFE
2.1	CuFlon	Polyflon	0.00045	129	129	129	0.01	X	8	X	X	X	Pure PTFE
2.10, 2.20	CuClad 217 LX	Arlon	0.0009	29	28	246	0.02	X	14	0.261	X	VO	Woven PTFE Crossplied
2.10, 2.20	DiClad 880	Arlon	0.0009	25	34	252	0.02	X	14	0.261	X	VO	Woven PTFE Unidirectional
2.10, 2.20	Isoclad 917	Arlon	0.0013	46	47	236	0.04	X	10	0.263	X	VO	Non-woven PTFE/Glass
2.15	605	Taconic	0.0009										Woven glass PTFE
2.17	Ultralam 1217	Rogers	0.0009	20	20	280							Woven glass PTFE
2.17	NY9217	Neltec	0.0008	25	35	260	0.02	X	12-16	0.272	50	V0	Woven PTFE/Glass
2.17	TLY5A	Taconic	0.0009	20	20	280	<0.02	X	12	0.22	X	VO	PTFE/Glass
2.17,2.20	DiClad880-PIM	Arlon	0.0009	25	34	252	0.02	X	12	0.261	X	VO	PIM Laminate. Woven Glass/PTFE
2.2	605	Taconic	0.0009	20	20	280	<0.02	X	12	0.22	X	VO	PTFE/Glass Equivalent to TLY-5
2.2	602	Taconic	0.0019	20	20	280	<0.02	X	12	0.22	X	VO	PTFE/Glass Equivalent to TLY-5
2.2	NY9220	Neltec	0.0009	25	35	260	0.02	X	12 -16	0.272	50	VO	Woven PTFE/Glass
2.2	RT/Duriod 5880	Rogers	0.0009				0.9	>260	22.8	0.2	X	VO	PTFE
2.2	TLY5	Taconic	0.0009	20	20	280	<0.02	X	12	0.22	X	VO	PTFE/Glass
2.32	Polyguide	Polyflon	0.0005	108	108	108	<0.01	X	X	X	X	X	High density polyolefin
2.33	CuClad 233 LX	Arlon	0.0013	23	24	194	0.02	X	14	0.258	X	VO	Woven PTFE Crossplied
2.33	DiClad 870	Arlon	0.0013	17	29	217	0.02	X	14	0.257	X	VO	Woven PTFE Unidirectional
2.33	Isoclad 933	Arlon	0.0016	31	35	203	0.05	X	10	0.263	X	VO	Non-woven PTFE/Glass
2.33	NY9233	Neltec	0.0011	25	35	260	0.02	X	12-16	0.272	50	V0	Woven PTFE/Glass
2.33	RT/Duriod 5870	Rogers	0.0012				0.9	>260	20.8	0.22	X	VO	PTFE
2.33	TLY3	Taconic	0.0009	25	35	280	<0.02	X	12	0.22	X	VO	PTFE/Glass
2.40-2.60	605	Taconic	0.001	20	20	280	<0.02	X	12	0.261	X	VO	Woven glass PTFE
2.40-2.60	Ultralam 2000	Rogers	0.0022	9.5	9.5		0.03	X				VO	Woven glass PTFE
2.40-2.60	CuClad 250 GT [2]	Arlon	0.001	18	19	177	0.03	X	X	0.254	X	VO	Woven PTFE Crossplied
2.40-2.60	CuClad 250 GX [3]	Arlon	0.0022	18	19	177	0.03	X	X	0.254	X	VO	Woven PTFE Crossplied
2.40-2.60	DiClad 522	Arlon	0.0022	14	21	173	0.03	X	14	0.254	0.75	VO	Woven PTFE Unidirectional
2.40-2.60	DiClad 527	Arlon	0.0022	14	21	173	0.03	X	14	0.254	0.75	VO	Woven PTFE Unidirectional
2.43	NX9243	Neltec	0.0016	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.45	NX9245	Neltec	0.0016	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.45	TLT0 [7]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.45	TLX0 [6]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.48	NX9248	Neltec	0.0017	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.5	TLT-9	Taconic	0.0019	9	12	140	<0.02	X	12	0.19	X	VO	PTFE/Glass.
2.5	TLX-9	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	PTFE/Glass.
2.5	AD 250	Arlon	0.0018	12	15	95	0.07	X	14	0.235	> 45	VO	Woven PTFE/Glass
2.5	AD-250-PIM	Arlon	0.0018	12	15	95	0.07	X	15	0.235	X	VO	PIM Laminate. Woven Glass/PTFE
2.5	NX9250	Neltec	0.0017	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.54	601	Taconic	0.0019	9	12	140	<0.02	X	12	0.19	X	VO	PTFE/Glass. Equivalent to TLT-8/TLX-8

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Dk @ 10GHz	MATERIAL	SUPPLIER	Df @ 10GHz	CTE (ppm/°C) X	Y	Z	Moisture Absorption (%)	Tg °C	Peel Strength (lbs/in)	Thermal Cond. (W/m/K)	Dk Breakdown (kV/mil)	UL - 94	COMMENTS
2.55	602	Taconic	0.0019	9	12	40	<0.02	X	12	0.19	X	VO	PTFE/Glass. Equivalent to TLT-8/TLX-8
2.55	NX9255	Neltec	0.0018	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.55	TLT8 [7]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	Woven PTFE/Glass
2.55	TLX8 [6]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	Woven PTFE/Glass
2.55 [5]	Norclad	Polyflon	0.0011 [5]	53	53	53	0.06	X	8	X	X		Thermoplastic Polyphenylene Oxide [4]
2.6	NX9260	Neltec	0.0019	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.6	TLT7 [7]	Taconic	0.0019	9	12	140	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.6	TLX7 [6]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.65	TLT6 [7]	Taconic	0.0019	9	12	140	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.65	TLX6 [6]	Taconic	0.0019	9	12	145	<0.02	X	12	0.19	X	VO	PTFE/Glass
2.7	AD 270	Arlon	0.0023	12	15	95	0.07	X	14	0.235	> 45	VO	Woven PTFE/Glass
2.7	NX9270	Neltec	0.002	12	18	150	0.05	X	12-16	0.251	50	VO	Woven PTFE/Glass
2.75	TLC27	Taconic	0.003	9	12	70	<0.02	X	12	0.24	X	VO	PTFE/Glass
2.9	R/Flex 3850 LCP	Rogers	0.002	17	17		0.04	X	5.4			VTM-O	Double clad LCP di electric
2.9	R/Flex 3600 LCP	Rogers	0.002	17	17		0.04	X	6			VTM-O	Single clad LCP di electric
2.92	RT/Duroid 6002	Rogers	0.0012	16	16	24	0.1	X	X	0.6	X	X	Ceramic/PTFE Woven
2.94	CLTE	Arlon	0.0025	10	12	40	0.004	X	7	0.5	X	VO	Ceramic/Woven PTFE
2.94	NX9294	Neltec	0.0022	9	12	71	0.08	X	12-16	0.23	45	VO	Woven PTFE/Glass
2.94	RT/Duroid 6202	Rogers	0.0015	15	15	30	0.1	X	X	0.68	X	VO	PTFE/Ceramic
2.94	RT/Duroid 6002	Rogers	0.0012			12	0.1	X	8.9	0.6	X	VO	Ceramic/PTFE Woven
2.95	AD 295	Arlon	0.003	12	15	95	0.07	X	X	0.235	> 45	VO	Woven PTFE/Glass
2.95	TLE95	Taconic	0.0028	9	12	70	<0.02	X	12	0.2	X	VO	PTFE/Glass
3	ASTRA MT77	Isola	0.0017	12	13	44.7	0.1	200	5.7		45.4	VO	Thermoset/Woven Glass
3	AD 300	Arlon	0.003	12	15	95	0.07	X	14	0.235	> 45	VO	Woven PTFE/Glass
3	AD300-PIM	Arlon	0.003	12	15	95	0.07	X	15	0.235	X	VO	Woven PTFE/Glass
3	N9300-13RF	Neltec	0.004	13	20	67							PTFE,Thermoset,Woven Glass
3	NX9300	Neltec	0.0023	9	12	71	0.08	X	12-16	0.23	45	VO	Woven PTFE/Glass
3	RO3003	Rogers	0.0013	17	17	24	<0.10	X	17.6	0.5	X	VO	Ceramic filled PTFE
3	TLE95	Taconic	0.0028	9	12	70	<0.02	X	12	0.2	X	VO	PTFE/Glass
3	TLC30	Taconic	0.0029	9	12	70	<0.02	X	12	0.24	X	VO	PTFE/Glass
3.02	Tachyon 100g	Isola	0.0021	15	15	45	0.05	185	5.5	0.42	60	VO	Thermoset/Woven Glass
3.02-3.20	GML 1000	GIL	0.004	40	34	80	0.02	1.35	5	0.2	X	VO	Polyester
3.02	RO3203	Rogers	0.0016	13	13	58	<0.1	X	10	0.47	X	VO	Ptfe,Ceramic,Woven Glass
3.05 [5]	Ultem	Polyflon	0.0030 [5]	56	46	56	0.25	X	X	X	X	X	Polyetherimide
3.18	NX9318	Neltec	0.0024	9	12	71							PTFE/Glass
3.2	AD 320	Arlon	0.003	12	15	95	0.07	X	14	0.23	> 45	V0	Ceramic filled PTFE/Glass
3.2	AD320-PIM	Arlon	0.003	12	15	95	0.07	X	15	0.235	X	VO	PIM Laminate. Woven Glass/PTFE
3.2	NX9320	Neltec	0.0024	9	12	71	0.08	X	12-16	0.23	45	V0	Woven PTFE/Glass
3.2	N9320-13RF	Neltec	0.0045	13	20	67							PTFE,Thermoset,Woven Glass
3.2	TLC32	Taconic	0.0029	9	12	70	<0.02	X	12	0.24	X	V0	PTFE/Glass

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3.2	AD320	Arlon	0.003	12	15	95	0.07	X	X	0.235	> 45	V0	Woven PTFE/Glass
3.27	TMM 3	Rogers	0.002	15	15	23	0.06	X	3	0.7	X	X	Ceramic/Polymer
3.3	LNB	Arlon	0.003	17	17	70	0.08	90-95	4	0.45	X		Ceramic filled plastic
3.35	Megtron 7 R-5785(N)	Panasonic	0.002	14-16	14-16	42	0.06	200	4.5			94VO	Thermoset/Woven Glass
3.38	25N	Arlon	0.0025	15	15	52	0.09	X	5	0.45	X	N/A	Thermsoet,Ceramic,Woven Glass
3.38	NH9338	Neltec	0.0025	9	12	71							PTFE,Ceramic, Woven Glass
3.38	RO4003C	Rogers	0.0027	11	14	46	0.04	>280	6	0.62	X	X	Ceramic filled plastic (Non PTFE)
3.4	Megtron 6 R-5775(N)	Panasonic	0.004	14-16	14-16	45	0.14	185	6.9				Thermoset/Woven Glass
3.48	NH9348	Neltec	0.003	9	12	71							Ptfe,Ceramic,Woven Glass
3.48	RO4350B	Rogers	0.0037	14	16	50	0.04	>280	5	0.62	X	VO	Ceramic filled plastic
3.5	N9350-13RF	Neltec	0.0055	13	20	67							PTFE,Thermoset,Woven Glass
3.5	RO3035	Rogers	0.0017	17	17	24	<0.1		9.1	0.5	X	VO	Ceramic/PTFE
3.5	AR350	Arlon	0.0026	35	35	107	0.08	X	12	0.31	X	VO	Non Woven Glass, Ceramic, PTFE
3.5	AD 350	Arlon	0.003	12	15	95	0.07	X	14	0.31	> 45	VO	Ceramic filled PTFE/Glass
3.5	AD350-PIM	Arlon	0.003	12	15	95	0.07	X	15	0.235	X	VO	PIM Laminate, Woven Glass/PTFE
3.5	RF-35 [8]	Taconic	0.0018	19-24	19-24	64	0.02	X	>10.0	0.2	X	VO	Ceramic/PTFE/Woven glass
3.58	25FR	Arlon	0.0035	16	18	59	0.09	X	5	0.45	X	VO	Non PTFE
3.6	Megtron 6 R-5775	Panasonic	0.004	14-16	14-16	45	0.14	185	6.9				Thermoset/Woven Glass
3.61	Megtron 7 R-5785	Panasonic	0.003	14-16	14-16	42	0.06	200	4.5			94VO	Thermoset/Woven Glass
4.5	AR 450	Arlon	0.0035	30	32	102	0.08	X	8	0.32	> 45	VO	Ceramic filled PTFE/Glass
4.5	TMM 4	Rogers	0.002	16	16	21	0.07	X	3	0.7	X	X	Ceramic/Polymer
6	TMM 6	Rogers	0.0023	18	18	26	0.06	X	3	0.76	X	X	Ceramic/Polymer
6.15	RF-60	Taconic	0.0028	11	13	75	<0.02	X	>8.0	0.43	X	VO	PTFE,Ceramic, Woven Glass
6.15	AR600	Arlon	0.0035	12	14	62	0.08	X	6	0.431	> 45	VO	Ceramic filled PTFE/Glass
6.15	RO3006	Rogers	0.002	17	17	24	<0.10	X	12.2	0.61	X	VO	Ceramic filled PTFE
6.15	RT/Duroid 6006	Rogers	0.0027	47	34		0.05	X		0.48	X	VO	Ceramic/PTFE Woven
9.2	TMM 10	Rogers	0.0022	21	21	20	0.09	X	3	0.76	X	X	Ceramic/Polymer
9.8	TMM 10i	Rogers	0.002	19	19	20	0.16	X	3	0.76	X	X	Ceramic/Polymer
10	CER-10	Taconic	0.0035	13-15	13-15	46	0.02	X	5	0.63	X	VO	Ceramic/PTFE/Woven glass
10	AR 1000	Arlon	0.003	14	16	37	0.08	X	5	0.645	> 45	VO	Ceramic filled PTFE/Glass
10.2	RO3210	Rogers	0.0027	13	13	34	<0.10	X	13	0.81	X	VO	Ceramic filled PTFE/Glass
10.2	RO3010	Rogers	0.0023	17	17	24	<0.10	X	13	0.66	X	VO	Ceramic filled PTFE
10.2	RT/Duroid 6010LM	Rogers	0.0023	24	24		0.05	X	X	0.78	X	VO	Ceramic/PTFE/Woven glass

[1] Varies with thickness [2] Thicknesses over copper [3] Thicknesses over dielectric [4] Requires solvent based processing [5] Tested at 3 GHz
[6] Values shown measured at 10GHz [7] Values shown measured at 1MHz [8] Tested at 1.90GHz

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