Revised January 2026

128-Macrocell MAX® EPLD

Features

- **128 macrocells in eight logic array blocks (LABs)**
- **Eight dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Available in 68-pin CLCC, PLCC, and CPGA packages**

Functional Description

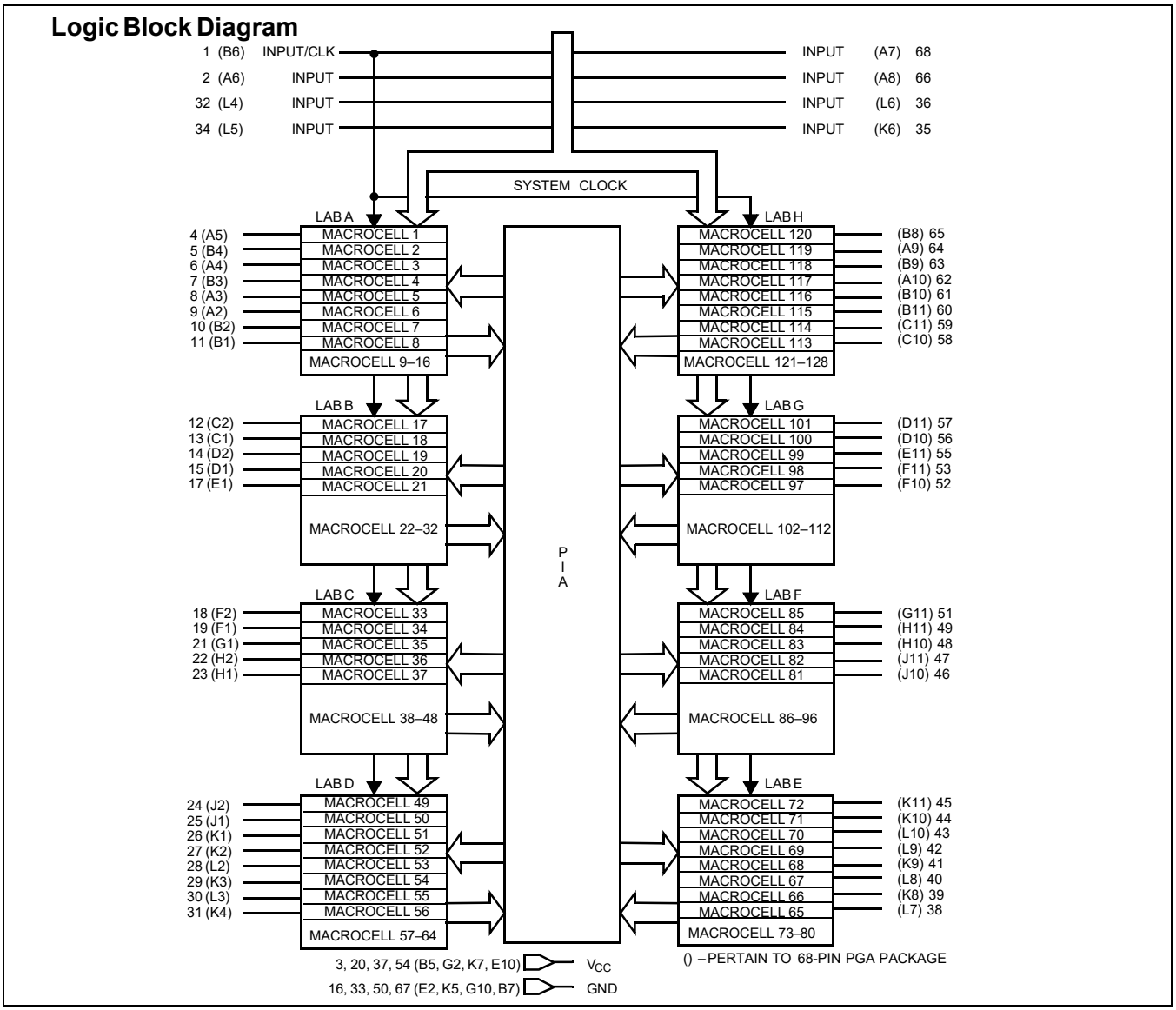
The CY7C342B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX® architecture is 100% user-configurable, allowing the device to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342B are divided into eight LABs, 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342B reduces board space, part count, and increases system reliability.

Logic Block Diagram

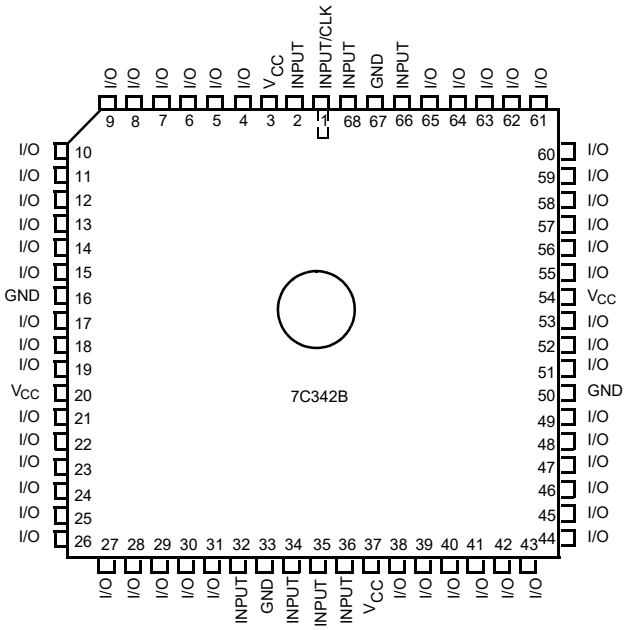


Selection Guide

	7C342B-15	7C342B-20	7C342B-25	7C342B-30	7C342B-35	Unit
Maximum Access Time	15	20	25	30	35	ns

Pin Configurations

CLCC, PLCC
Top View



H81, J81

CPGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L		I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	I/O	I/O	
K	I/O	I/O	I/O	I/O	GND	INPUT	VCC	I/O	I/O	I/O	I/O
J	I/O	I/O								I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	VCC								GND	I/O
F	I/O	I/O				7C342B				I/O	I/O
E	I/O	GND								VCC	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O								I/O	I/O
B	I/O	I/O	I/O	I/O	VCC	INPUT/ CLK	GND	I/O	I/O	I/O	I/O
A	■	I/O	I/O	I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	

R68

Logic Array Blocks

There are eight logic array blocks in the CY7C342B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342B provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals that may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a signal pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342B may be easily determined using *Warp*®, *Warp* Professional™, or *Warp* Enterprise™ software by the model shown in *Figure 1*. The CY7C342B has fixed internal delays, allowing the user to determine the worst-case timing delays for any design.

Design Recommendations

Operation of the devices described herein with conditions above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

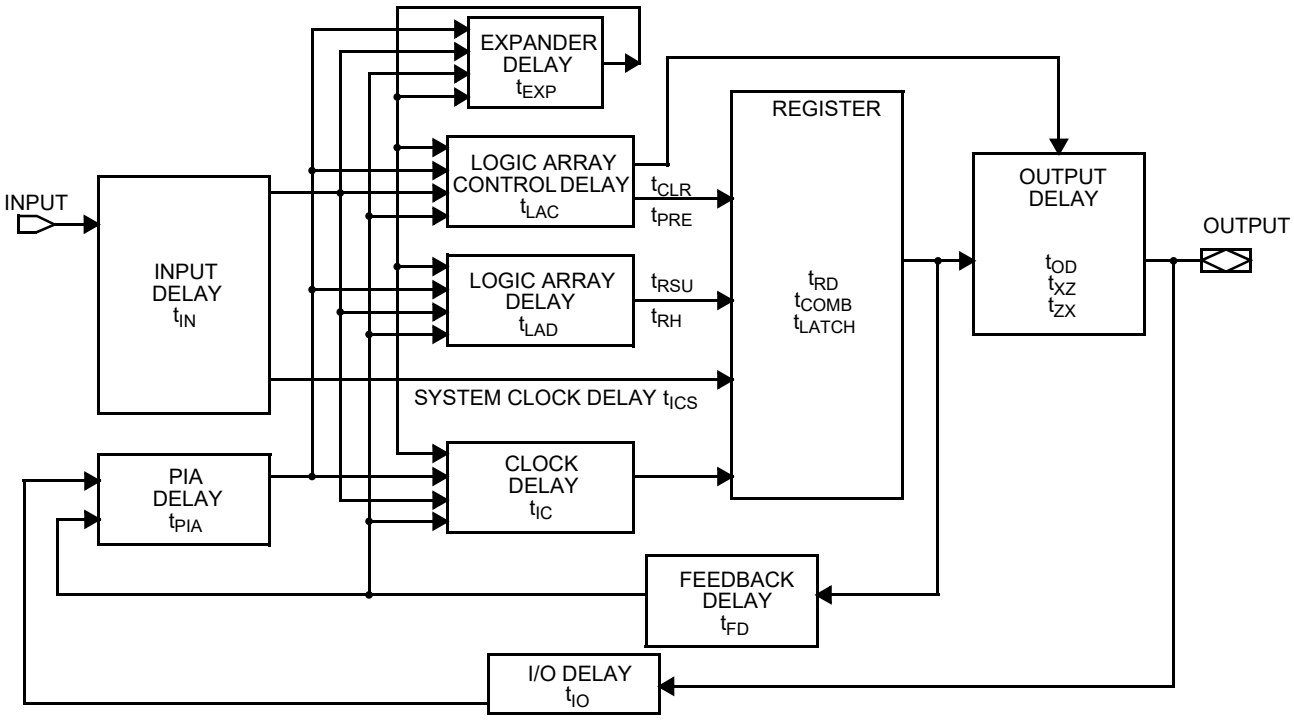


Figure 1. CY7C342B Internal Timing Model

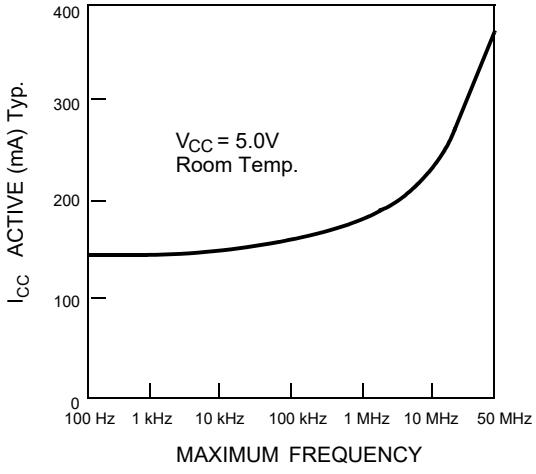
Design Security

The CY7C342B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

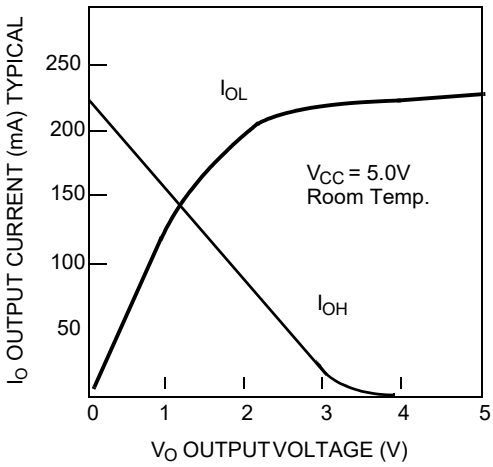
The CY7C342B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{SU} if all inputs are on dedicated input pins. When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +135°C

Ambient Temperature with Power Applied..... –65°C to +135°C

Maximum Junction Temperature (under bias)..... 150°C

Supply Voltage to Ground Potential .....–2.0V to +7.0V[1]

DC Output Current per Pin[1]..... –25 mA to +25 mA

DC Input Voltage[1] .....–2.0V to +7.0V

Operating Range

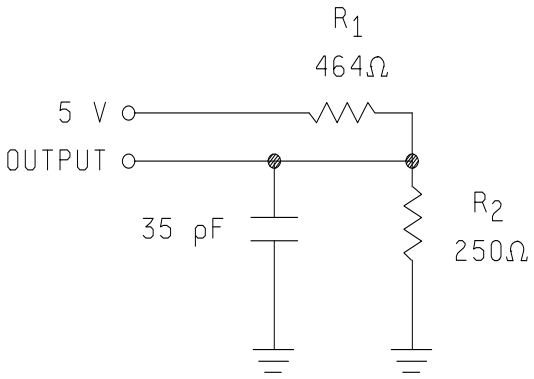
Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%
Military	–55°C to +125 °C	5V ± 10%

Truth Table (unprogrammed)

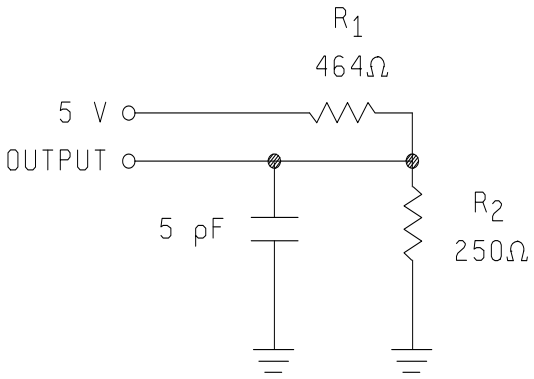
Truth table		
Input pins		Output pins
CP/I		I/O
X		Z

NOTES:
1. = Don't care
2. Z = High impedance

Output load circuit and test conditions



Circuit A
Output Load



Circuit B
Output Load for t_{ER}

Input pulses
AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

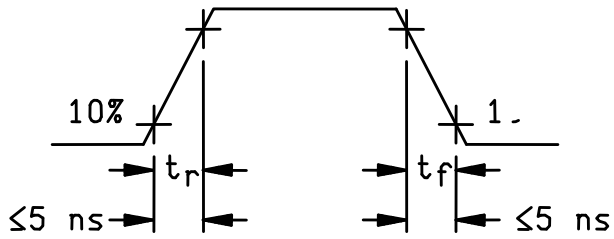


TABLE I. Electrical performance characteristics.

Table I **Dash Number** to **Device Type** Key : 01 = -35 ns, 02 = -30 ns, 03 = -25 ns, 04 = -20 ns, 05 = -15 ns

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = -2.2 V I_{OH} = -4.0 mA, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IH} = 2.2 V I_{OH} = -4.0 mA, V_{IL} = 0.8 V	1, 2, 3	All		0.45	V
Input high voltage 1/ 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 1/ 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{IN} = 5.5 V and GND	1, 2, 3	All	-40	40	µA
Output short circuit current 2/ 3/	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	mA
Power supply current 2/ 4/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = V_{CC} to GND, f = $1/t_{PD1}$	1, 2, 3	All		700	mA
Power supply current (Standby) 2/ 4/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND	1, 2, 3	All		300	mA
Input capacitance 2/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0.0 V, T_A = 25°C, f = 1 MHz (see 4.3.1c)	4	AI		10	pF
Output capacitance 2/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0.0 V, T_A = 25°C, f = 1 MHz (see 4.3.1c)	4	AI		20	pF
Functional tests		See 4.3.1d	7, 8A, 8B	All			
External Synchronous Switching Characteristics							
Dedicated input to combinatorial output delay 6/	t_{PD1}	See figure 5 5/	9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics – Continued.							
I/O input to combinatorial output delay 7/	t_{PD2}	See figure 5 5/	9, 10, 11	01		55	ns
				02		46	
				03		40	
				04		33	
				05		25	
Dedicated input to combinatorial output delay delay with expander delay	t_{PD3}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		10	
I/O input to combinatorial output delay with expander delay 2/ 9/	t_{PD4}		9, 10, 11	01		75	ns
				02		60	
				03		51	
				04		43	
				05		33	
Input to output enable delay 2/ 6/	t_{EA}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Input to output disable delay 2/ 6/ 10/	t_{ER}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		10	
Synchronous clock input to output delay	t_{CO1}		9, 10, 11	01		20	ns
				02		16	
				03		14	
				04		8	
				05		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics – Continued.							
Synchronous clock to local feedback to combinatorial output 2/ 11/	t_{CO2}	See figure 5 5/	9, 10, 11	01		42	ns
				02		35	
				03		30	
				04		22	
				05		17	
Dedicated input or feedback setup time to synchronous clock input 6/ 13/	t_{S1}		9, 10, 11	01	25		ns
				02	20		
				03	15		
				04	13		
				05	10		
I/O input setup time to synchronous clock input 6/	t_{S2}		9, 10, 11	All	0		ns
Input hold time from synchronous clock input 6/	t_H		9, 10, 11	01	12.5		ns
				02	10		
				03	8		
				04	7		
				05	5		
Synchronous clock input high time 2/	t_{WH}		9, 10, 11	01	12.5		ns
				02	10		
				03	8		
				04	7		
				05	5		
Synchronous clock input low time 2/	t_{WL}		9, 10, 11	01	12.5		ns
				02	10		
				03	8		
				04	7		
				05	5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics – Continued.							
Asynchronous clear width 2/ 6 12/	t_{RW}	See figure 5 5/	9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous clear recovery time 2 6/ 12/	t_{RR}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous clear to registered output delay 6/	t_{RO}		9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Asynchronous preset width 2/ 6 12/	t_{PW}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous preset recovery time 2 6/ 12/	t_{PR}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		
Asynchronous preset to registered output delay 6/	t_{PO}		9, 10, 11	01	35		ns
				02	30		
				03	25		
				04	22		
				05	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Synchronous Switching Characteristics – Continued.							
Synchronous clock to local feedback input 2/ 14/	t_{CF}	See figure 5 5/	9, 10, 11	01		6	ns
				02 – 05		3	
External synchronous clock period (t_{CO1} + t_S) 2/	t_P		9, 10, 11	01	45		ns
				02	36		
				03	29		
				04	21		
				05	12		
External feedback maximum frequency 1/(t_{CO1} + t_{S1}) 2/ 15/	f_{MAX1}		9, 10, 11	01	22.2		MHz
				02	27.7		
				03	34.5		
				04	47.6		
				05	58.8		
Internal local feedback maximum frequency, lesser of 1/(t_{S1} + t_{CF}) or 1/(t_{CO1}) 2/ 16/	f_{MAX2}		9, 10, 11	01	32.2		MHz
				02	43.4		
				03	55.5		
				04	62.5		
				05	76.9		
Data path maximum frequency, least of 1/(t_{WL} + t_{WH}), 1/(t_{S1} + t_H) or 1/(t_{CO1}) 12/ 17/	f_{MAX3}		9, 10, 11	01	40.0		MHz
				02	50.0		
				03	62.5		
				04	71.4		
				05	100		
Maximum register toggle frequency 1/(t_{WH} + t_{WL}) 12/ 18/	f_{MAX4}		9, 10, 11	01	40.0		MHz
				02	50.0		
				03	62.5		
				04	71.4		
				05	100		
Output data stable time from synchronous clock input 12/ 19/	t_{OH}		9, 10, 11	All	3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Asynchronous Switching Characteristics							
Asynchronous clock input to output delay 6/	t_{ACO1}	See figure 5 5/	9, 10, 11	01		35	ns
				02		30	
				03		25	
				04		20	
				05		15	
Asynchronous clock input to local feedback to combinatorial output 2/ 20/	t_{ACO2}		9, 10, 11	01		55	ns
				02		49	
				03		41	
				04		32	
				05		25	
Dedicated input or feedback setup time to asynchronous clock input 6/	t_{AS1}		9, 10, 11	01	8		ns
				02	6		
				03 – 05	5		
I/$\overline{O}$ input setup time to asynchronous clock input 6/ 12/	t_{AS2}		9, 10, 11	01	28		ns
				02	22		
				03	19		
				04	18		
				05	14.5		
Input hold time from asynchronous clock input 6/	t_{AH}		9, 10, 11	01	10		ns
				02	8		
				03	6		
				04	6		
				05	5		
Asynchronous clock input high time 2/ 6/	t_{AWH}		9, 10, 11	01	16		ns
				02	14		
				03	11		
				04	7		
				05	9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Asynchronous Switching Characteristics – Continued.							
Asynchronous clock input low time 2 6/	t_{AWL}	See figure 5 5/	9, 10, 11	01	16		ns
				02	14		
				03	11		
				04, 05	7		
Asynchronous clock to local feedback input 2/ 21/	t_{ACF}		9, 10, 11	01		22	ns
				02		18	
				03		15	
				04		13	
				05		11	
External asynchronous clock period (t_{AC01} + t_{AS1}) or (t_{AWH} + t_{AWL}) 2/	t_{AP}		9, 10, 11	01	43		ns
				02	28		
				03	22		
				04	14		
				05	16		
External feedback maximum frequency in asynchronous mode 1/(t_{AP}) 2/ 22/	f_{MAXA1}		9, 10, 11	01	23.2		MHz
				02	27.7		
				03	33.3		
				04	40		
				05	50		
Maximum internal asynchronous frequency 1/(t_{AS2} + t_{ACF}) or 1/t_{ACO1} 2/ 25/	f_{MAXA2}		9, 10, 11	01	20		MHz
				02	25		
				03	29.4		
				04	32.3		
				05	62.5		
Data path maximum frequency In asynchronous mode 1/(t_{AWH} + t_{AWL}) or 1/(t_{AS1} + t_{AH}) or /t_{ACO1} 12/ 24/	f_{MAXA3}		9, 10, 11	01	28.5		MHz
				02	33.3		
				03	40		
				04	50		
				05	66.6		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Asynchronous Switching Characteristics – Continued.							
Maximum asynchronous register toggle frequency $1/(t_{AWH} + t_{WL})$ 12/ 23/	f_{MAXA4}	See figure 5 5/	9, 10, 11	01	10		MHz
				02	8		
				03	6		
				04	6		
				05	5		
Asynchronous clock input high Time 2 6/ –	t_{AWH}		9, 10, 11	01	16		ns
				02	14		
				03	11		
				04	7		
				05	9		
Asynchronous clock input low time 2/ 6/	t_{AWL}		9, 10, 11	01	16		ns
				02	14		
				03	11		
				04 – 05	7		
Asynchronous clock to local feedback input 2/ 21/	t_{ACF}		9, 10, 11	01		22	ns
				02		18	
				03		15	
				04		13	
				05		11	
External asynchronous clock period $(t_{ACO1} + t_{AS1})$ or $(t_{AWH} + t_{AWL})$ 2/	t_{AP}		9, 10, 11	01	43		ns
				02	28		
				03	22		
				04	14		
				05	16		
External feedback maximum frequency i asynchronous mode $1/(t_{AP})$ 2/ 22/	f_{MAXA1}		9, 10, 11	01	23.2		MHz
				02	27.7		
				03	33.3		
				04	40		
				05	50		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External Asynchronous Switching Characteristics – Continued.							
Maximum internal asynchronous frequency $1/(t_{AS2} + t_{ACF})$ or $1/t_{ACO1}$ 2/ 25/	f_{MAXA2}	See figure 5 5/	9, 10, 11	01	20		MHz
				02	25		
				03	29.4		
				04	32.3		
				05	62.5		
Data path maximum frequency in asynchronous mode $1/(t_{AWH} + t_{AWL})$ or $1/(t_{AS1} + t_{AH})$ or $/t_{ACO1}$ 12/ 24/	f_{MAXA3}		9, 10, 11	01	28.5		MHz
				02	33.3		
				03	40		
				04	50		
				05	66.6		
Maximum asynchronous register toggle frequency $1/(t_{AWH} + t_{AWL})$ 12/ 23/	f_{MAXA4}		9, 10, 11	01	31.2		MHz
				02	35.7		
				03	45.5		
				04	71.4		
				05	62.5		
Output data stable time from – asynchronous clock input – 12/ 26/	t_{AOH}		9, 10, 11	All	12		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.
4/ Specified with device programmed as a 16-bit counter in each LAB. Tested with manufacturer test pattern and shall be made available upon request.
5/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 4, circuit A.
6/ This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.

When this note is applies to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.

If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.

7/ This parameter is the delay from an input signal applied to an I/O microcell pin to any output. This delay assumes no expander terms are used to form the logic function.

TABLE I. Electrical performance characteristics – Notes Continued.

8/ This parameter is the delay from an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

9/ This parameter is the delay from an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.

10/ Transition is measured ± 0.5 V from steady state voltage on the output from the 1.5 V level on the input with the load on figure 4, circuit B.

11/ This specification is the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes that no expanders are used, register is synchronously clocked and all feedback is within the same LAB.

12/ Values guaranteed by design and are not tested.

13/ If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.

14/ This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB.

15/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.

16/ This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.

17/ This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.

18/ This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.

19/ This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

20/ This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB.

21/ This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin.

22/ This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.

23/ This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.

24/ This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/(t_{ACO1})$. It assumes data and clock input signals are applied to dedicated input pins and no expander logic is used.

25/ This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.

This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB.

26/ This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

Terminal connections.

Device types	All	Device types	All
Case outlines	H81, J81	Case outlines	H81, J81
Terminal number 1/	Terminal symbol	Terminal number 1/	Terminal symbol
1	I/CLK	35	I
2	I	36	I
3	VCC	37	VCC
4	I/O	38	I/O
5	I/O	39	I/O
6	I/O	40	I/O
7	I/O	41	I/O
8	I/O	42	I/O
9	I/O	43	I/O
10	I/O	44	I/O
11	I/O	45	I/O
12	I/O	46	I/O
13	I/O	47	I/O
14	I/O	48	I/O
15	I/O	49	I/O
16	GND	50	GND
17	I/O	51	I/O
18	I/O	52	I/O
19	I/O	53	I/O
20	I/O	54	VCC
21	I/O	55	I/O
22	I/O	56	I/O
23	I/O	57	I/O
24	I/O	58	I/O
25	I/O	59	I/O
26	I/O	60	I/O
27	I/O	61	I/O
28	I/O	62	I/O
29	I/O	63	I/O
30	I/O	64	I/O
31	I/O	65	I/O
32	I	66	I
33	GND	67	GND
34	I	68	I

1/ Terminal numbers are referenced to the electrical pin one.

Terminal connections - Continued.

Case outline R68

1	2	3	4	5	6	7	8	9	10	11	
	I/O	I/O	I	I	I	I/O	I/O	I/O	I/O		L
I/O	I/O	I/O	I/O	GND	I	V_{CC}	I/O	I/O	I/O	I/O	K
I/O	I/O								I/O	I/O	J
I/O	I/O								I/O	I/O	H
I/O	V_{CC}								GND	I/O	G
I/O	I/O								I/O	I/O	F
I/O	GND								V_{CC}	I/O	E
I/O	I/O								I/O	I/O	D
I/O	I/O	1/							I/O	I/O	C
I/O	I/O	I/O	I/O	V_{CC}	I/CLK			I/O	I/O	I/O	B
	I/O	I/O	I/O	I/O	I	I	I	I/O	I/O		A
1	2	3	4	5	6	7	8	9	10	11	

BOTTOM VIEW

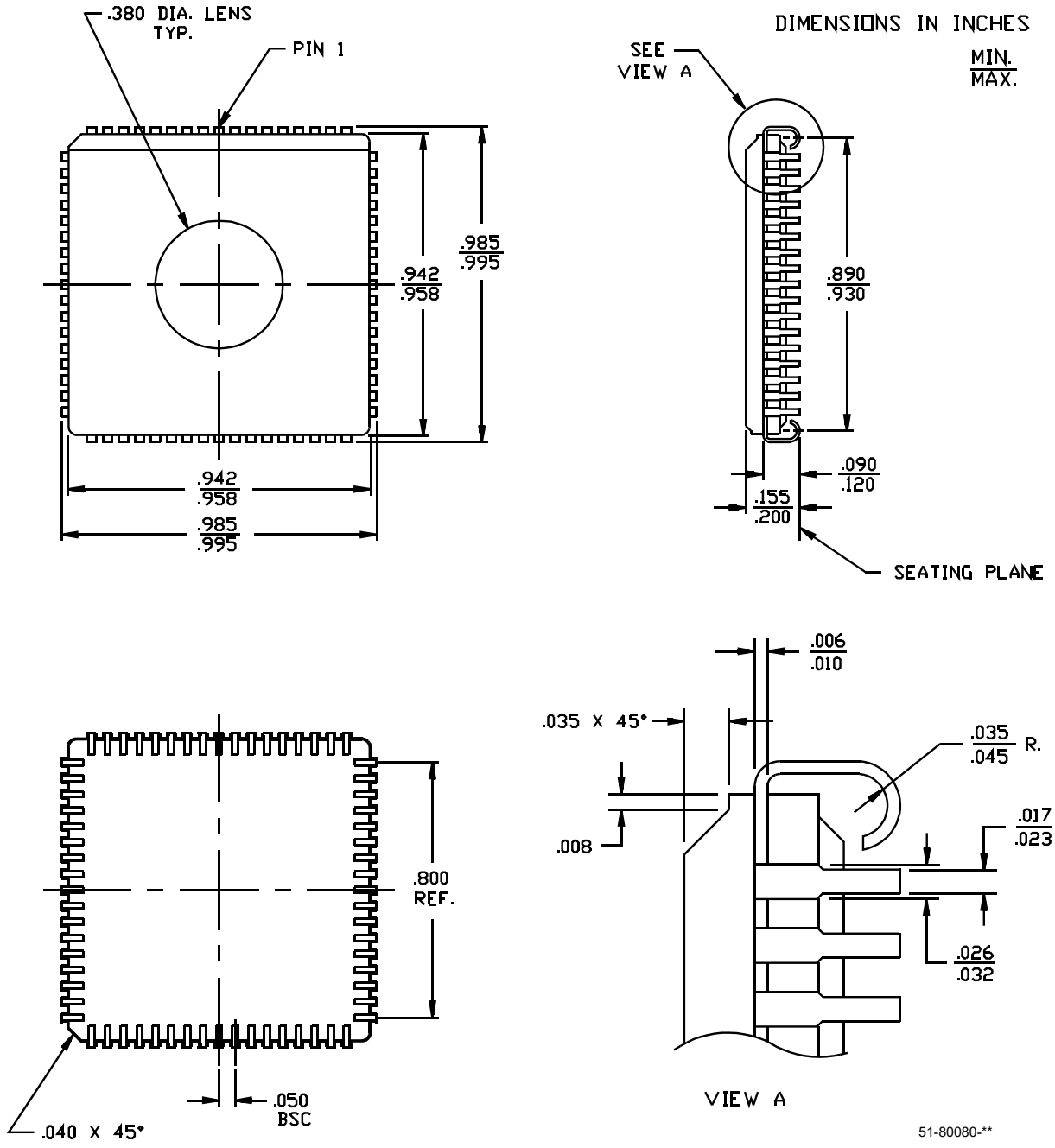
1/ Reference mark

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C342B-15JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
20	CY7C342B-20JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
25	CY7C342B-25HC/HI	H81	68-pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B-25JC/JI	J81	68-lead Plastic Leaded Chip Carrier	
	CY7C342B-25RC/RI	R68	68-pin Windowed Ceramic Pin Grid Array	
30	CY7C342B-30JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B–30HC/HI	H81	68-Pin Windowed Leaded Chip Carrier	
35	CY7C342B-35JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B-35RJ/RI	R68	68-pin Windowed Ceramic Pin Grid Array	

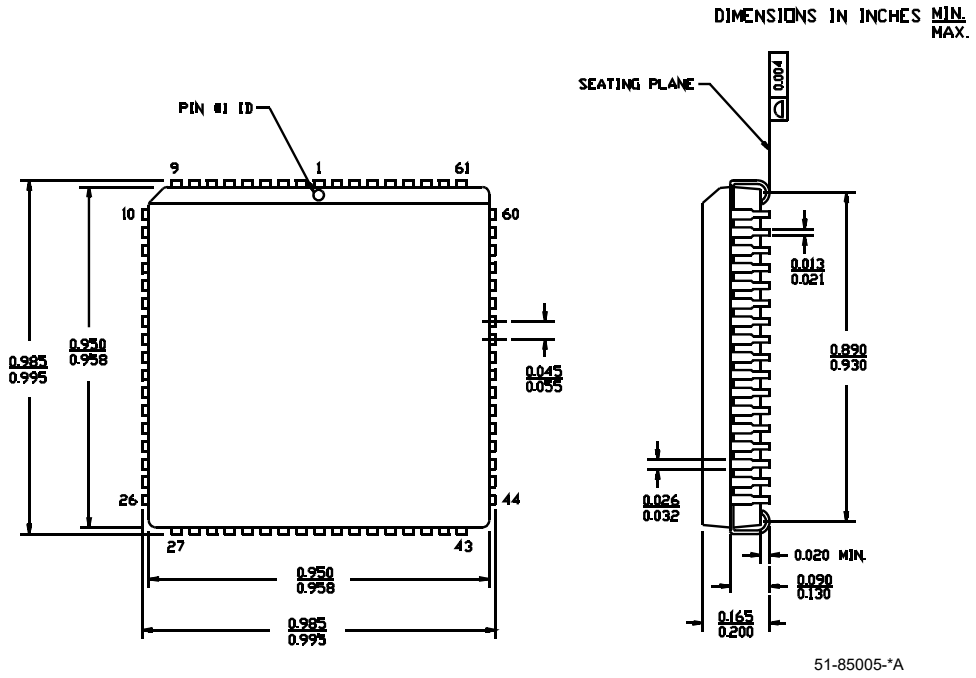
Package Diagrams

68-pin Windowed Leaded Chip Carrier H81
and conforms to MIL-STD-1835D descriptive designator
GQCC1-J68 with transparent window



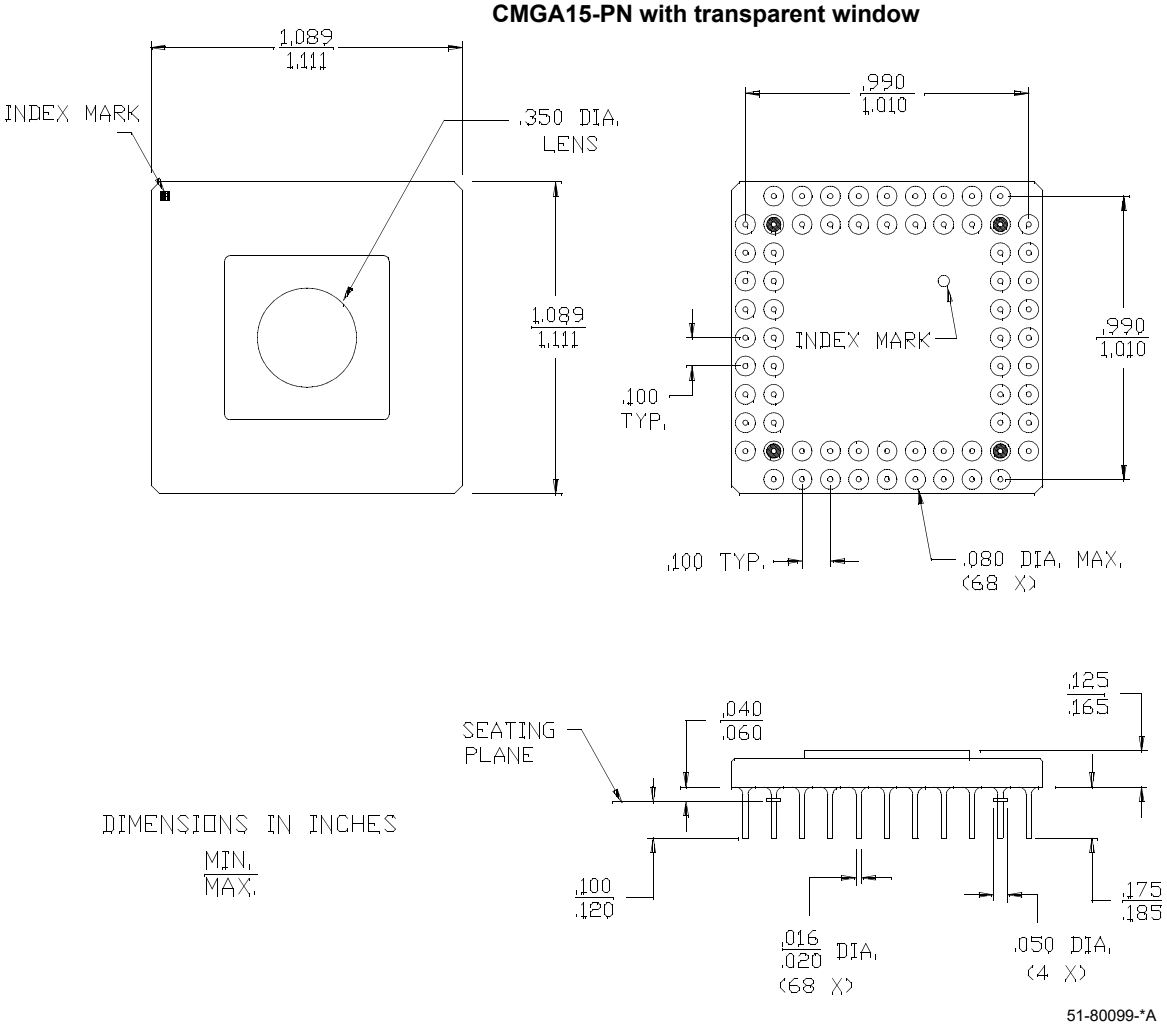
Package Diagrams (continued)

68-lead Plastic Leaded Chip Carrier J81



Package Diagrams (continued)

68-Pin Windowed PGA Ceramic R68
and conforms to MIL-STD-1835D descriptive designator
CMGA15-PN with transparent window



Document History Page

Document Title: CY7C342B 128-Macrocell MAX® EPLD Document Number: 38-03014				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106314	04/25/01	Cypress	Change from Spec number: 38-00119 to 38-03014
*A	113612	04/11/02	Cypress	PGA package diagram dimensions were updated
*B	213375	See ECN	Cypress	Added note to title page: “Use Ultra37000 For All New Designs”
*C	N/A	N/A	Teledyne	Added PNs CY7C342B-30HC/HI to the Ordering Information Table and updated TAble 1. Added PCGA package pinout diagram.

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