Teledyne HiRel Semiconductors
Aerospace & Defense Electronics

TDLNA002093

Product Specification

Ultra-Low Noise Amplifier Tuning Range: 1.0 to 6.0 GHz

Features

Reference: 5 V / 55 mA / 2.33 GHz

- EVB Noise Figure (NF): 0.37 dB
- Gain: 22.0 dB
- OP1dB: 19.0 dBm
- OIP3: 35.5 dBm
- Flexible Bias Voltage and Current
- Process: GaAs pHEMT
- TID: 100 krad (Si)

Applications

- Satellite Communications
- Military and Space Applications
- Distributed Antenna Systems
- GPS Receivers

Description

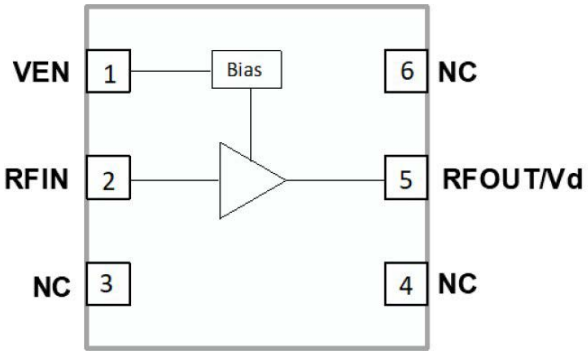
The TDLNA002093 ultra-low noise amplifier offers industry-leading noise figure (NF) and gain performance and can be tuned over a wide range of frequencies from roughly 1.0 to 6.0 GHz.

With application-specific biasing, TDLNA002093 is part of Teledyne e2v's new, high performance harsh environment MMIC solutions suitable for use as the first-stage LNA for advanced satellite or military communication receivers.

It can be biased over a range of Vdd from 2.7 to 5.0 volts and typical Iddq values from 30 mA to 100 mA.

The device uses a hermetic DFN package and standard LNA pin out, and the device can be screened for military and space applications per customer requirements.

3 mm x 3 mm DFN
Functional Block Diagram
Top View



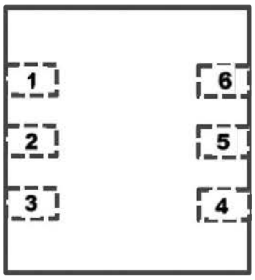
Absolute Maximum Ratings:

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	0	6.0	V
RF Input Power CW: (Load VSWR < 2:1; V_D: 5.0 volts)	$P_{IN\ MAX}$		23	dBm
Operating Temperature (Package Heat Sink)	T_{AMB}	-55	125	°C
Maximum Channel Temperature (MTTF > 10^6 Hours)	T_{MAX}		170	°C
Maximum Dissipated Power	$P_{DISS\ MAX}$		1000	mW
Electrostatic Discharge:				
Charged Device Model:	CDM	1000		V
Human Body Model:	HBM	500		V
Storage:				
Storage Temperature	T_{STG}	-65	150	°C

Caution! ESD Sensitive Device

Exceeding Absolute Maximum Rating conditions may cause permanent damage to the device.

Pin Out (Top View)



Pin Assignments: (3 x 3 mm DFN package type)

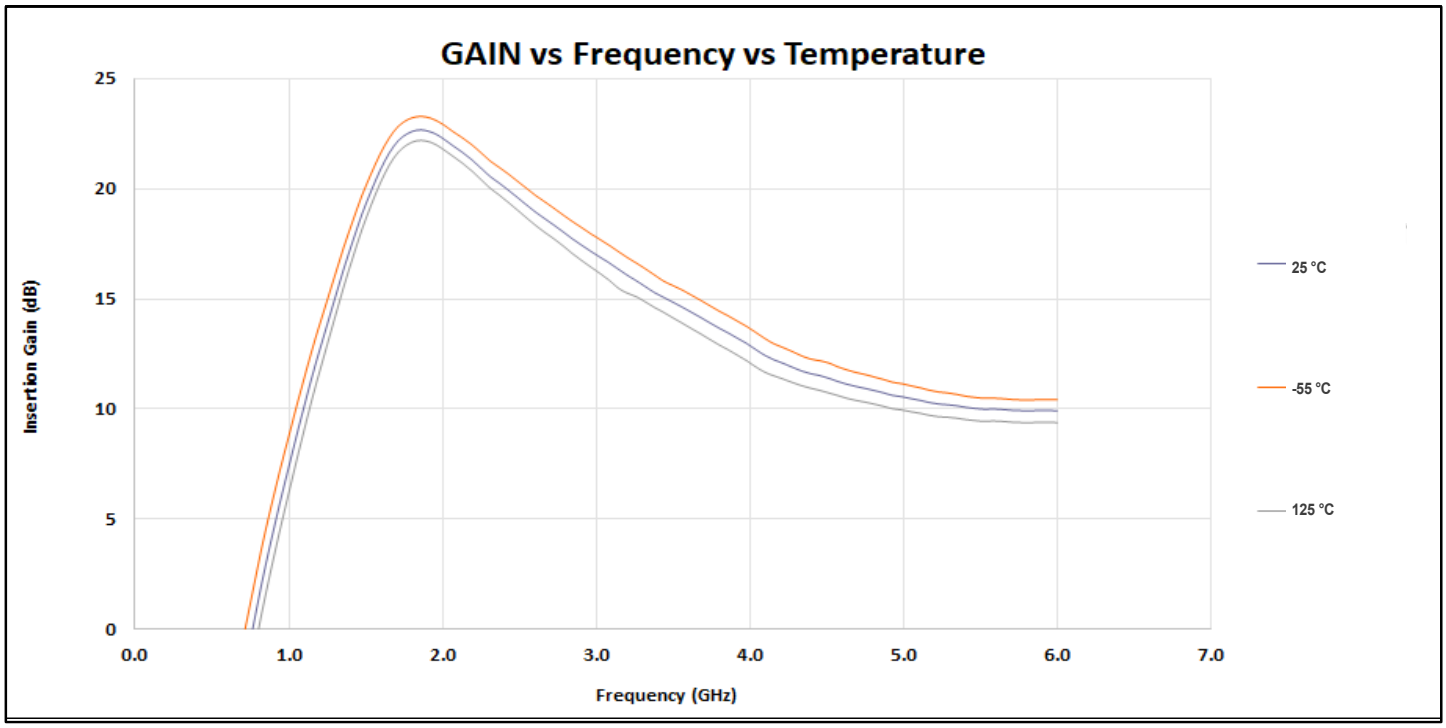
Pin	Name	Description	Note
1	**VENABLE**	Enable Voltage Input	VENABLE and series resistor set IDDQ. VENABLE < =0.2 volts disables device. On die pull-down resistor will turn the part off if this node is allowed to float.
2	RF_In	LNA RF input	An external DC blocking cap must be used.
3	NC	No Connect or Ground	No internal connection to die
4	NC	No Connect or Ground	No internal connection to die
5	RF_Out	LNA RF output	VDD must be applied through a choke to this pin.
6	NC	No Connect or Ground	No internal connection to die
PKG BASE	GND	Ground	Provides DC and RF ground for LNA, as well as thermal heat sink. TDY recommends multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page.

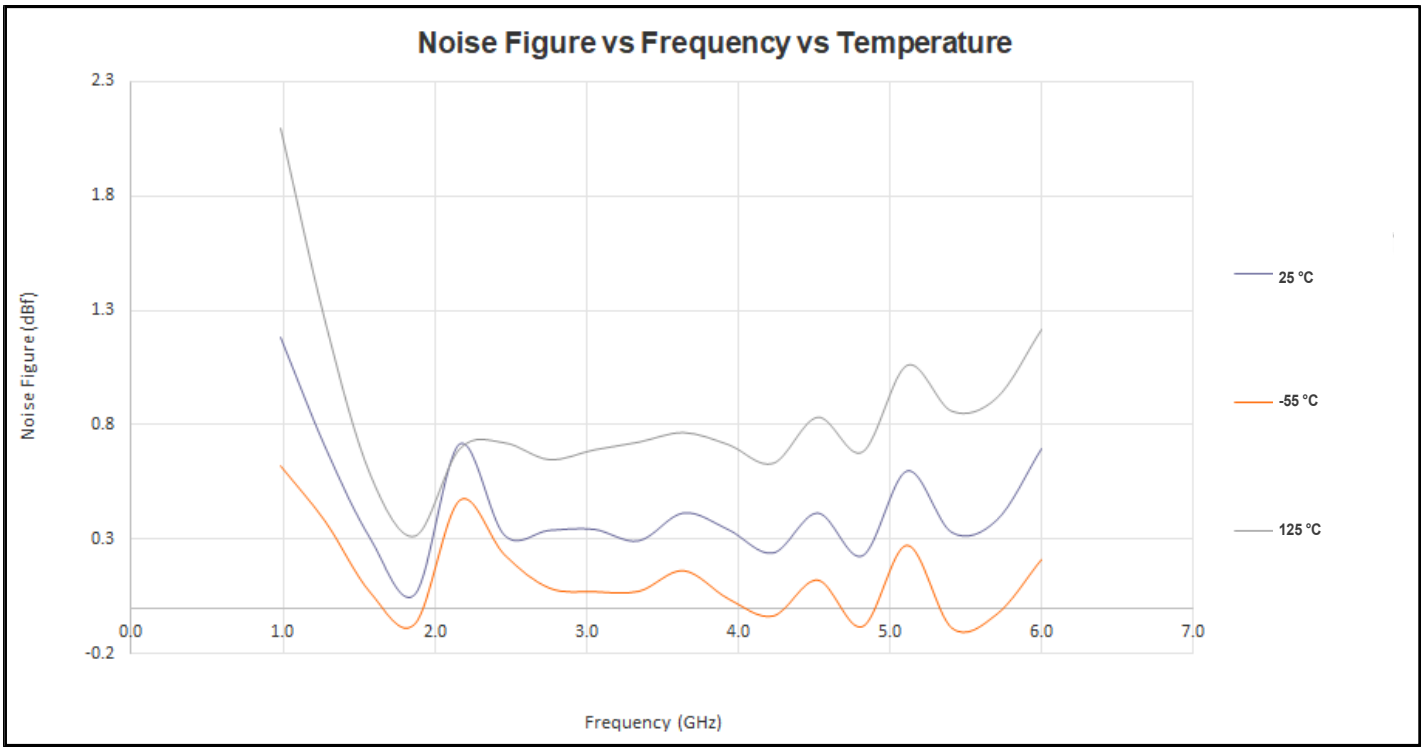
Electrical Specifications: Test conditions, unless otherwise noted: -55 °C ≤ T_A ≤ 125 °C, V_{DD} = 5 V, F_{TEST} = 2 GHz

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Test Frequency	FTEST		2.33		GHz	VDD = 5.0 V, TA = 25°C
Gain	S21	20	22.0	25	dB	
Evaluation Board Noise Figure	NF		0.37		dB	Includes Board Losses
Output 1dB Compression Power	OP1dB	15.4	19.0		dBm	
Output 3rd Order Intercept	OIP3		30		dBm	4.0 dBm POUT per tone at 2 MHz Spacing (2331.5 and 2333.5 MHz)
Switching Rise Time	TRISE		400		ns	
Switching Fall Time	TFALL		100		ns	
Supply Current	IDD	30		80	mA	VDD==VENABLE=5.0V; RBIAS=3.3k Ohm
Enable Current	IENABLE			2.0	mA	
Leakage Current	ILEAKAGE			500	uA	VDD: 5.0V; VENABLE: 0.0V
Thermal Data						
Thermal Resistance: (Infra-Red Scan)	Θjc		91.3		°C/W	On standard Evaluation Board
Channel Temperature @ +85 C Reference (Package heat sink)	TCHANNEL		100 (See note)		°C	VDD: 5.0 V; IDDQ: 70 mA; No RF; PDISS: 350 mW

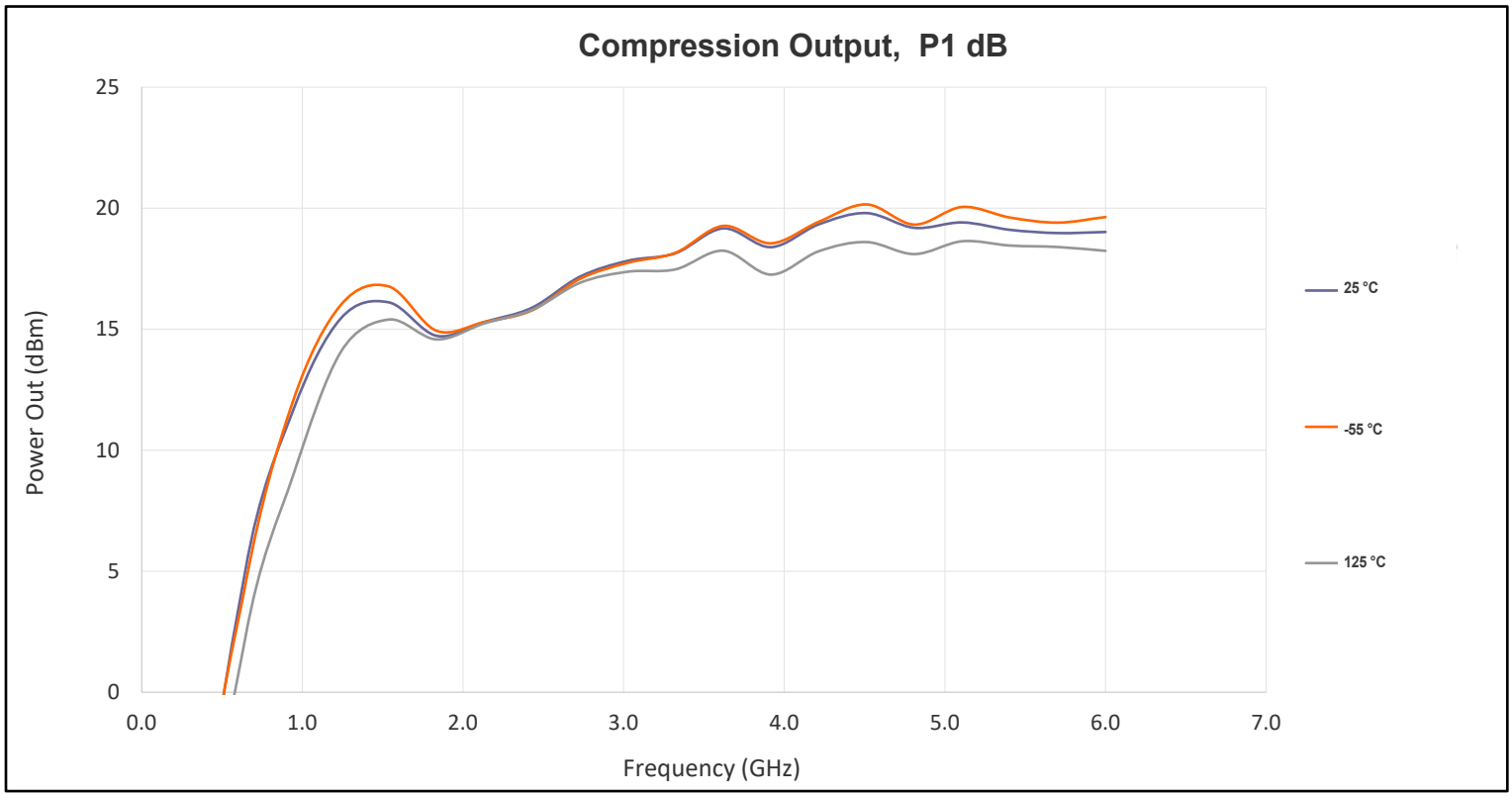
Note: MTTF >10^6 hours for $T_{CHANNEL}$ ≤ 170 degrees C.

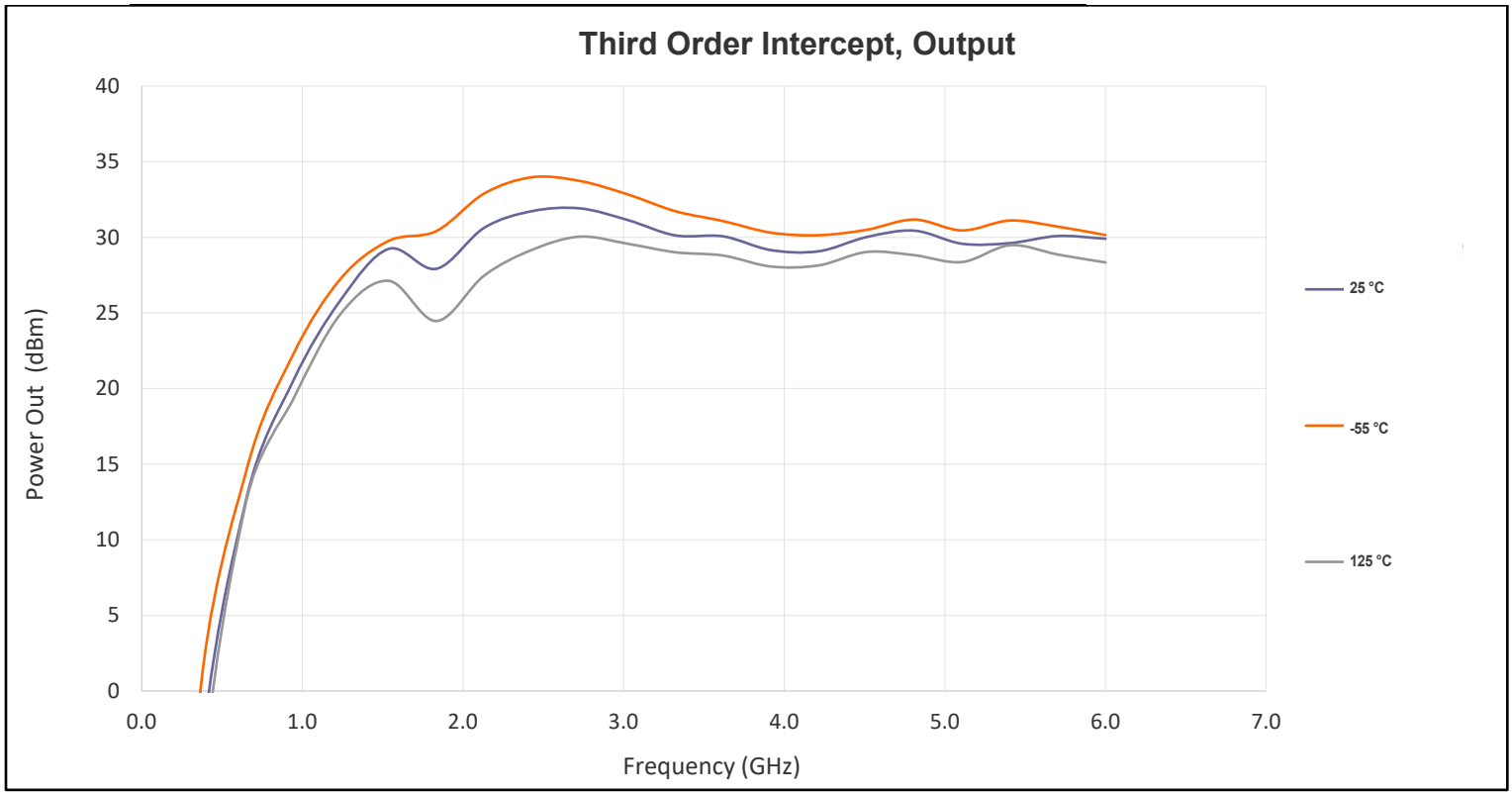
TDLNA002093 Evaluation Board Data:

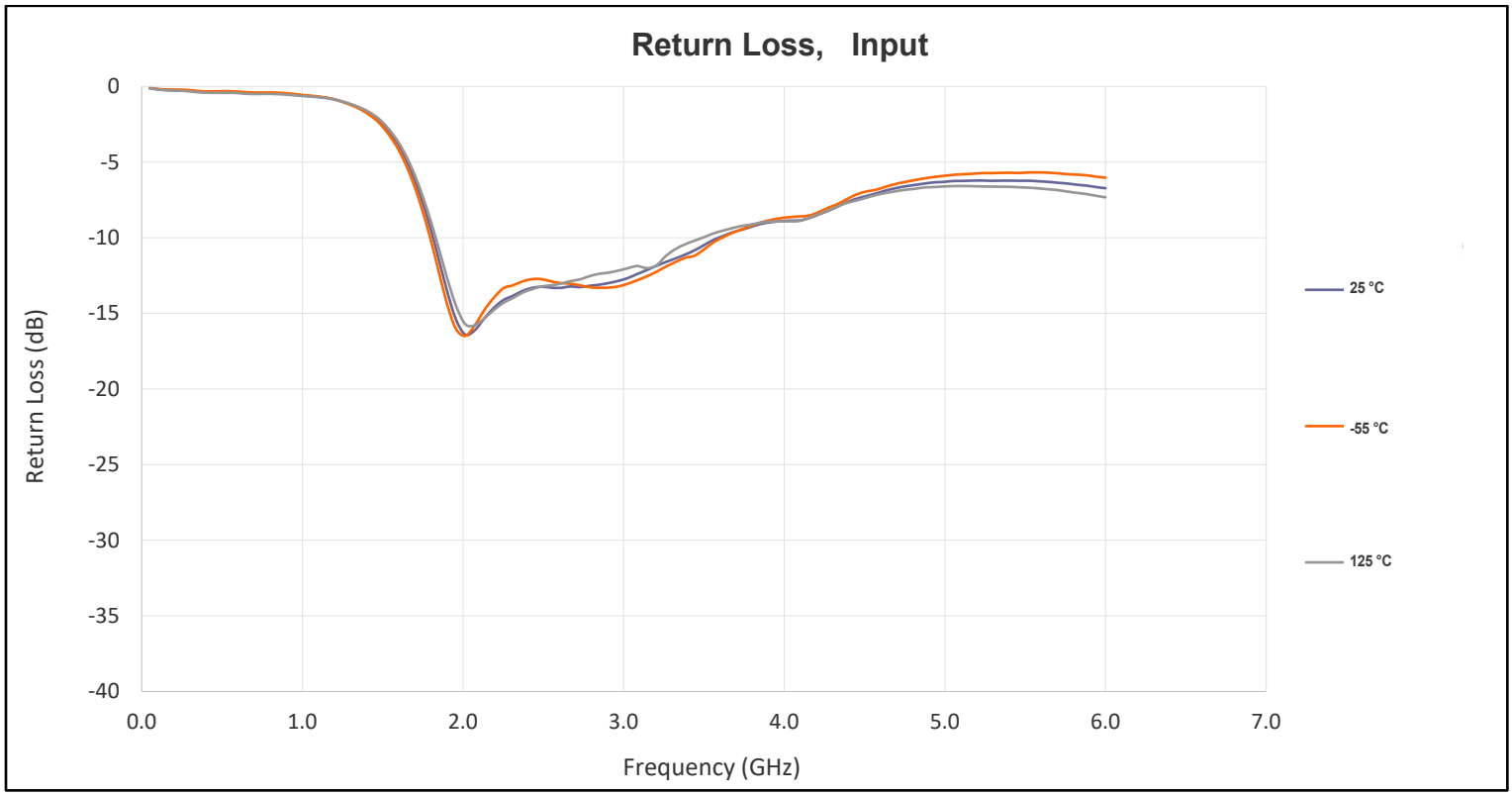


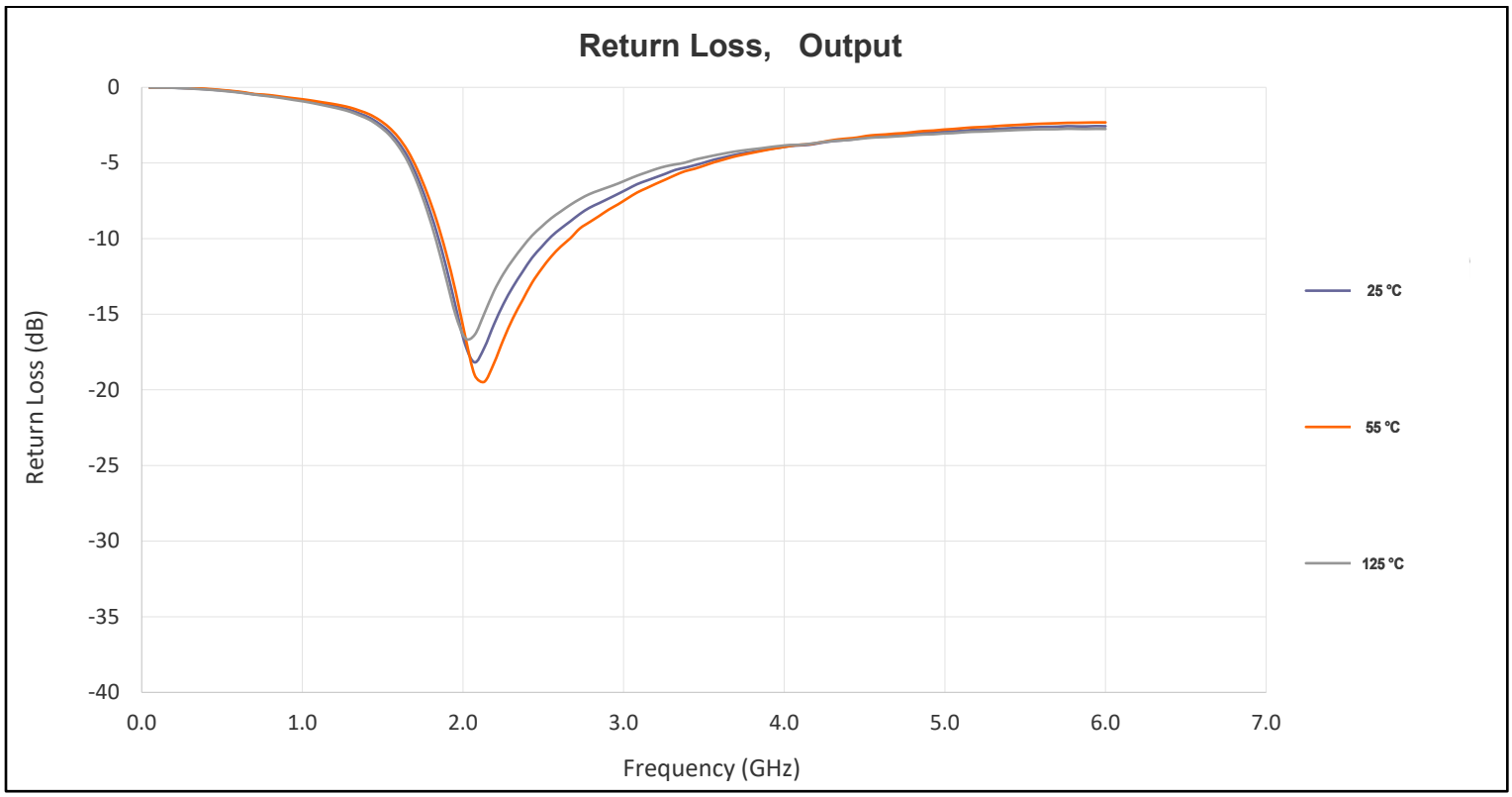


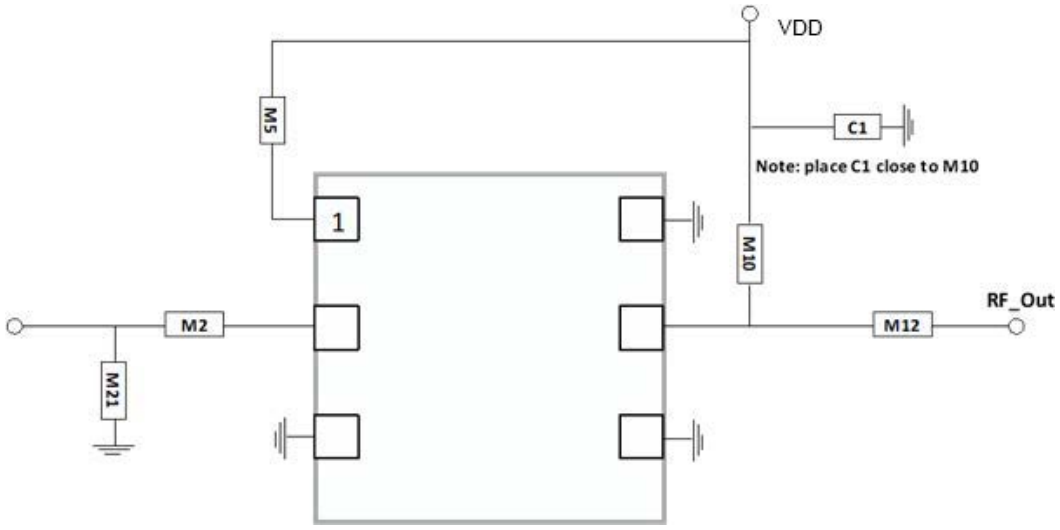
TDLNA002093 Evaluation Board Data:



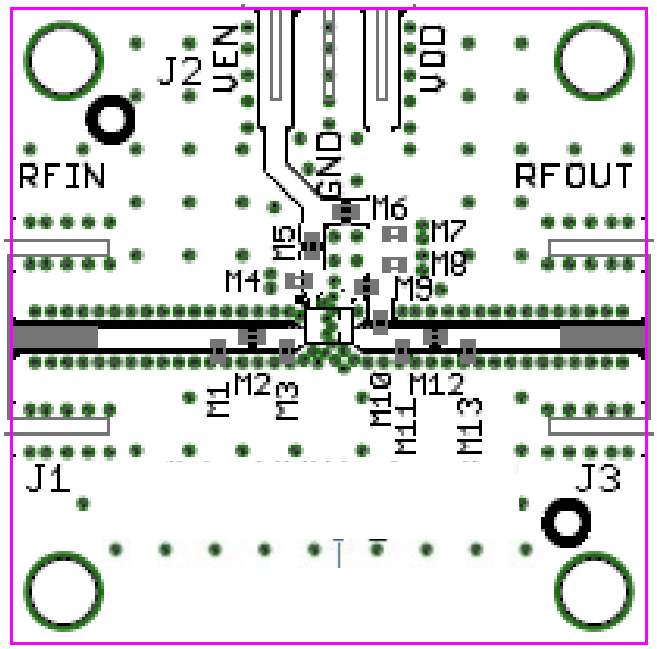








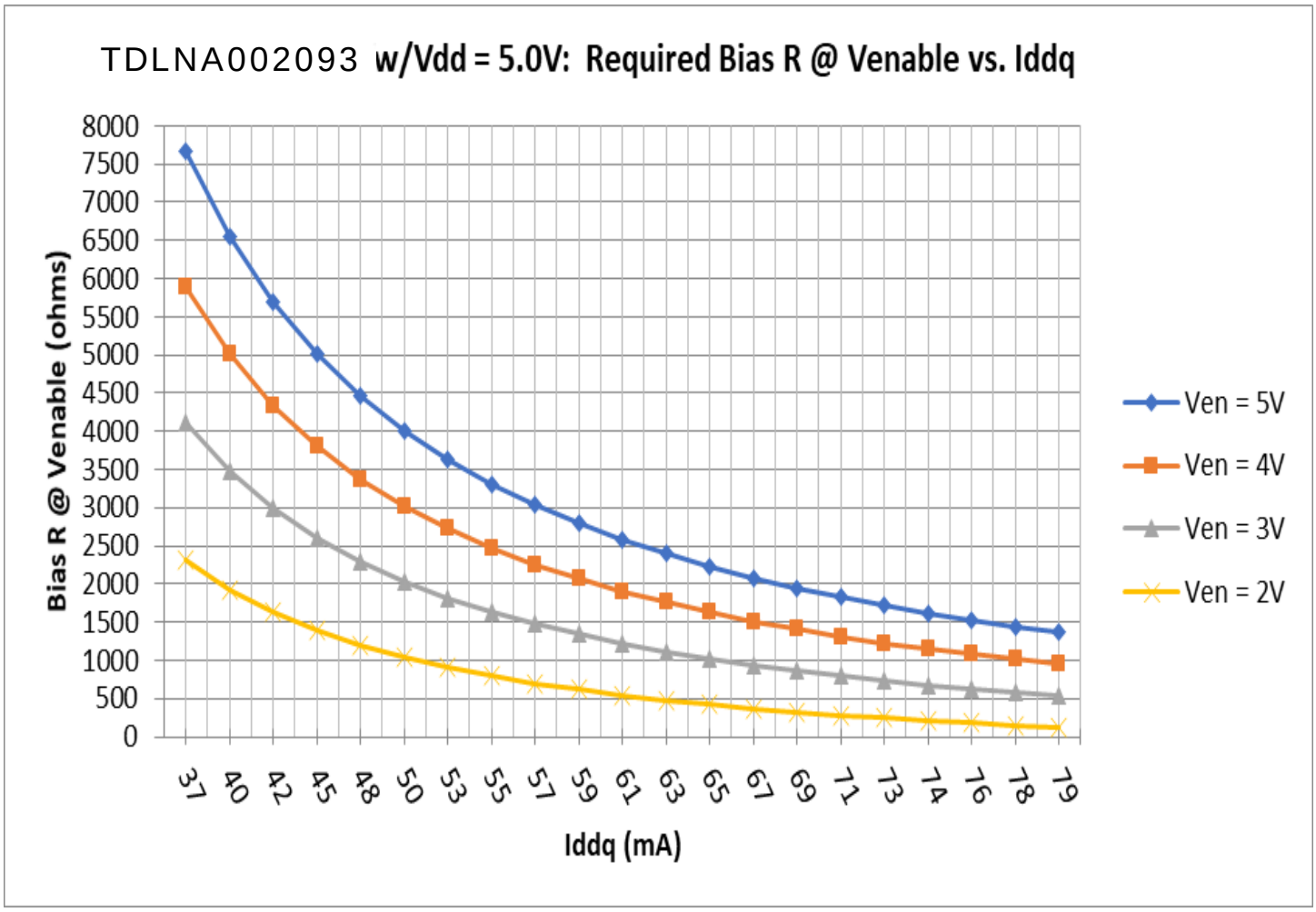
TDLNA002093 Application Schematic
(Top View)



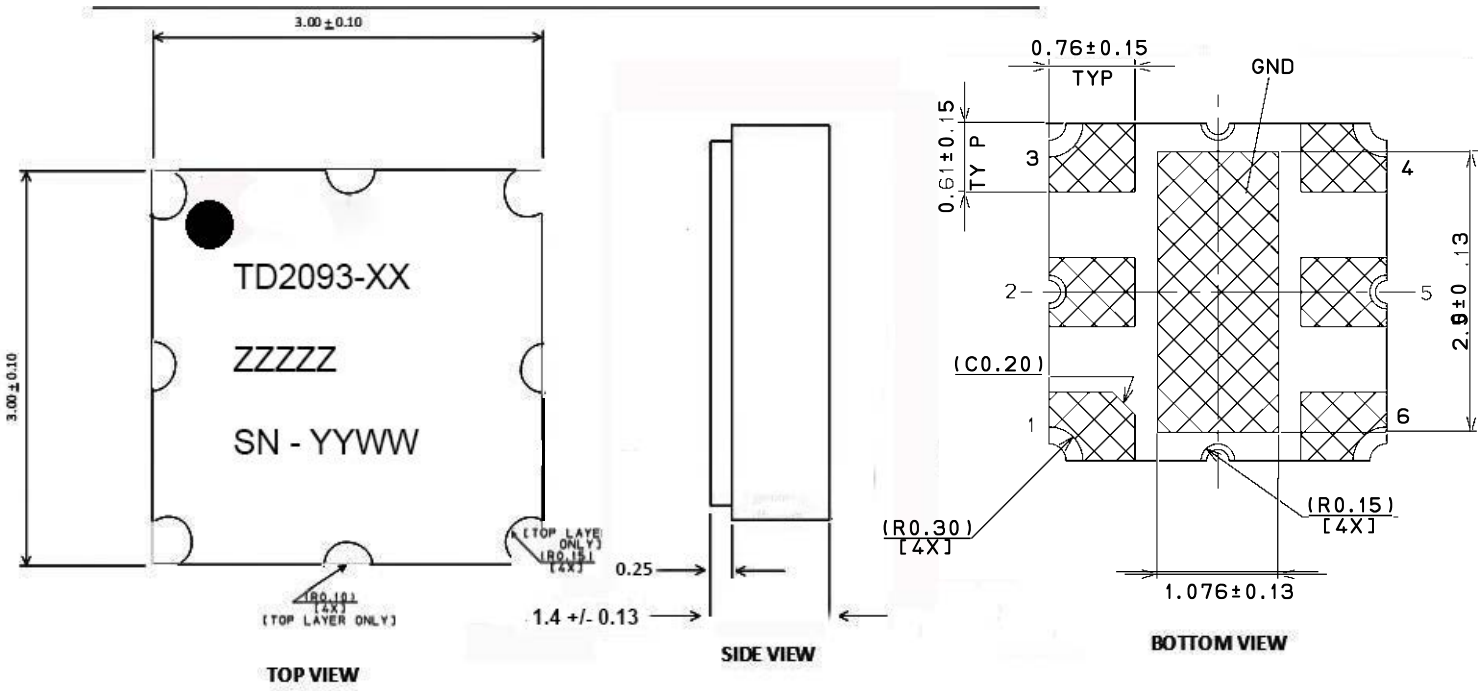
TDLNA002093 Evaluation Board
(Top View Component Side)

TDLNA002093 Standard Evaluation Board BOM: (2.3 to 2.7 GHz Tune)

Component	Type	Manufacturer	Family	Value	Package Size	Sub tu on
M1	Inductor	Coilcraft	HP	3.3 nH	0402	ok
M2	Capacitor	Murata	GJM	2.7 pF	0402	ok
M5 (See curves)	Resistor: 5%	Various	—	—	0402	ok
C1	Capacitor	Murata	GRM	0.1 uF	0402	ok
M10	Inductor	Murata	LQG	1.8 nH	0402	ok
M12	Capacitor	Murata	GJM	2.7 pF	0402	ok
Evaluation Board	GRF400X_RevC					



Mechanical Information:



Key:
Color Contrasting Dot = Pin 1
XX = 01 or 11
ZZZZZ = Lot Code
SN = Serial Number
YYWW = Date Code (year, week)

3.0 mm DFN-6 Package Dimensions

Note: All measurements in drawings are in mm.

Ordering Information

Order Code / Notes	Description	Package	Shipping Method
TDLNA002093-11	TDLNA002093 Flight Units	DFN	Trays
TDLNA002093-01 /1	TDLNA002093 Engineering Samples	DFN	Trays
TDLNA002093-00	TDLNA002093 Evaluation Board	Evaluation Kit	1/box

Note /1: The TDLNA002093-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the TDLNA002093-11 flight units. The TDLNA002093-01 device provides the same functionality and footprint as the TDLNA002093-11 device, and is intended for engineering evaluation only. They are tested at +25°C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are are not suitable for qualification, production, radiation testing or flight use. Units ship without a C of C, standard warranty, and are limited in quantity.

Document Revision History

Document	Description	Comments	Date /Document Revision
TDLNA002093 - 10/2023 Prod Spec	Product Specification data sheet	Initial Release	10/6/2023 Rev -
TDLNA002093 - 02/2024 Prod Spec	Side view updated page 11	Mechanical Info Update	02/9/2024 Rev 1
TDLNA002093 - 02/2025 Prod Spec	Ordering Information page 11	Ship Method Correction / Trays	02/10/2025 Rev 2
TDLNA002093 - 03/2025 Prod Spec	Electrical Sp[ecifications page 4	Updated Thermal Resistance	03/11/2025 Rev 3
TDLNA002093 - 08/2025 Prod Spec	Ordering Information page 11	Added Note **/1** to table	08/11/2025 Rev 4

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