SN54F543, SN74F543
OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

T-52-31

D2942, MARCH 1987—REVISED JANUARY 1989

- 3-State True Outputs
- Back-to-Back Registers for Storage
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

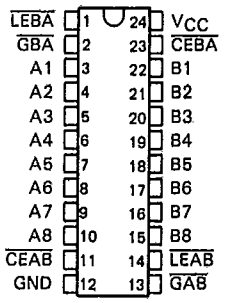
description

The 'F543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For the SN54F543 and SN74F543, respectively, the A outputs are characterized to sink 20 or 24 milliamperes while the B outputs are characterized for 48 or 64 milliamperes.

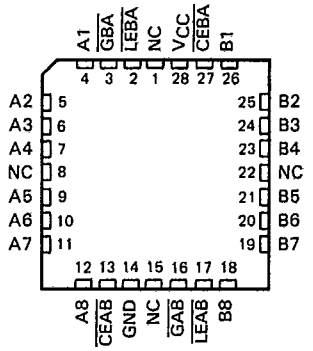
The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The SN54F543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F543 is characterized for operation from 0°C to 70°C.

SN54F543 . . . JT PACKAGE
SN74F543 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54F543 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$	A TO B†	B1 THRU B8
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

†A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡Before low-to-high transition of $\overline{LEAB}$.

2 Data Sheets

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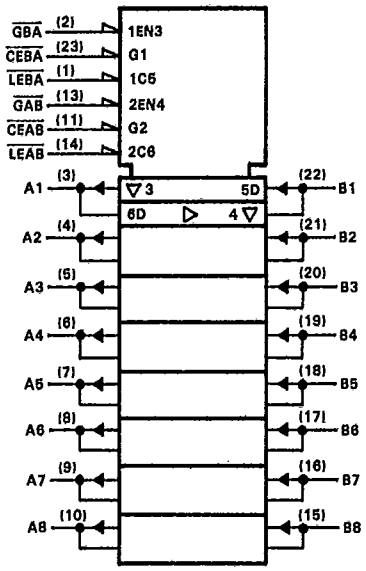
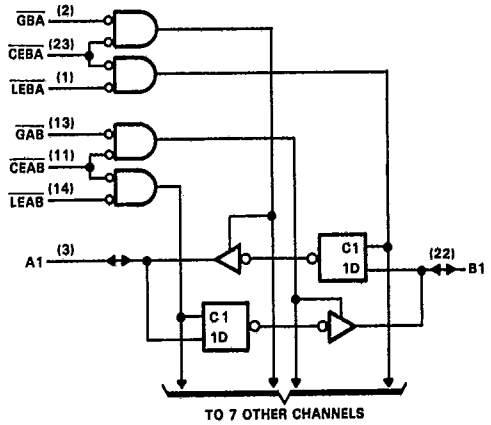
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage (excluding I/O ports)‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F543 (A1 thru A8) . . . . . 40 mA
SN54F543 (B1 thru B8) . . . . . 96 mA
SN74F543 (A1 thru A8) . . . . . 48 mA
SN74F543 (B1 thru B8) . . . . . 128 mA
Operating free-air temperature range: SN54F543 . . . . . −55°C to 125°C
SN74F543 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡The input voltage ratings may be exceeded provided the input current ratings are observed.

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recommended operating conditions

			SN54F543			SN74F543			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F543			SN74F543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	A1 thru A8	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V, I_{OH} = −1 mA to −3 mA					2.7			
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A and B		V_I = 5.5 V			1			1	
I_{IH}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A and B					70			70	
I_{IL}‡	$\overline{G}$, $\overline{LE}$, and $\overline{CE}$	V_{CC} = 5.5 V, V_I = 0.5 V				−1.2			−1.2	mA
	A and B					−0.65			−0.65	
I_{OS}§	A1 thru A8	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8			−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V			67	100		67	100	mA
I_{CCL}		V_{CC} = 5.5 V			83	125		83	125	mA
I_{CCZ}		V_{CC} = 5.5 V			83	125		83	125	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'F543		SN54F543		SN74F543		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable	High or low	3				3.5		ns
t_h	Hold time, data after latch enable	High or low	3				3.5		ns

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F543			SN54F543		SN74F543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.2	5.1	7.5			2.2	8.5	ns
t_{PHL}			2.2	4.6	6.5			2.2	7.5	
t_{PLH}	$\overline{LEBA}$	A	3.7	8.1	11			4.1	12.5	ns
t_{PHL}			3.7	8.1	11			4.1	12.5	
t_{PLH}	$\overline{LEAB}$	B	3.7	8.1	11			4.1	12.5	ns
t_{PHL}			3.7	8.1	11			4.1	12.5	
t_{PZH}	$\overline{G}$ or $\overline{CE}$	A or B	2.2	6.6	9			2.2	10	ns
t_{PZL}			3.2	7.1	10.5			3.2	12	
t_{PHZ}	$\overline{G}$ or $\overline{CE}$	A or B	1.7	5.6	8			1.7	9	ns
t_{PLZ}			1.7	5.1	7.5			1.7	8.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.

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