TDLM202402

Quasi-active PIN Diode Limiter Module - SMT

Product Specification
April 2020

Features:

- **Surface Mount S-band Limiter Module 5 mm x 8 mm x 2.5 mm**
- **Frequency Range ..... 2 to 4 GHz**
- **High Average Power Handling ..... +50 dBm (CW)**
- **High Peak Power Handling ..... +60 dBm**
- **Low Insertion Loss ..... 0.5 dB**
- **Return Loss ..... 17 dB**
- **Low Flat Leakage Power ..... 14 dBm**
- **Low Spike Energy Leakage ..... 0.5 ergs**
- **Input and output dc blocking capacitors**
- **"Always On Protection"**
  - **No external control lines or power supply required**
- **RoHS Compliant**

Description:

The TDLM202402 SMT Silicon PIN Diode Limiter Modules offers "Always On" High Power CW and Peak protection in the S-band region. This family of Limiter Modules is based on proven hybrid assembly technology utilized extensively in high-reliability, mission-critical applications. The TDLM202402 offers excellent thermal characteristics in a compact, low profile 8 mm x 5 mm x 2.5 mm package. It is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the S-band frequency range.

The TDLM202402 Limiter Modules provide outstanding passive receiver protection (Always On) which protects against High Average Power up to +50 dBm (CW), High Peak Power up to +60 dBm pulsed, maintains low flat leakage to less than 14 dBm (typical), and reduces Spike Leakage to less than 0.5 ergs (typical).

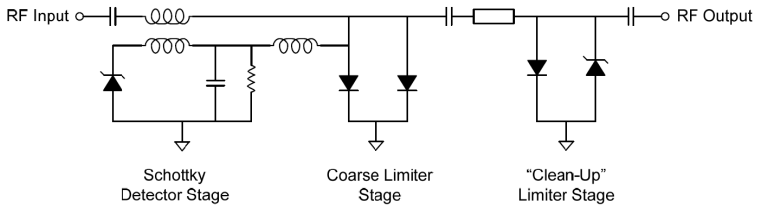
ESD and Moisture Sensitivity Rating

The TDLM202402 Limiter Module carries a Class 0 ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The proprietary design methodology minimizes the thermal resistance from the PIN Diode junction-to-base plate (RTHJ-A). The two-stage limiter design employs a two-stage detector circuit which enables ultra-fast turn on of the High Power PIN Diodes. This circuit topology, coupled with the thermal characteristic of the substrate design, enables the Limiter Module to reliably handle High Input RF Power up to +50 dBm (CW) and RF Peak Power levels up to +60 dBm (25 µsec pulse width @ 5.0% duty cycle) with base plate temperature held at +85°C.The TDLM202402-based substrate has been designed to offer superior, long-term reliability in customers' applications by utilizing ultra-thin Au plating to combat Au embrittlement concerns.

TDLM202402QF: Limiter Module -Input & Output RF Blocking Capacitors



Absolute Maximum Ratings

@ Z_o=50 Ω, T_A= +25ºC as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65ºC to 125ºC
Storage Temperature		-65ºC to 150ºC
Junction Temperature		175ºC
Assembly Temperature	T = 30 seconds	260ºC
RF Peak Incident Power	T_{CASE} = 85ºC, source and load VSWR < 1.2:1, RF Pulse width = 25 µsec, duty cycle = 5%, derated linearly to 0 W at T_{CASE} = 150ºC (note 1)	60 dBm
RF CW Incident Power	T_{CASE} = 85ºC, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE} = 150ºC (note 1)	50 dBm
RF Input & Output dc Block Capacitor Voltage Breakdown		100 V dc

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

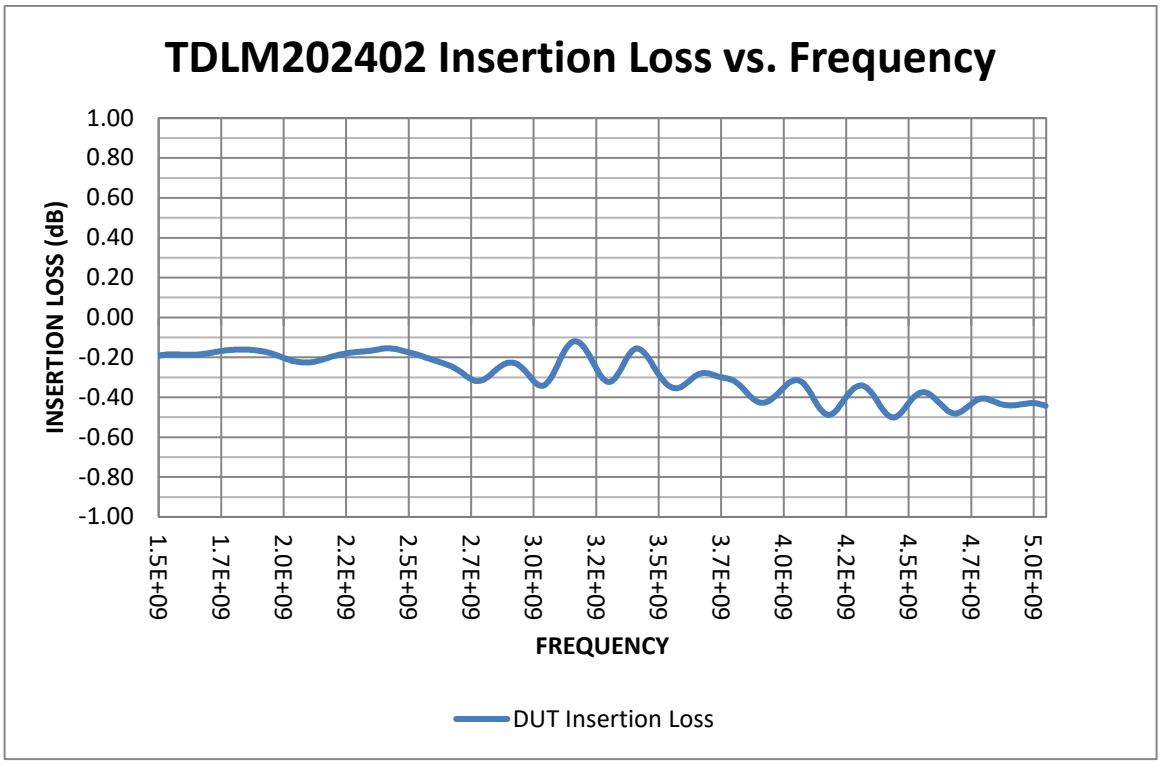
TDLM202402 Electrical Specifications

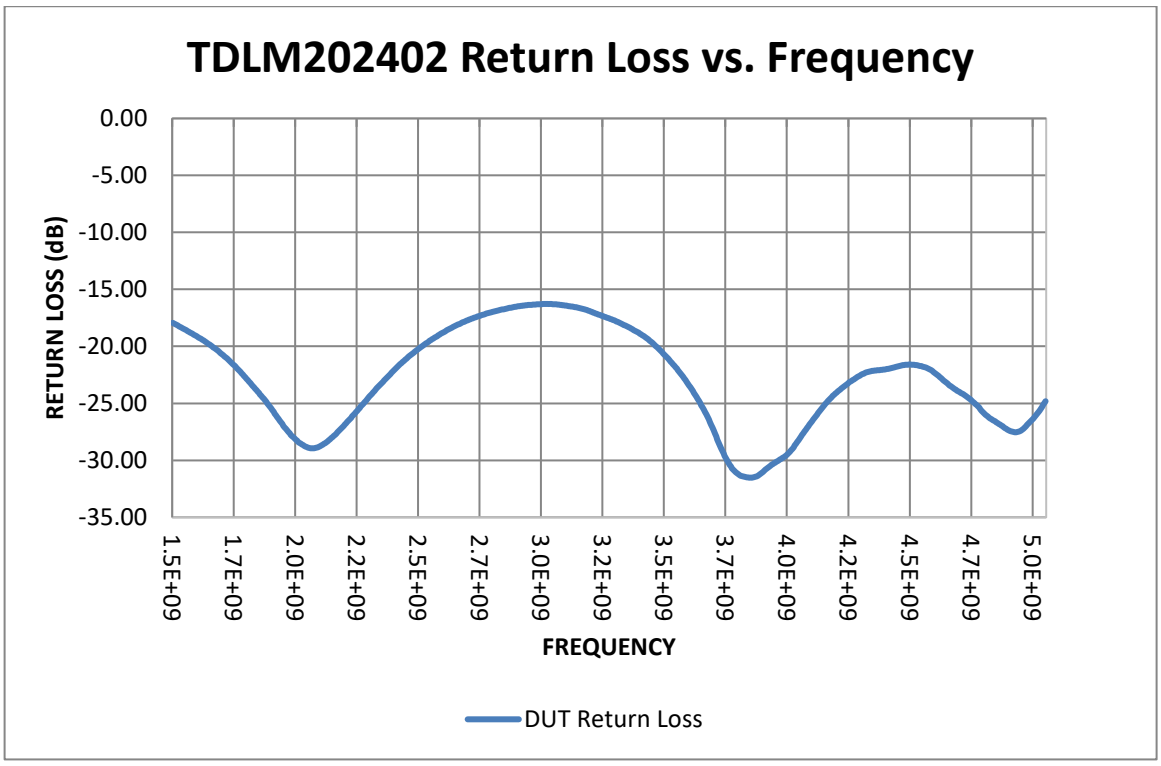
@ Z_o=50 Ω, TA= +25°C as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	2 GHz ≤ F ≤ 4 GHz	2		4	GHz
Insertion Loss	IL	2 GHz ≤ F ≤ 4 GHz, P_{in} = -10 dBm		0.5	0.7	dB
Insertion Loss Rate of Change vs. Operating Temperature	ΔIL	2 GHz ≤ F ≤ 4 GHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	2 GHz ≤ F ≤ 4 GHz, Pin = -10 dBm	16	17		dB
Input 1 dB Compression Point	IP_{1dB}	2 GHz ≤ F ≤ 4 GHz	0	8	11	dBm
2nd Harmonic	$2F_o$	P_{in} = -10 dBm, F_o = 3.0 GHz		-40	-30	dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 25 µsec, duty cycle = 5%, t_{rise} ≤ 3µs, t_{fall} ≤ 3µsec			60	dBm
CW Incident Power	$P_{inc(CW)}$	2 GHz ≤ F ≤ 4 GHz			50	dBm
Flat Leakage	FL	P_{in} = 60 dBm, RF Pulse width = 25 µs, duty cycle = 5%, t_{rise}≤ 3 µs, t_{fall}≤ 3 µs		14	15	dBm
Spike Leakage	SL	Pin = 60 dBm, RF Pulse width = 25 µs, duty cycle = 5%		0.5	0.7	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = 60 dBm peak, RF PW = 25 µs, duty cycle = 5%, trise ≤ 3µs, t_{fall} ≤ 3µsec		1	2	µsec

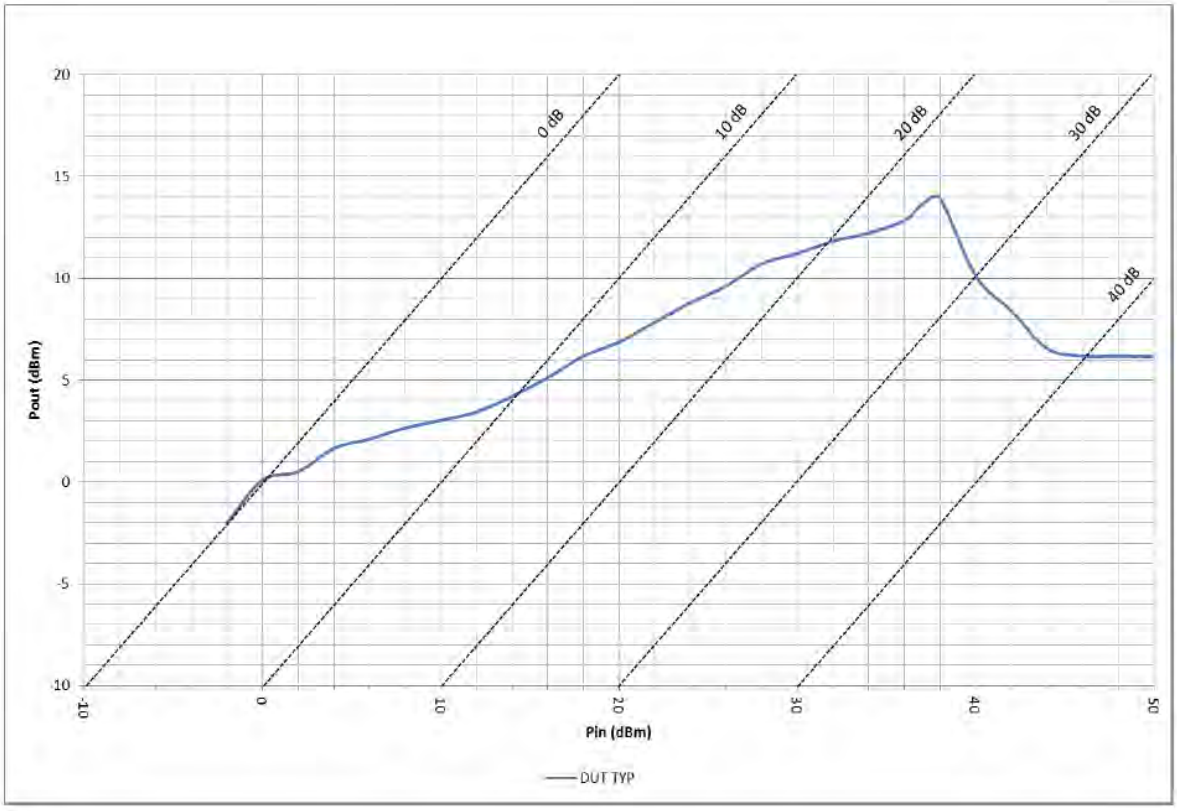
TDLM202402 Typical Performance

Z_o = 50 Ω, T_{CASE} = 25°C, PIN = -20 dBm as measured on the Ground Plane of the device.





TDLM202402: Pin vs. Pout

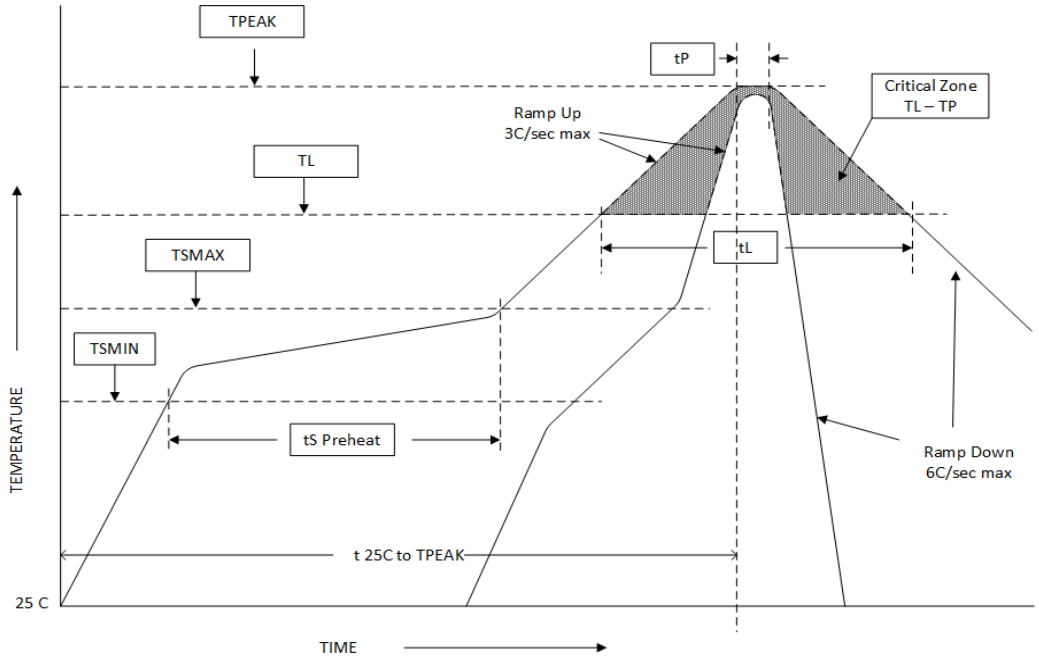


Assembly Instructions

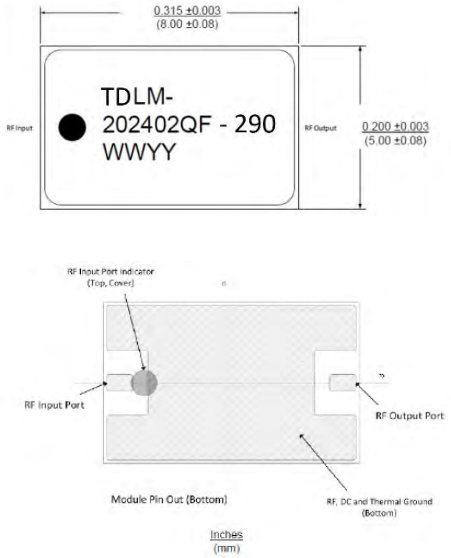
The TDLM202402 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 180 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



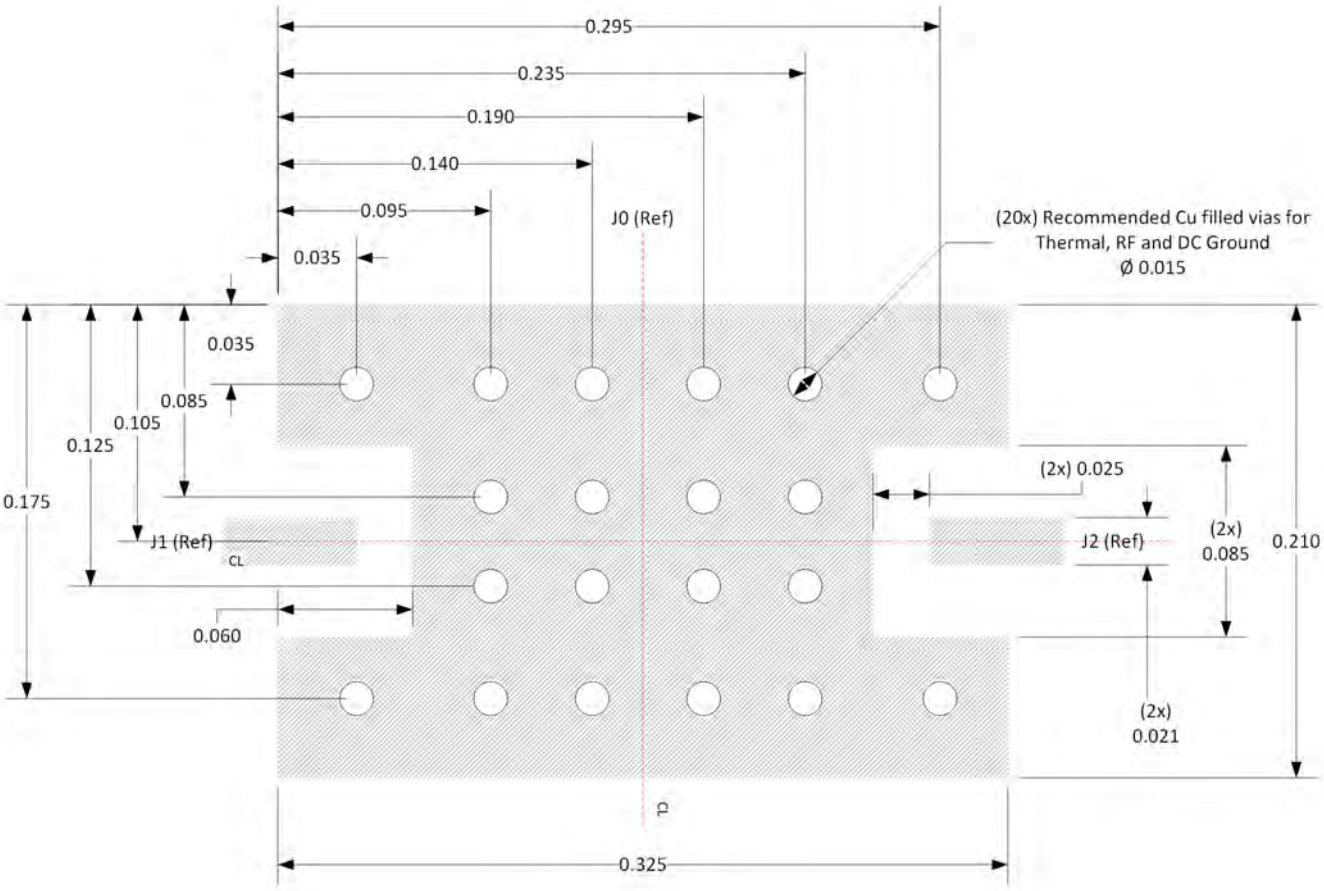
TDLM202402 Limiter Module Package Outline Drawing



Notes:

1) Metalized area on backside is the RF, dc and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).
3) Unit = mils

Recommended RF Circuit Solder Footprint for the TDLM202402



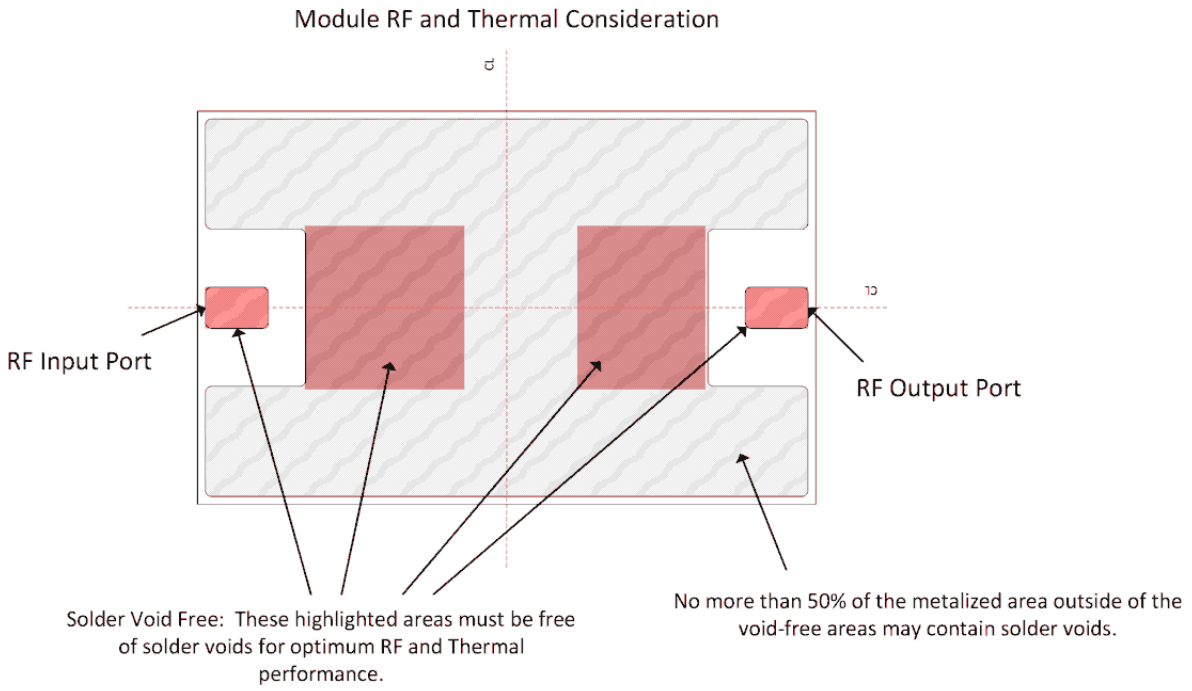
Notes:

1) Recommended PCB material is Rogers 4350B, 10 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
2) Hatched area is RF, dc and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.
3) Unit = mils

Thermal Design Considerations:

The design of the TDLM202402 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than +85°C.

There must be a minimal thermal and electrical resistance between the limiter module and ground. Adequate thermal management is required to maintain a Tjunction at less than +175°C and thereby avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.



Part Number Ordering Detail:

Part Number	Description	Packaging
TDLM202402QF-290	S-band Limiter with Input & Output dc Blocking Caps	Tube

Document Revision History:

Document No.	Description	Date
TDLM202402_4_2020_Rev -	Initial Release	4/3/2020
TDLM202402_4_2020_Rev 1	Updated dc bocking bullet on page #1, Removed T&R ordering option page # 9	4/7/2020

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