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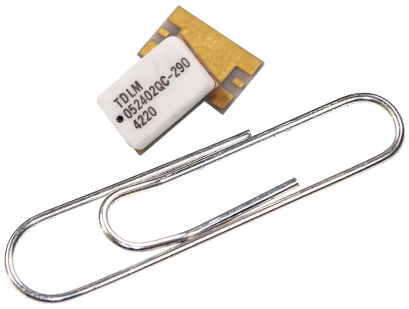
Product Specification

March 2021

TDLM052402QC-290

Quasi Active 2 kW PIN Diode Limiter Module - SMT

Features:



- Frequency Range: 500 MHz to 4.0 GHz
- High Average Power Handling: +53 dBm
- High Peak Power Handling: +63 dBm
- Low Insertion Loss: +0.9 dB
- Return Loss: 13 dB
- Low Flat Leakage Power: 17 dBm
- Low Spike Energy Leakage: 0.5 ergs
- Surface Mount Limiter Module : 8 mm x 5 mm x 2.5 mm
- dc Blocking Capacitors
- "Always On Protection"
  - No external control lines or power supply required
- RoHS Compliant

Description:

The TDLM052402QC-290 SMT Silicon PIN Diode Limiter Modules offers "Always On" High Power CW and Peak protection in the 500 MHz to 4.0 GHz frequency region. This Limiter Module is based on proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The TDLM052402QC-290 offers excellent thermal characteristics in a compact, low profile 8 mm x 5 mm x 2.5 mm package. It is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering very low Flat Leakage under high power conditions thereby offering excellent receiver protection across the 500 MHz to 4.0 GHz frequency range.

The TDLM052402QC-290 Limiter Module provide outstanding passive receiver protection (Always on) which protects against High Average Power up to +53 dBm (CW), High Peak Power up to +63 dBm pulsed mode, while maintaining low Flat Leakage to less than 17 dBm (typ), and reduces Spike Leakage to less than 0.5 ergs (typ).

ESD and Moisture Sensitivity Rating

The TDLM052402QC-290 Limiter Module carries a Class 0 ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The proprietary design methodology minimizes the thermal resistance from the PIN Diode junction to base plate (RTHJ-A). The two stage limiter design employs a two stage detector circuit which enables ultra-fast turn on of the High Power PIN Diodes. This circuit topology coupled with the thermal characteristic of the substrate design enables the Limiter Module to reliably handling High Input RF Power up to +53 dBm(CW) and RF Peak Power levels up to +63 dBm (25 µsec pulse width @ 5.0% duty cycle) with base plate temperature at +85°C. The TDLM052402QC-290 based substrate has been design to offer superior long term reliability in customers' applications by utilizing ultra-thin, Au plating to combat Au embrittlement concerns.

Absolute Maximum Ratings

@ Z_o = 50 Ω, T_A = +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}= +85°C, source and load VSWR < 1.2:1, RF Pulse width = 25 µsec, duty cycle = 5%, derated linearly to 0 W at T_{CASE}=150°C (note 1)	63 dBm
RF CW Incident Power	T_{CASE}= +85°C, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE}=150°C (note 1)	53 dBm
RF Input & Output dc Block Capacitor Voltage Breakdown		100 V dc

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

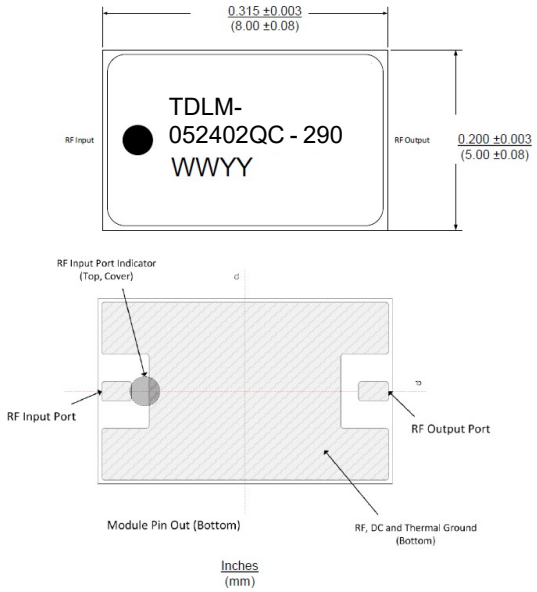
TDLM052402QC-290 Electrical Specifications

@ Z_o = 50 Ω, TA = +25ºC as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	500 MHz ≤ F ≤ 4 GHz	0.05		4.0	GHz
Insertion Loss	IL	500 MHz ≤ F ≤ 4 GHz, P_{in}= -20 dBm		0.7	0.9	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	500 MHz ≤ F ≤ 4 GHz, Pin ≤ -20 dBm		0.005		dB/ºC
Return Loss	RL	500 MHz ≤ F ≤ 4 GHz, Pin= -20 dBm	13			dB
Input 1 dB Compression Point	IP_{1dB}	500 MHz ≤ F ≤ 4 GHz	7	10		dBm
2nd Harmonic	$2F_o$	P_{in}= -10 dBm, F_o= 2.0 GHz		-40	-35	dBc
Peak Incident Power /1	$P_{inc\ (PK)}$	RF Pulse = 25 µsec, duty cycle = 5%, t_{rise} ≤ 3µs, t_{fall} ≤ 3µsec			63	dBm
CW Incident Power /1	$P_{inc(CW)}$	500 MHz ≤ F ≤ 4 GHz			53	dBm
Flat Leakage /1	FL	P_{in} = +63 dBm, RF Pulse Width = 25 µs, Duty Cycle = 5%, t_{rise}≤ 3 µs, t_{fall}≤ 3 µs			17	dBm
Spike Leakage /1	SL	Pin = +63 dBm, RF Pulse Width = 25 µs, Duty Cycle = 5%			0.5	erg
Recovery Time /1	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = +63 dBm peak, RF PW = 25 µs, Duty Cycle = 5%, trise ≤ 3µs, t_{fall} ≤ 3µsec			1.5	µsec

Note /1: Guaranteed by characterization.

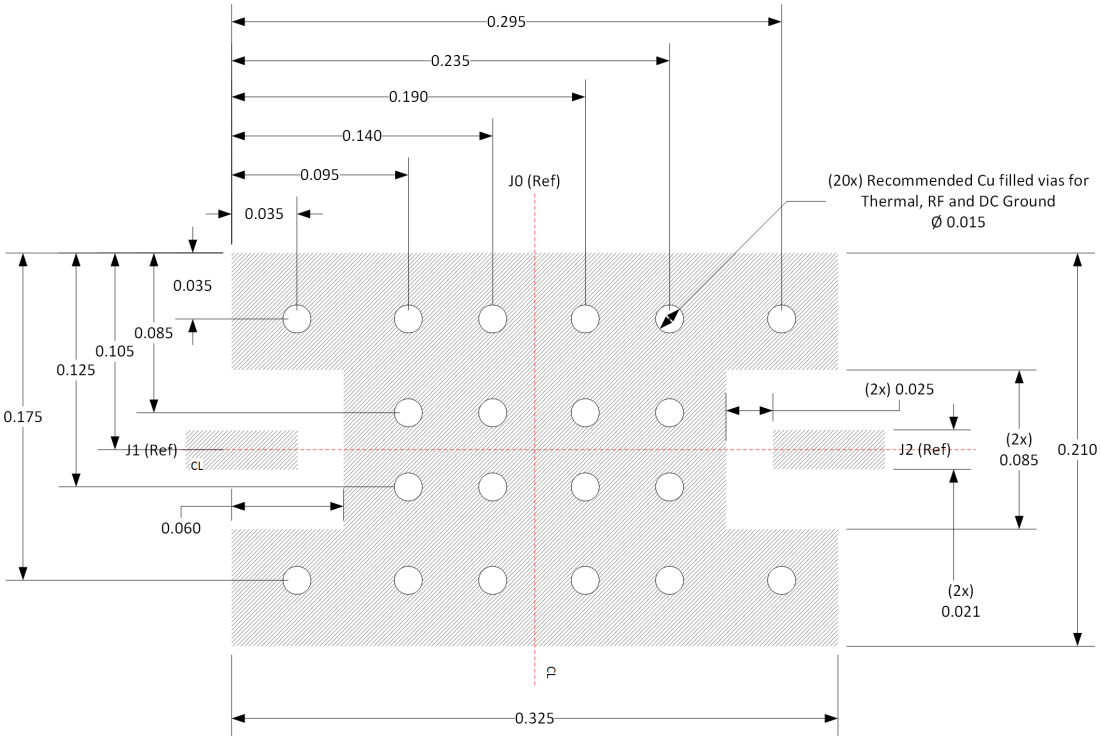
TDLM052402QC-290 Limiter Module Package Outline Drawing



Notes:

1) Metalized area on backside is the RF, dc and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).
3) Unit = mils

Recommended RF Circuit Solder Footprint for the TDLM052402QC-290



Document Categories

Advance Information

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Product Specification

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Sales Contact

For additional information, contact us via email: [redacted] www.tdehirel.com

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