LM139/LM139A, LM339

Single Supply Quad Comparators

Features

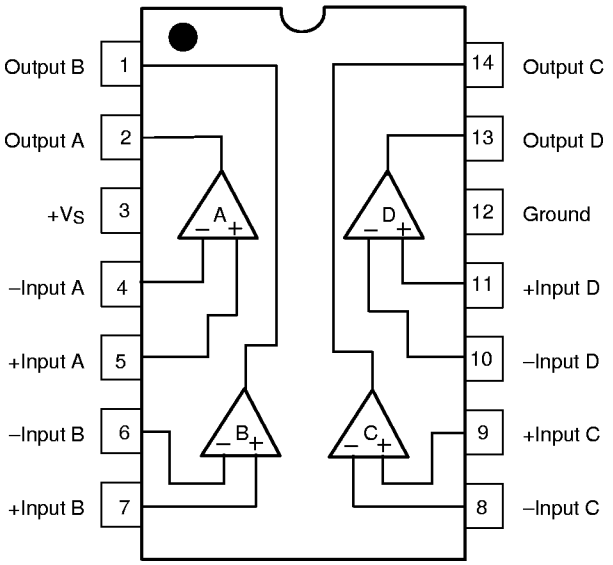
- Input common mode voltage range includes ground
- Wide single supply voltage range—2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8 mA) independent of supply voltage

Description

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two stage common-emitter output circuit provides gain and output sink capacity of 3.2 mA at an output level of 400 mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1 μs, but demanding excellent op amp input parameters to offset voltage, current and bias current, to ensure accurate comparison with a reference voltage.

Pin Assignments



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit.
Supply Voltage	-8	+36 or +8	V
Differential Input Voltage		36	V
Input Voltage Range[2]	-0.3	+36	V
Output Short Circuit to Ground[1]	Continuous		
Input Current (V_{IN} < -0.3V)[(2)]		50	mA
Operating Temperature Range			
LM139	-55	+125	°C
LM339	0	+70	°C
Storage Temperature Range	-65	150	°C
Lead Soldering Temperature			
SOIC, 10 seconds		+260	°C
DIP, 60 seconds		+300	°C

Notes:

1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of +Vs.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and nominal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.

Thermal Characteristics

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Maximum P_D T_A <50°C	300 mW	468 mW	1042mW
Thermal Resistance, θ_{JC}	—	—	60°C/W
Thermal Resistance, θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.33 mW/°C

Electrical Characteristics

V_S = +5V, see Note 1.

Parameters	Test Conditions	LM139A			Unit
		Min.	Typ.	Max.	
Input Offset Voltage	T_A = +25°C[2]		±1.0	±2.0	mV
Input Bias Current	Output In Linear Range T_A = +25°C[3], V_{CM} = 0V		25	100	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25	nA
Input Voltage Range	T_A = +25°C[4], V_S = 30V			$+V_S$–1.5	V
Supply Current	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5	mA
Large Signal Voltage Gain	R_L = ∞, $+V_S$ = 30V, R_L ≥ 15 KΩ, $+V_S$ = +5V (to support large V_{OUT} swing) T_A = +25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 KΩ,T_A = +25°C		300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 KΩ, T_A = +25°C[5]		1.3		µs
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0, V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		mA
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1		µA
Input Offset Voltage[2]				±4.0	mV
Input Offset Current	V_{CM} = 0V			±100	nA
Input Bias Current	V_{CM} = 0V			300	nA
Input Voltage Range	$+V_S$ = 30V	0		$+V_S$–2.0	V
Saturation Voltage	V_{IN-} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 30V			1.0	µA
Differential Input Voltage[7]	V_{IN+} ≥ 0V, (or -V_S, if used)[6]			36	V

Notes:

1. These specifications apply for $+V_S$ = 5V and -55°C ≤ T_A ≤ +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C ≤ T_A ≤ +70°C.
2. At output switch points V_{OUT} = 1.4V, R_S = 0Ω with $+V_S$ from 5V to 30V; and over the full input common mode range (V_{OUT} to $+V_S$–1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$–1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
7. Guaranteed by design.

Electrical Characteristics

V_S = +5V, see Note 1.

Parameters	Test Conditions	LM139			LM339			Units
		Mln	Typ	Max	Mln	Typ	Max	
Input Offset Voltage	T_A = +25°C[2]		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range T_A = +25°C[3], V_{CM} = 0V		25	100		25	250	nA
Input Offset Current	T_A = +25°C, V_{CM} = 0V		±3.0	±25		±5.0	±50	nA
Input Voltage Range	T_A = +25°C[4], +V_S = 30V	0		+V_S –1.5	0		+V_S –1.5	V
Supply Cunent	R_L = ∞ on all comparators, T_A = +25°C		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	R_L= ∞ +V_S = 30V, R_L ≥ 15 KΩ, +V_S = +5V (to support large V_{OUT} swing), T_A = +25°C	25	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1 KΩ, T_A = +25°C		300			300		ns
Response Time	V_{RL} = 5V, R_L = 5.1 KΩ T_A = +25°C[5]		1.3			1.3		µS
Output Sink Current	V_{IN-} ≥ 1V, V_{IN+} = 0, V_{OUT} ≤ 1.5V, T_A = +25°C	6.0	16		6.0	16		mA
Output Voltage, V_{OL}	V_{IN} ≥ 1V, V_{IN+} = 0, I_{SINK} ≤ 4 mA, T_A = +25°C		250	400		250	400	mV
Output Leakage Current	V_{IN+} ≥ 1V, V_{IN-} = 0, V_{OUT} = 5V, T_A = +25°C		0.1			0.1		µA
Input Offset Voltage[2]				±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	V_{CM} = 0V			300			400	nA
Input Voltage Range	V_{CM} = 30V	0		+V_S –2.0	0		+V_S –2.0	V
Output Voltage V_{OL}	$V_{IN–}$ ≥ 1V, V_{IN+} = 0 I_{SINK} ≤ 4 mA			700			700	mV
Output Leakage Cunent	V_{IN+} ≥ 1V, $V_{IN–}$ = 0 V_{OUT} = 30V			1.0			1.0	µA
Differential Input Voltage[7]	V_{IN+} ≥ 0V (or -V_S, if used)[6]			36			36	V

Notes:

1. These specifications apply for +V_S = 5V and -55°C ≤ T_A ≤ +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C ≤ TA ≤ +70°C.
2. At output switch points V_{OUT} = 1.4V, R_S = 0Ω with +V_S from 5V to 30V; and over the full input common mode range (V_{OUT} to +V_S–1.5V).
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is +V_S–1.5V, but either or both inputs can go to +30V without damage.
5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
7. Guaranteed by design.

Typical Performance Characteristics

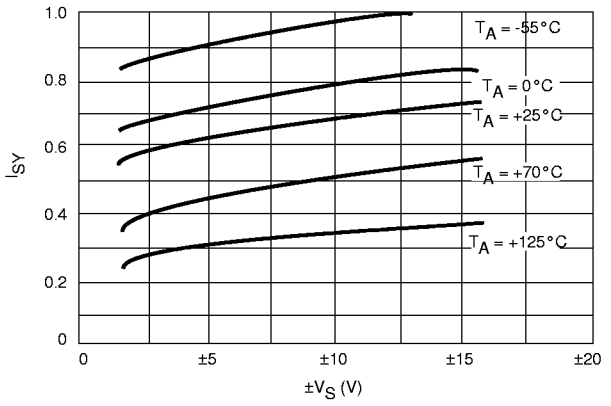


Figure 1. Supply Current vs. Supply Voltage

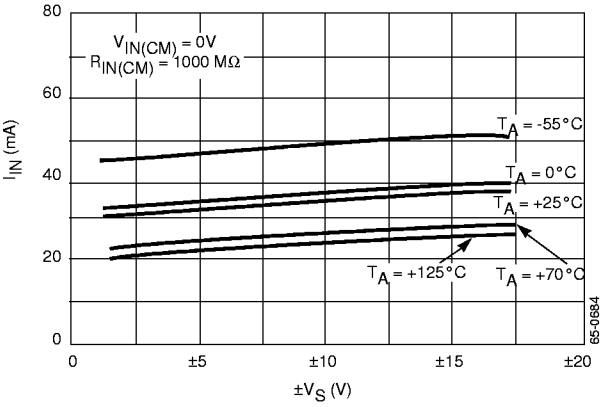


Figure 2. Input Current vs. Supply Voltage

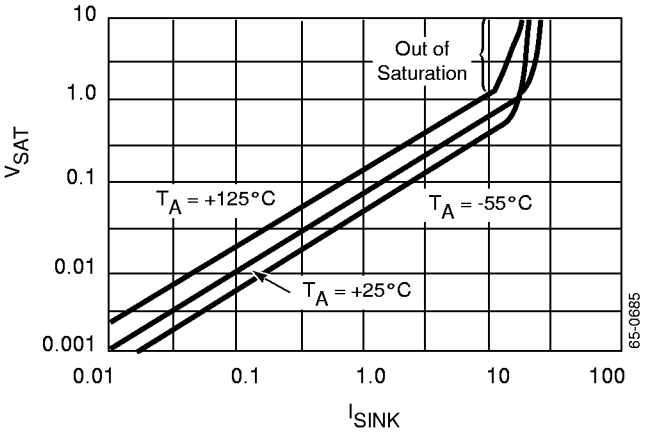


Figure 3. Output Saturation Voltage vs. Sink Current

Typical Performance Characteristics (continued)

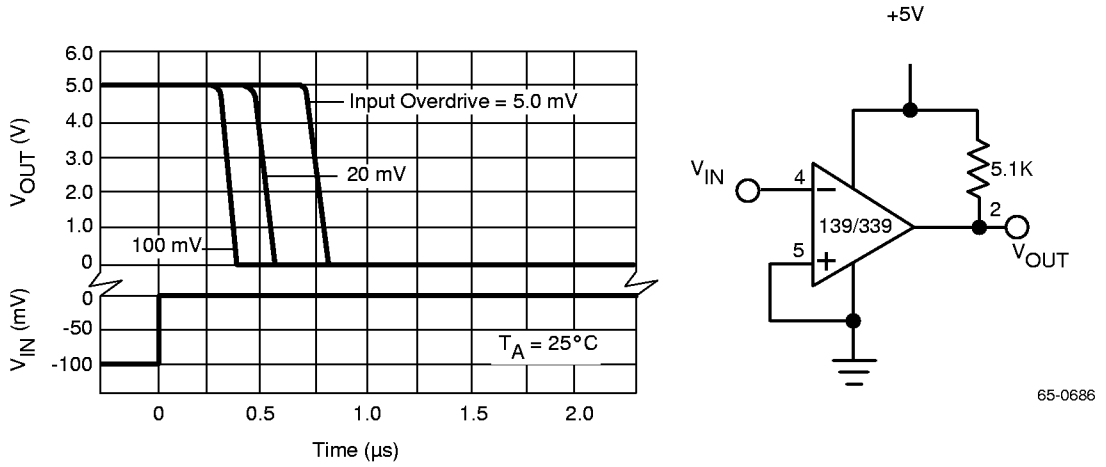


Figure 4. Input Overdriver Repsonse Time

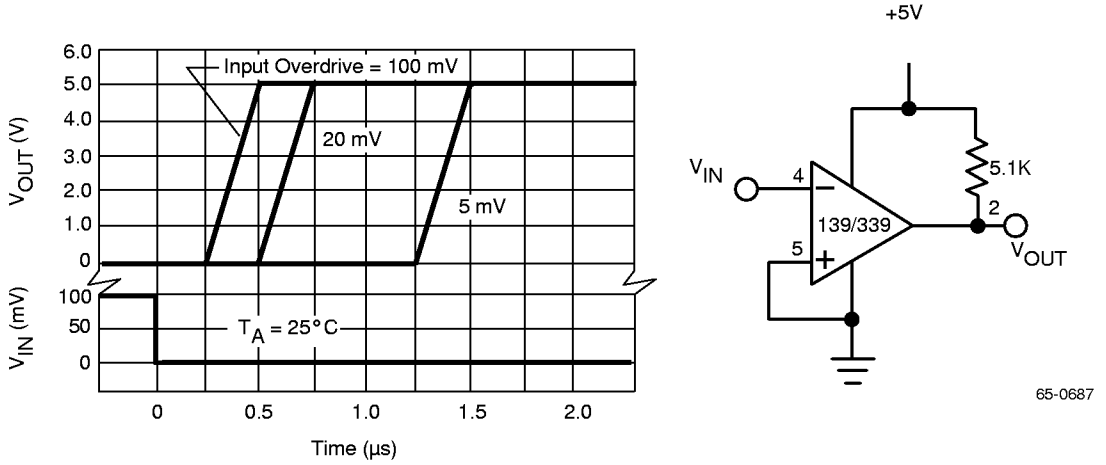


Figure 5. Input Overdrive Response Time

Applications

Single Supply (+V_S = +15V).

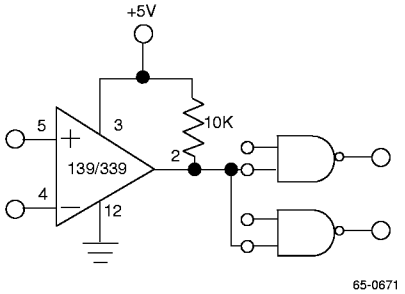


Figure 6. Driving TTL

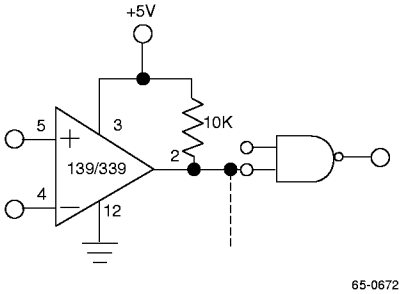


Figure 7. Driving CMOS

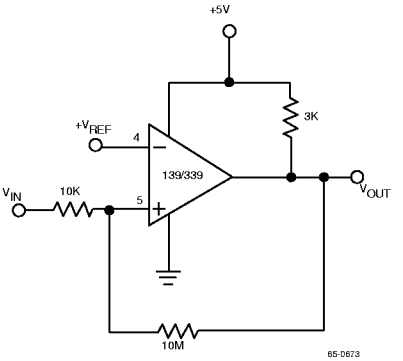


Figure 8. Comparator with Hysteresis

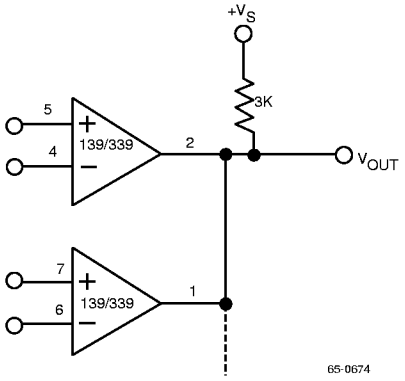


Figure 9. ORing the Output

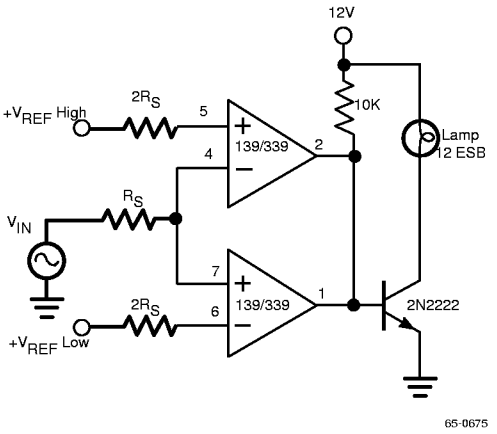


Figure 10. Limit Comparator

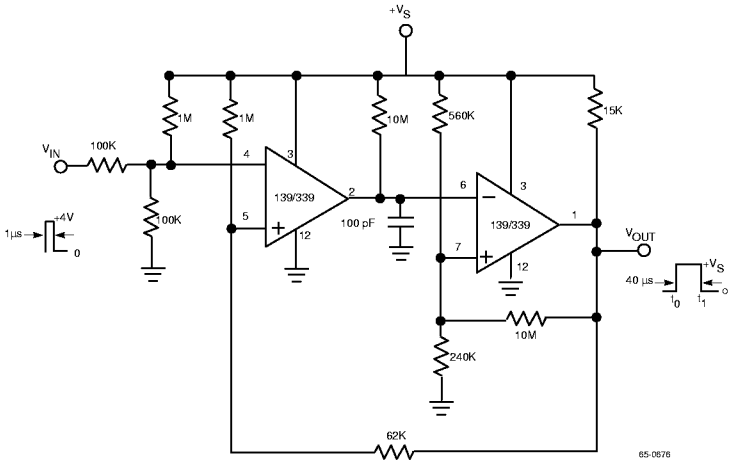


Figure 11. One-Shot Multivibrator with Input Lock Out

Applications (continued)

Single Supply (+V_S = +15V).

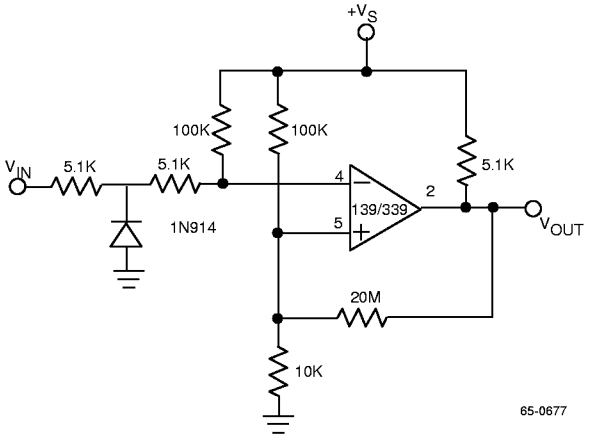


Figure 12. Zero Crossing Detector (Single Power Supply)

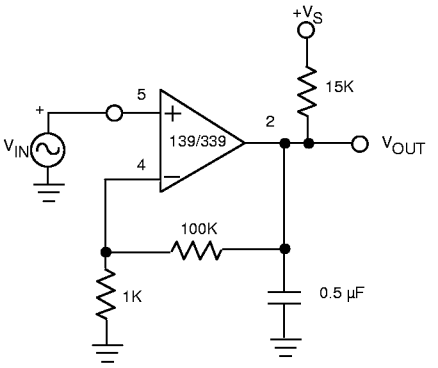


Figure 13. Low Frequency Op Amp

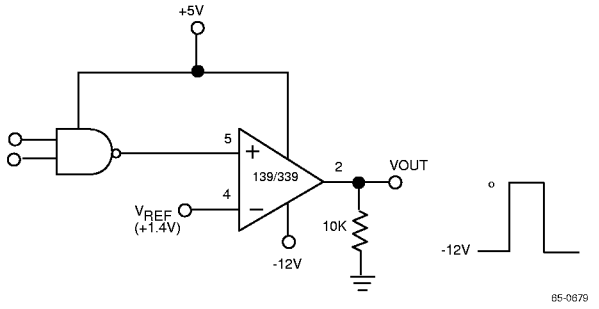


Figure 14. TTL to MOS Logic Converter

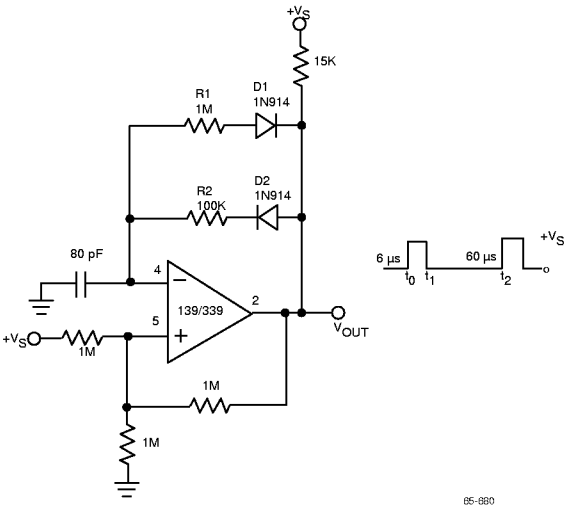


Figure 15. Pulse Generator

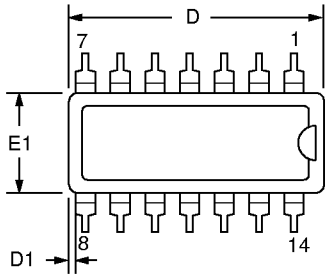
Mechcanical Dimensions

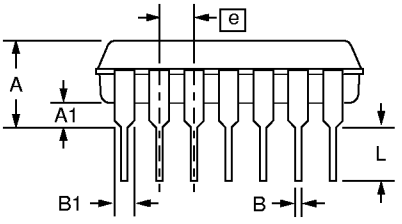
14-Lead Plastic DIP

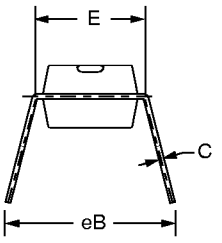
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.200	2.92	5.08	
N	14		14		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







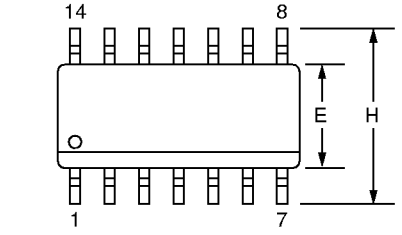
Mechanical Dimensions (continued)

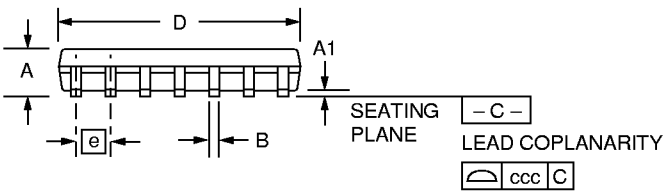
14-Lead Plastic SOIC

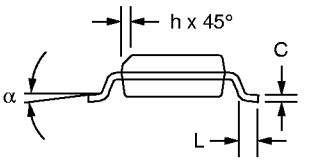
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	14		14		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







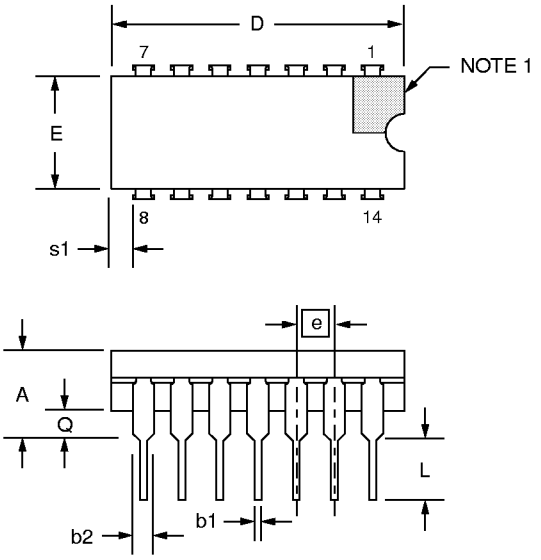
Mechanical Dimensions (continued)

14-Lead Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D	—	.785	—	19.94	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (leads number 1, 7, 8, and 14).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twelve spaces.



Ordering Information

Part Number	Package	Operating Temperature Range
LM339M	14-Lead Plastic SOIC	0°C to +70°C
LM339N	14-Lead Plastic DIP	0°C to +70°C
LM139D	14-Lead Ceramic DIP	-55°C to +125°C
LM139D/883B	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD/883B	14-Lead Ceramic DIP	-55°C to +125°C

Notes:

1. /883B suffix denotes MIL-STD-883, Level B processing

Raytheon Electronics
Semiconductor Division
350 Ellis Street
Mountain View, CA 94043
650.968.9211
FAX 650.966.7742

8/97 0.0m
Stock# DS60000139