QP SEMICONDUCTOR

October 9, 2007

QP7216L – CMOS 16 x 16 Multiplier

General Description

The QP7216L is a high-speed, low-power 16 x 16-bit multiplier, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and our high-performance, submicron CMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

The QP7216L is ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

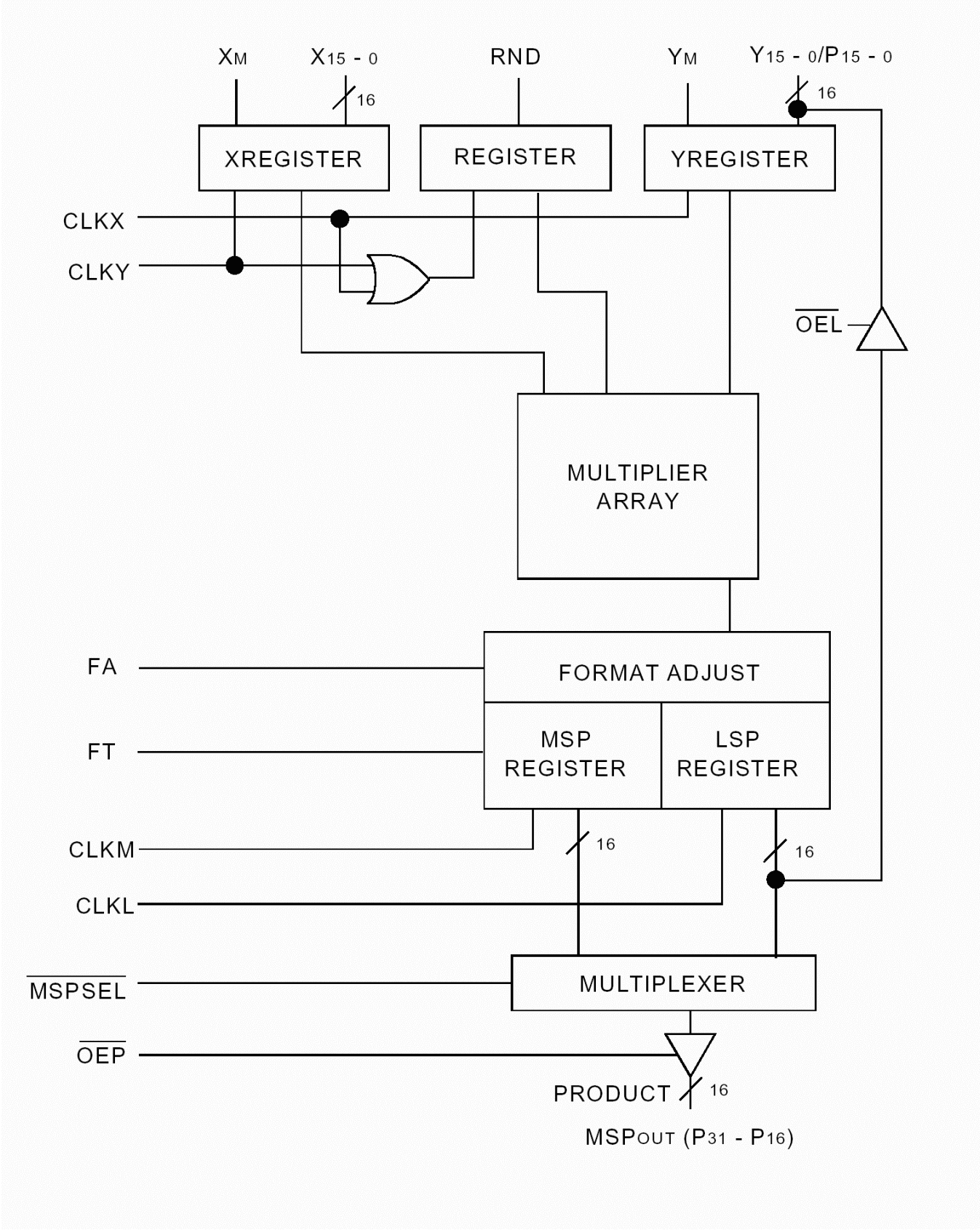
All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the QP7216L, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers.

The QP7216L offers additional flexibility with the FA control and $MSPSEL_{BAR}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. $MSPSEL_{BAR}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The QP7216L features:

- 16 x 16 parallel multiplier with double precision product.
- 16ns clocked multiply time
- Low power consumption: 120mA
- Pin and function compatible with TRW MPY016H/K, AMD29516, IDT7216 and CY7C516.
- Tri-state outputs
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible

Block Diagram

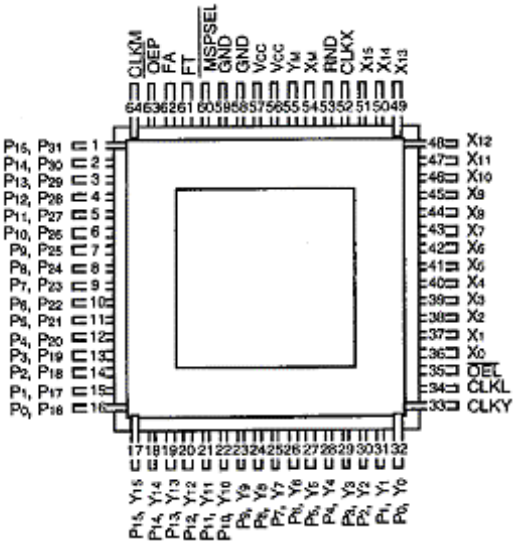


Pin Name	I/O	Description
X0-X15	I	Data inputs
Y0-Y15 / P0-P15	I/O	Y0-Y15 are data inputs P0-P15 are LSP register output, enabled when OELbar=0
P16-P31	O	Data Output (LSP or MSP)
OEL_{BAR}	I	Output enable control for LSP (least significant product). When low enables P0-P15. When high P0-P15 high-z (tri-state)
OEP_{BAR}	I	Output enable control for MSP (most significant product). When low enables P16-P31. When high P16-P31 high-z (tri-state)
XM, YM	I	Mode control for each data word. Low designates unsigned data input and high designates two's complement.
RND	I	"Round" control for rounding of MSP. When high, 1 is added to the most significant bit of LSP. This signal is affected by the state of the FA pin. When FA=1 and RND=1, 1 is added to the 2-15 bit (P15). When RND=1 and FA=0, 1 is added to the 2-16 bit (P14). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY. Rounding always occurs in the positive direction, which may introduce a systematic bias.
$MSPSEL_{BAR}$	I	When low, MSP is output on P16-P31. When high, LSP is output on P16-P31.
FA	I	Format adjust control. When high, a full 32-bit product is selected. When low, a left shifted 31-bit product is selected with the sign bit replicated in the LSP. FA is normally high; except for certain fractional two's complement applications (see multiplier input/output formats).
FT	I	Flow through control. When high, both MSP and LSP registers are by-passed.
CLKX	I	X register clock input. Also clocks RND register.
CLKY	I	Y register clock input. Also clocks RND register.
CLKL	I	LSP register clock input.
CLKM	I	MSP register clock input.

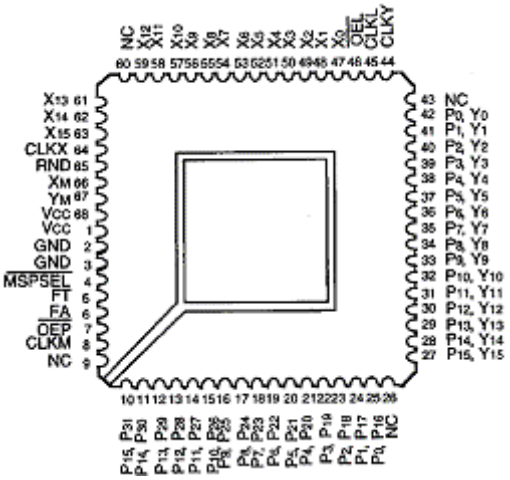
Connection Diagrams

QP7216L

Flat Pack



LCC

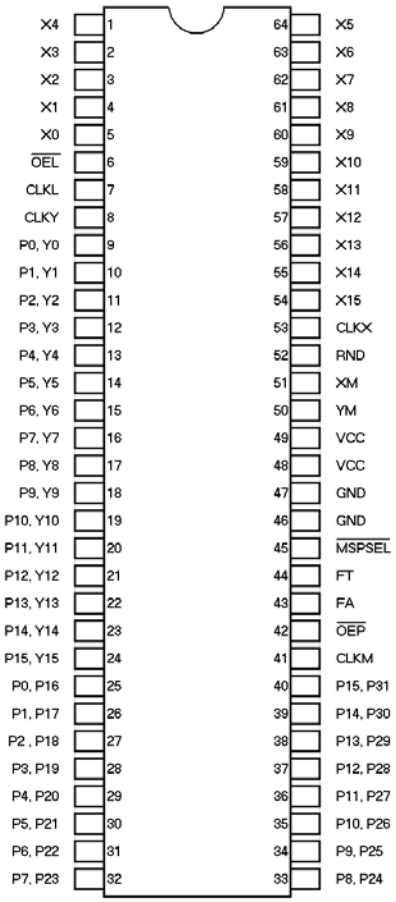


PGA

	A	B	C	D	E	F	H	H	J	K	L
11		NC	X13	X15	RND	YM	VCC	GND	FT	OEP	
10	X11	X12	X14	CLKS	XM	VCC	GND	MSP SEL	FA	CLKM	NC
9	X9	X10								P30 P14	P31 P15
8	X7	X8								P28 P12	P29 P13
7	X5	X6								P26 P10	P27 P11
6	X3	X2								P24 P8	P25 P7
5	X1	X2								P22 P6	P23 P7
4	OEL	X0								P20 P4	P21 P3
3	CLKY	CLKL								P18 P2	P19 P3
2	NC	Y0 P0	Y2 P2	Y4 P4	Y6 P6	Y8 P8	Y10 P10	Y12 P12	Y14 P14	P16 P0	P17 P1
1		Y1 P1	Y3 P3	Y5 P5	Y7 P7	Y9 P9	Y11 P11	Y13 P13	Y15 P15	NC	

Pin 1 Designator

DIP



Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Power Supply and Input Voltage	-0.5 to +7.0	Volts DC	
Terminal Voltage with respect to GND	-0.5 to V_{CC}+0.5	Volts	
DC Output Current	50	MA	
Storage Temperature Range	-65 to +150	ºC	
Lead Temperature (soldering, 10 seconds)	+300	ºC	
Junction Temperature (T_J)	+150	ºC	

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
Input or Output Voltage Range	0.0 to V_{CC}	Volts DC	/5
Minimum High-Level Input Voltage (V_{IH})	2.0	Volts DC	
Maximum Low-Level Input Voltage (V_{IL})	0.8	Volts DC	
Maximum high level output current	-2	mA	
Maximum low level output current	8	mA	
Case Operating Range (T_c)	-0C to +70	ºC /5	Commercial
Case Operating Range (T_c)	-40C to +85	ºC /5	Industrial
Case Operating Range (T_c)	-55 to +125	ºC /5	Military

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

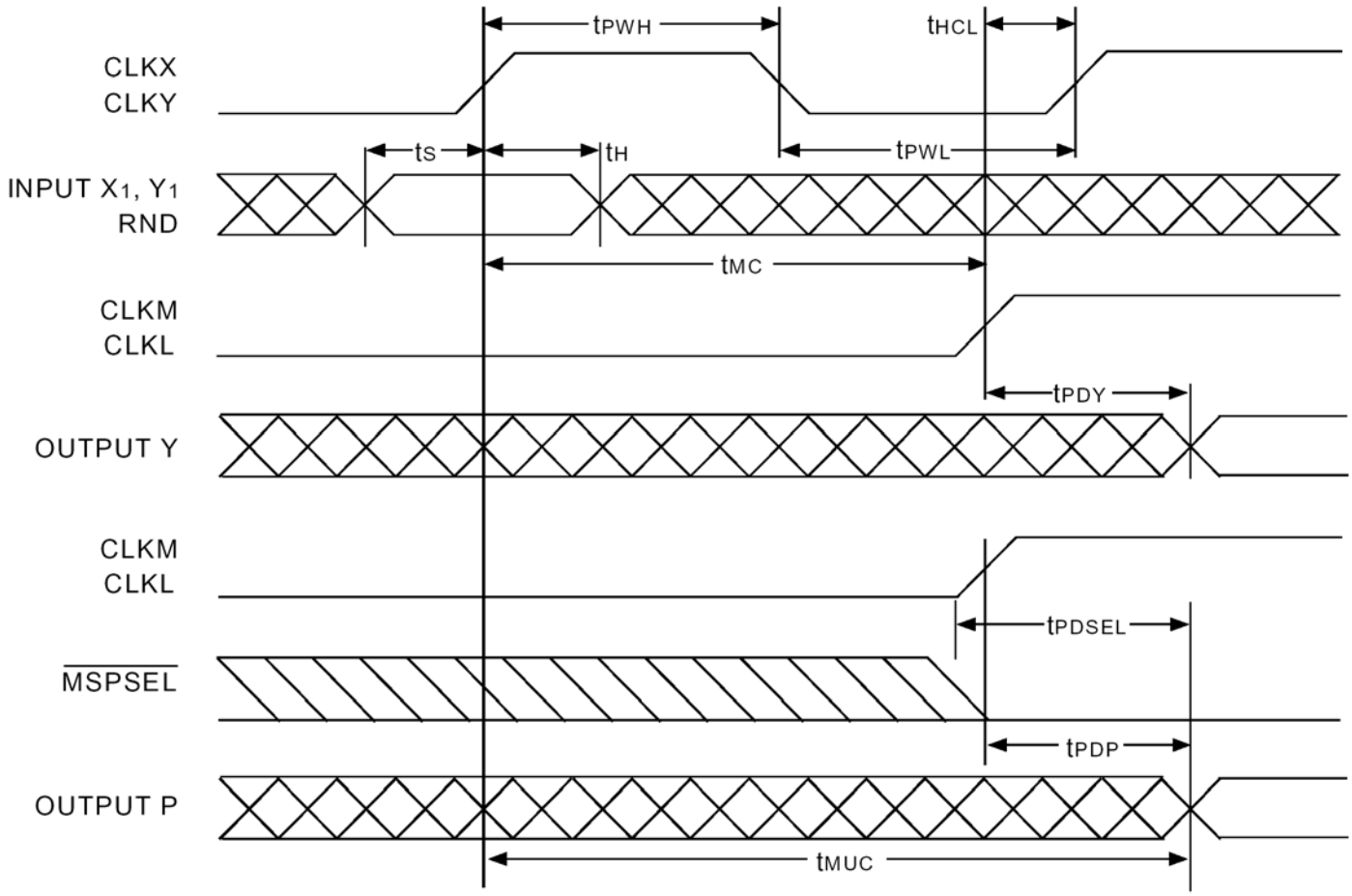
Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified	Min	Max	Unit
All Devices					
Input High Voltage	V_{IH}	V_{CC} = 4.5V	3.0		V
Input Low Voltage	V_{IL}	V_{CC} = 5.5V		0.8	mA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = 0-V_{CC}	-10.0	+10.0	mA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V, OE_{BAR}=3.5V, V_{OUT} = 0 to VCC	-10.0	+10.0	µA
Operating Power Supply Current	I_{CC}	V_{CC} = 5.5V, OE_{BAR}=3.5V, f = 10MHz		+110.0	mA
Quiescent Power Supply Current	I_{CCQ1}	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$		+40.0	mA
Quiescent Power Supply Current	I_{CCQ2}	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V		+25.0	mA
Increase in Power Supply Current (above 10MHz)	$I_{CC/f}$	V_{CC} = 5.5V, OE_{BAR}=3.5V		+6.0	mA/MHz /1
Short Circuit Current /3	I_{OS}	V_{CC} = 5.5V, V_{OUT} = 0.0V		-120	mA
Output High Voltage	V_{OH}	V_{CC} = 4.5V, I_{OH}= -2mA	2.4		V
Output Low Voltage	V_{OL}	V_{CC} = 4.5V, I_{OL}= 8 mA		0.4	V /2

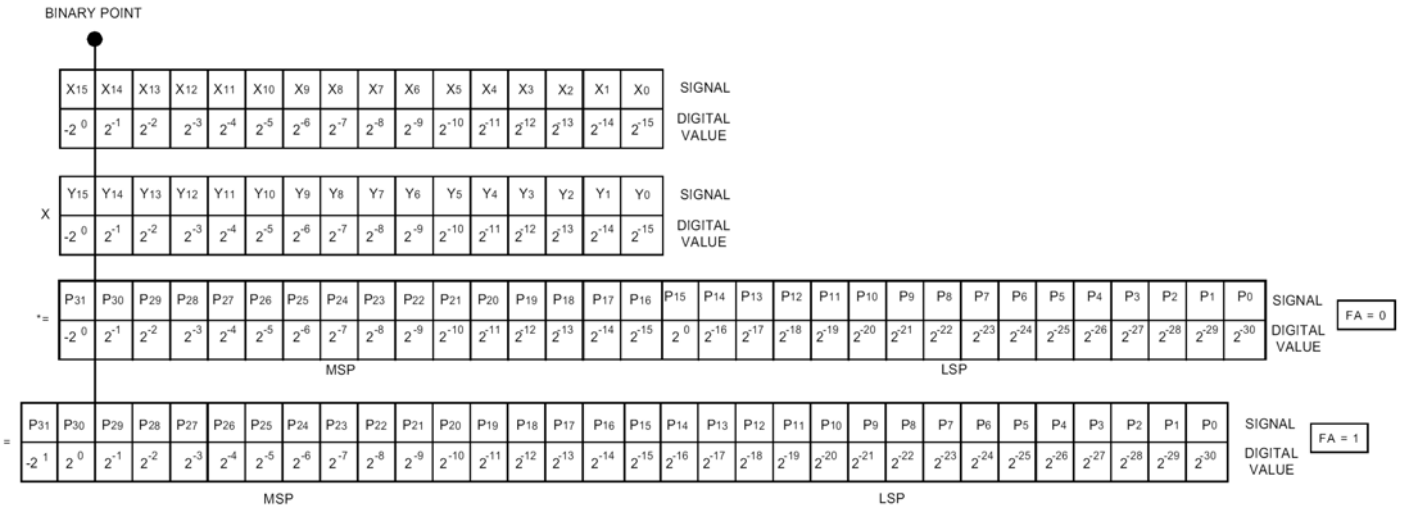
TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS					
Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified	Min	Max	Unit
20ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		50 /4	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		20	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	11		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	1		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	9		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	9		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		18	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		18	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		18	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		15	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		15	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns
25ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		50 /4	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		25	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	12		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	2		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	10		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	10		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		20	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		20	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		20	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		18	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		18	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns
30ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		50 /4	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		30	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	12		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	2		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	10		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	10		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		20	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		20	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		20	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		20	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		20	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS					
Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified	Min	Max	Unit
42ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		65	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		42	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	15		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	3		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	15		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	15		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		25	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		30	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		30	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		25	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		25	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns
55ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		75	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		55	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	20		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	3		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	25		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	25		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		30	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		30	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		30	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		31	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		30	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns
75ns					
Unclocked Multiply Time /1	MUC	V_{CC} = 5.0V		100	ns
Clocked Multiply Time	MC	V_{CC} = 5.0V		75	ns
X, Y, RND Set-up Time	t_S	V_{CC} = 5.0V	25		ns
X, Y, RND Hold Time	t_H	V_{CC} = 5.0V	3		ns
Clock Pulse Width HIGH	t_{PWH}	V_{CC} = 5.0V	30		ns
Clock Pulse Width LOW	t_{PWL}	V_{CC} = 5.0V	30		ns
$MSPSEL_{BAR}$ to Product Out /1	t_{PDSEL}	V_{CC} = 5.0V		35	ns
Output Clock to P /1	t_{PDP}	V_{CC} = 5.0V		35	ns
Output Clock to Y /1	t_{PDY}	V_{CC} = 5.0V		40	ns
Tri-State Enable Time	t_{ENA}	V_{CC} = 5.0V		36	ns
Tri-State Disable Time	t_{DIS}	V_{CC} = 5.0V		40	ns
Clock LOW Hold Time /1 CLKX/Y Relative to CLKM/L	t_{HCL}	V_{CC} = 5.0V	0		ns

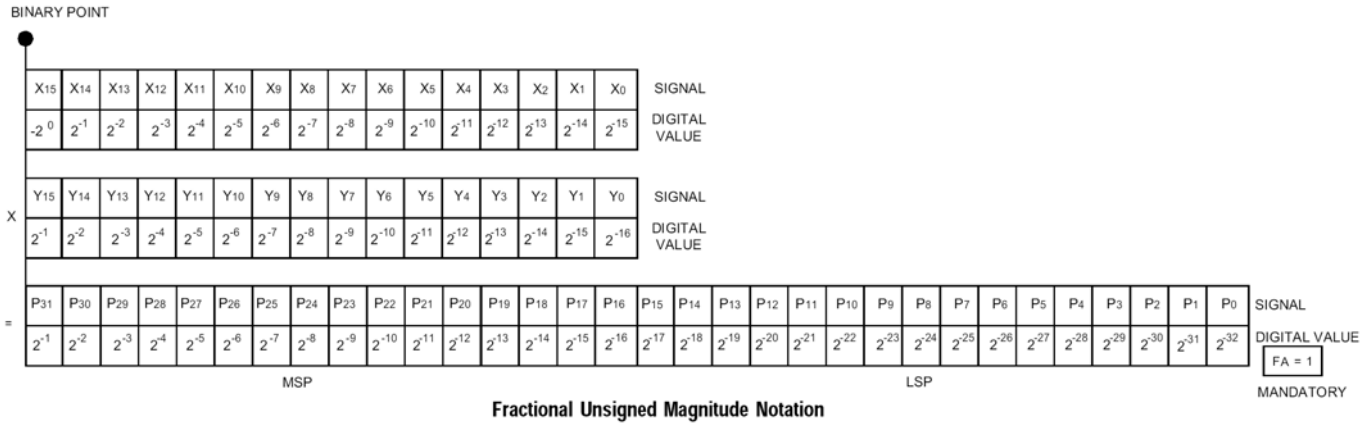
/1 – Guaranteed, Not Tested
/2 – 4mA for t_{MC} > 65ns.
/3 – Duration not to exceed 1 second, one output at a time.
/4 – Unclocked Multiply Time Slower than Original Manufacturer Device
/5 – Maximum PD, Maximum T_J Are Not to Be Exceeded

TIMING DIAGRAM



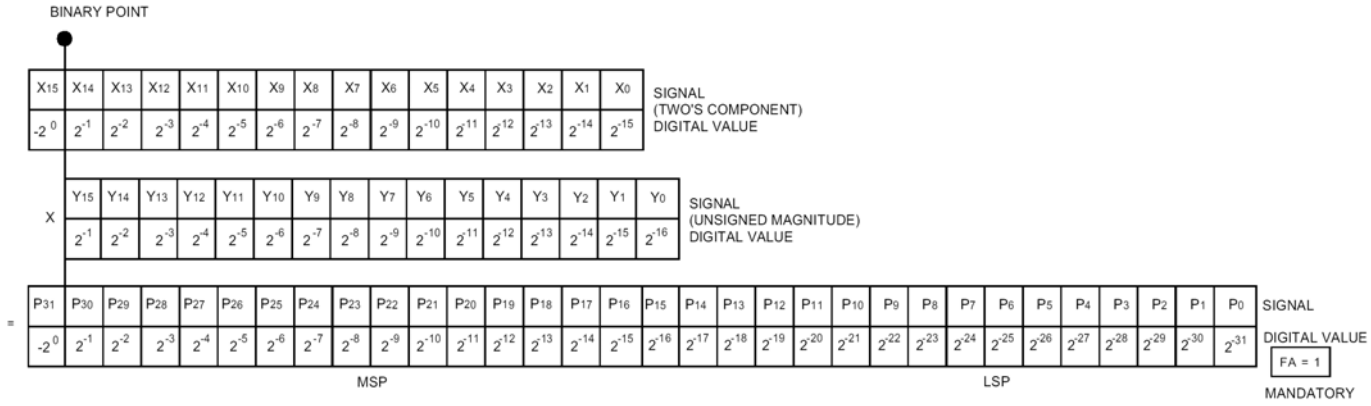


Fractional Two's Complement Notation

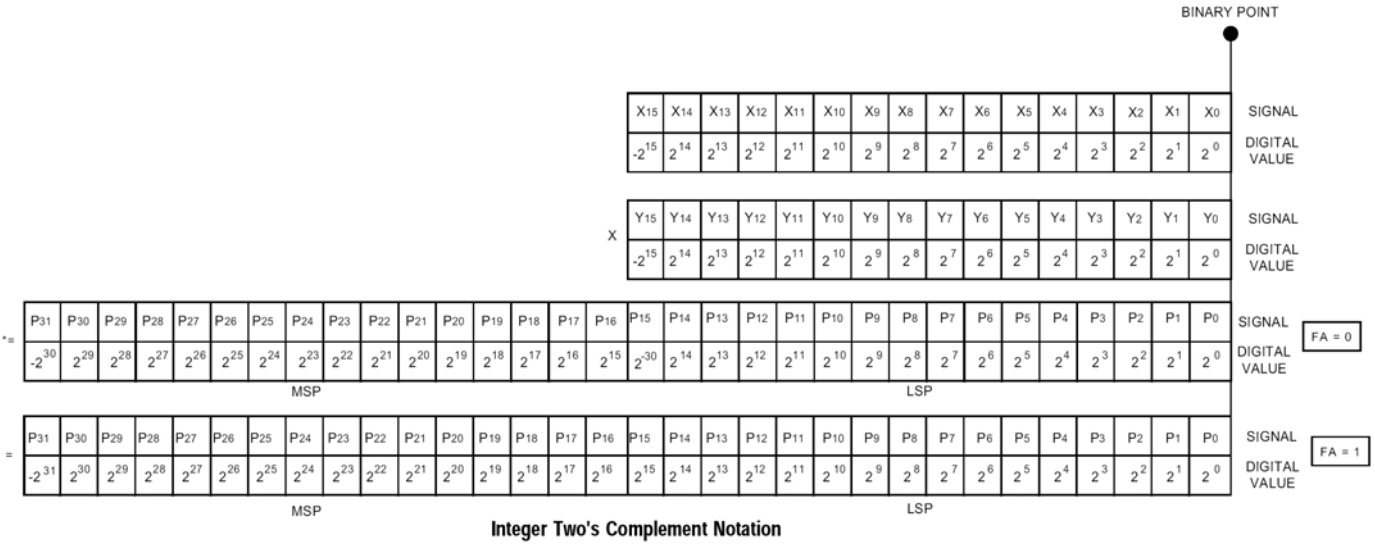


Fractional Unsigned Magnitude Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yeilding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

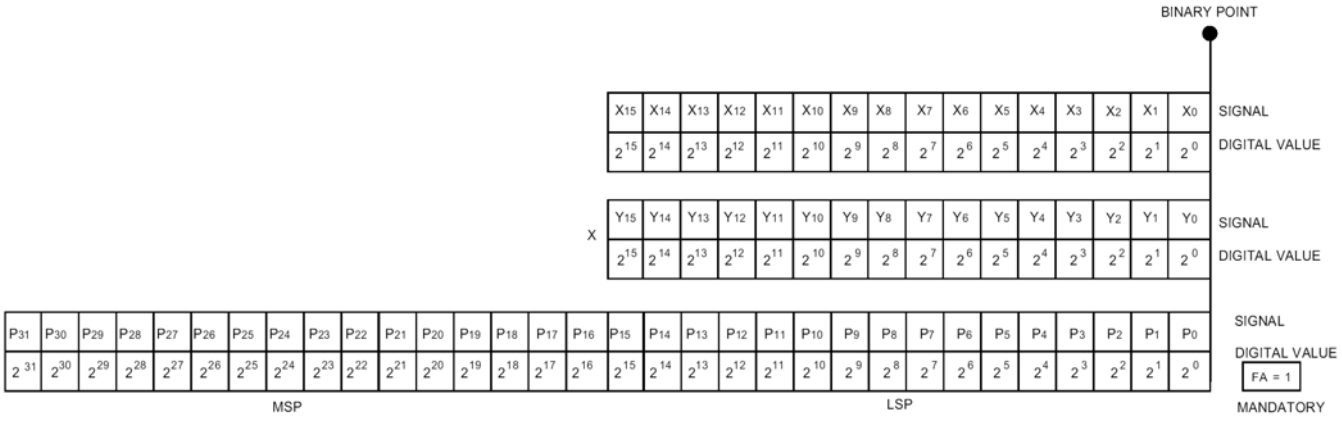


Fractional Mixed Mode Notation

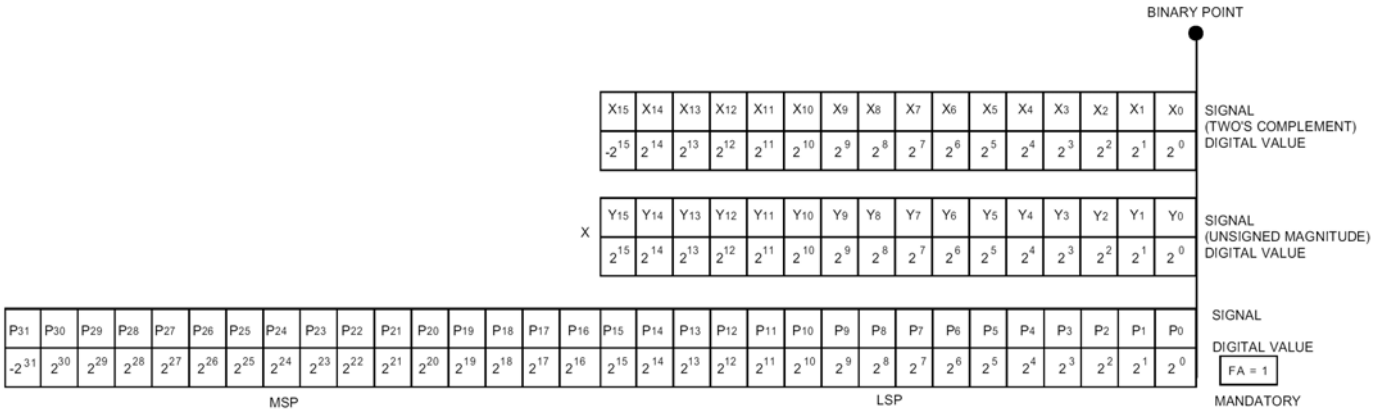


Integer Two's Complement Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000...0 with 1,000.0 yeilding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.



Integer Unsigned Magnitude Notation



Integer Mixed Mode Notation

Ordering Information

Temp Range	Part Number	Multiply T_{Clock}	Package (Mil-Std-1835)	Generic
Military	QP7216L20DB-MIL	20 ns	CDIP1-T64	7216L
Military	QP7216L20LB-MIL	20 ns	CQCC1-N68	7216L
Military	QP7216L20ZB-MIL	20 ns	CMGA15-PN 68	7216L
Military	QP7216L20FB-MIL	20 ns	CerQuad 64	7216L
Military	QP7216L20GB-MIL	20 ns	CMGA3-PN 68	7216L
Military	QP7216L25DB-MIL	25 ns	CDIP1-T64	7216L
Military	QP7216L25LB-MIL	25 ns	CQCC1-N68	7216L
Military	QP7216L25ZB-MIL	25 ns	CMGA15-PN 68	7216L
Military	QP7216L25FB-MIL	25 ns	CerQuad 64	7216L
Military	QP7216L25GB-MIL	25 ns	CMGA3-PN 68	7216L
Military	QP7216L30DB-MIL	30 ns	CDIP1-T64	7216L
Military	QP7216L30LB-MIL	30 ns	CQCC1-N68	7216L
Military	QP7216L30ZB-MIL	30 ns	CMGA15-PN 68	7216L
Military	QP7216L30FB-MIL	30 ns	CerQuad 64	7216L
Military	QP7216L30GB-MIL	30 ns	CMGA3-PN 68	7216L

Temp Range	Part Number	Multiply T_{Clock}	Package (Mil-Std-1835)	Generic
Military	QP7216L42DB-MIL	42 ns	CDIP1-T64	7216L
Military	QP7216L42LB-MIL	42 ns	CQCC1-N68	7216L
Military	QP7216L42ZB-MIL	42 ns	CMGA15-PN 68	7216L
Military	QP7216L42FB-MIL	42 ns	CerQuad 64	7216L
Military	QP7216L42GB-MIL	42 ns	CMGA3-PN 68	7216L
Military	QP7216L55DB-MIL	55 ns	CDIP1-T64	7216L
Military	QP7216L55LB-MIL	55 ns	CQCC1-N68	7216L
Military	QP7216L55ZB-MIL	55 ns	CMGA15-PN 68	7216L
Military	QP7216L55FB-MIL	55 ns	CerQuad 64	7216L
Military	QP7216L55GB-MIL	55 ns	CMGA3-PN 68	7216L
Military	QP7216L75DB-MIL	75 ns	CDIP1-T64	7216L
Military	QP7216L75LB-MIL	75 ns	CQCC1-N68	7216L
Military	QP7216L75ZB-MIL	75 ns	CMGA15-PN 68	7216L
Military	QP7216L75FB-MIL	75 ns	CerQuad 64	7216L
Military	QP7216L75GB-MIL	75 ns	CMGA3-PN 68	7216L

QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

"-MIL" products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com