QP7133SA
QP7133LA
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QP7133SA & QP7133LA High-Speed 2K x 16 Dual-Port Static RAM

General Description

The QP7133SA/LA are CMOS Fast 2K x 16 Dual-Port Static RAMs (SRAM). QP Semiconductor designed the QP7133SA/LA to be direct replacements for the IDT7133SA/LA. They are designed to be used as stand-alone Dual-Port RAMs in 16 bit applications.

The QP7133SA/LA support asynchronous access for reads or writes to any location in memory via two independent ports with separate control and address and I/O pins that function identically to the IDT7133SA/IDT7133LA.

The QP7133SA/LA have an automatic power down feature controlled by the appropriate Chip Enable ($\overline{CE}$) pin that puts each port into a very low standby power mode.

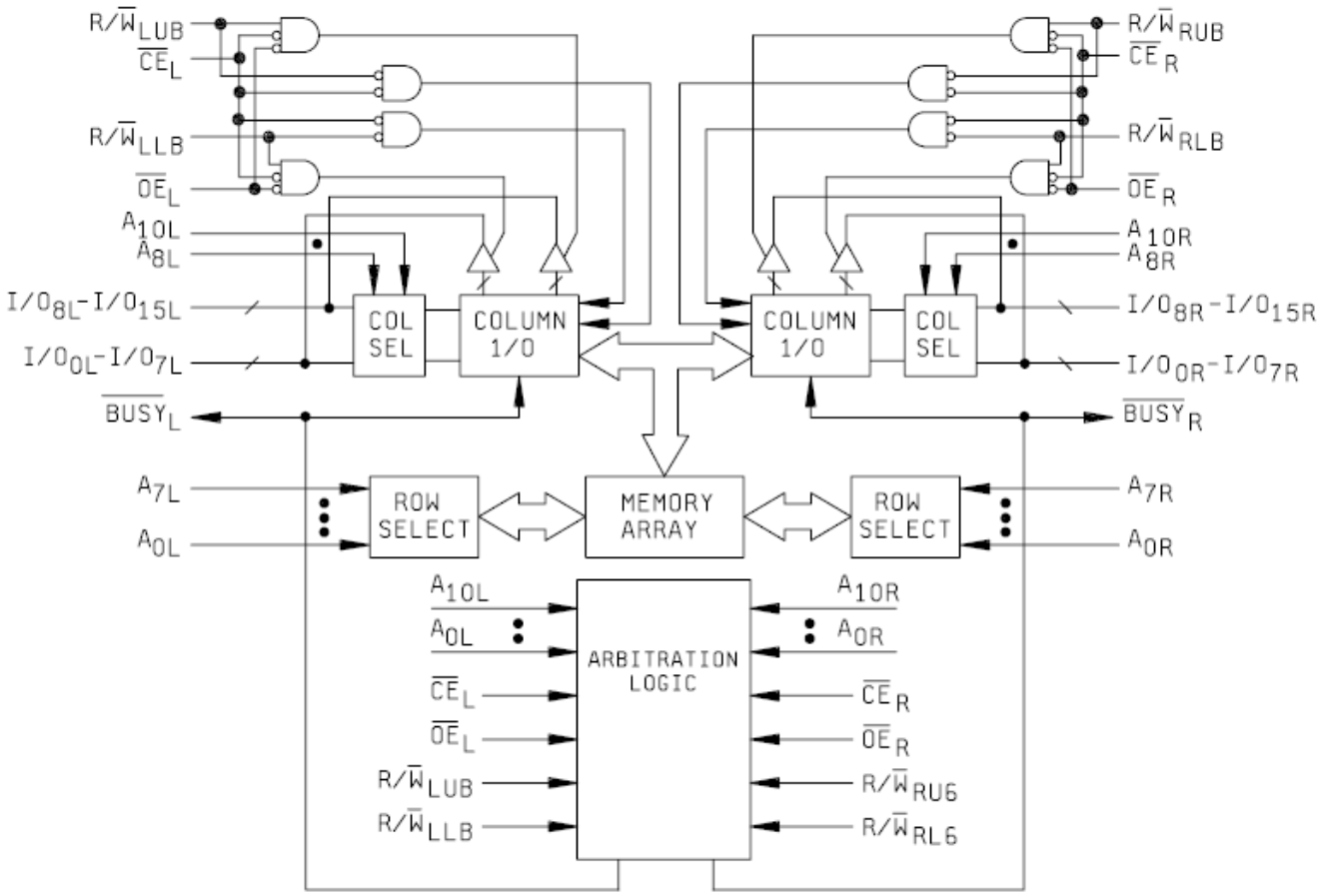
The QP7133SA/LA utilize CMOS high-performance technology which allows access times as fast as 35ns and low power consumption typically at 750mW. The QP7133LA is the low-power version which offers a battery backup data retention capability with typical power consumption of 10µW from a 2V source.

The QP7133SA/LA are available in hermetic ceramic 68-pin PGA and ceramic 68-pin Flatpack packages. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- Fully asynchronous operation from either port
- High-speed access
  - Military: 35/45/55/70/90 ns
- Low-power operation
  - QP7133SA
    - Active: 750mW (typ.)
    - Standby: 0.2mW (typ.)
  - QP7133LA
    - Active: 750mW (typ.)
    - Standby: 0.2mW (typ.)
    - Data Retention mode: 10µW (typ.)
- Separate upper-byte and lower-byte write control for each port
- On-chip port arbitration logic
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Packages: 68-pin PGA & 68-pin Flatpack
- Available as SMD# 5962-88665 and 5962-88610
- Industrial temperature range (–40°C to +85°C) is available

Block Diagram

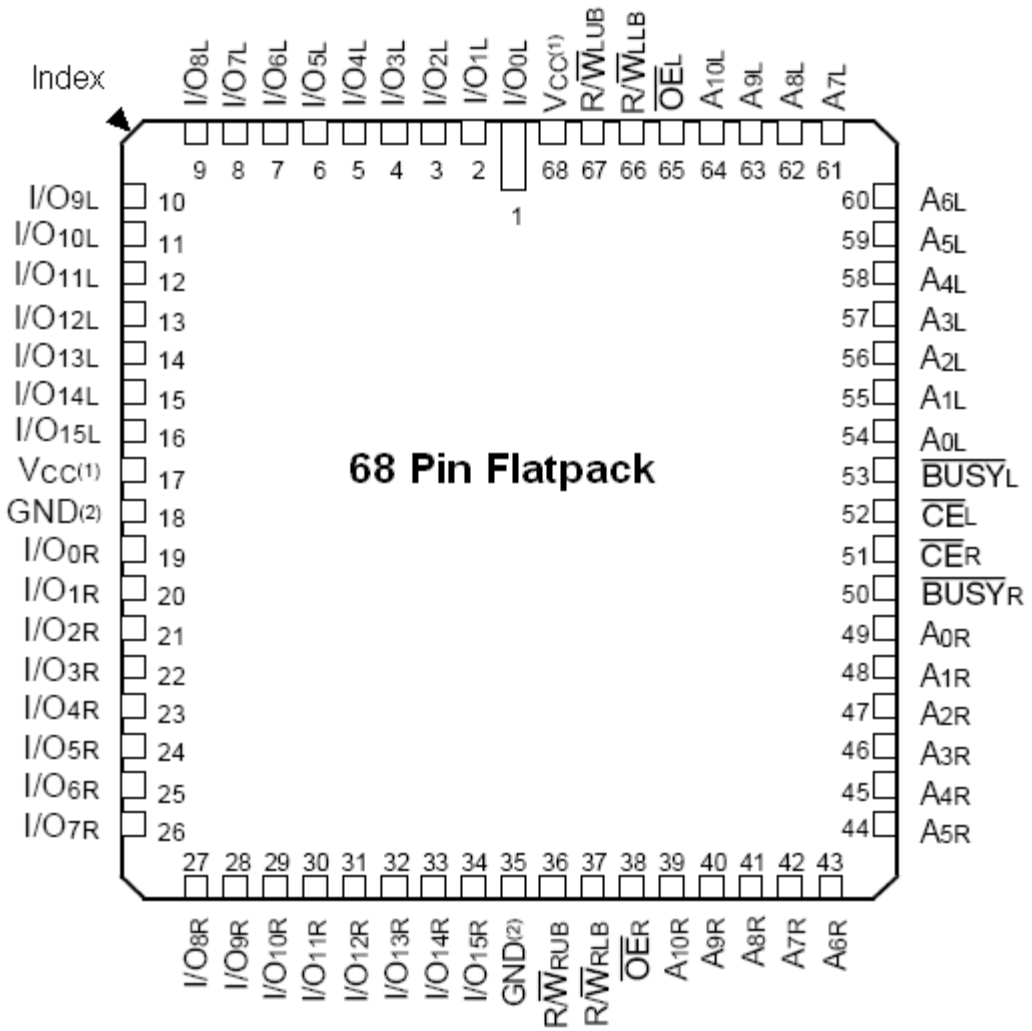


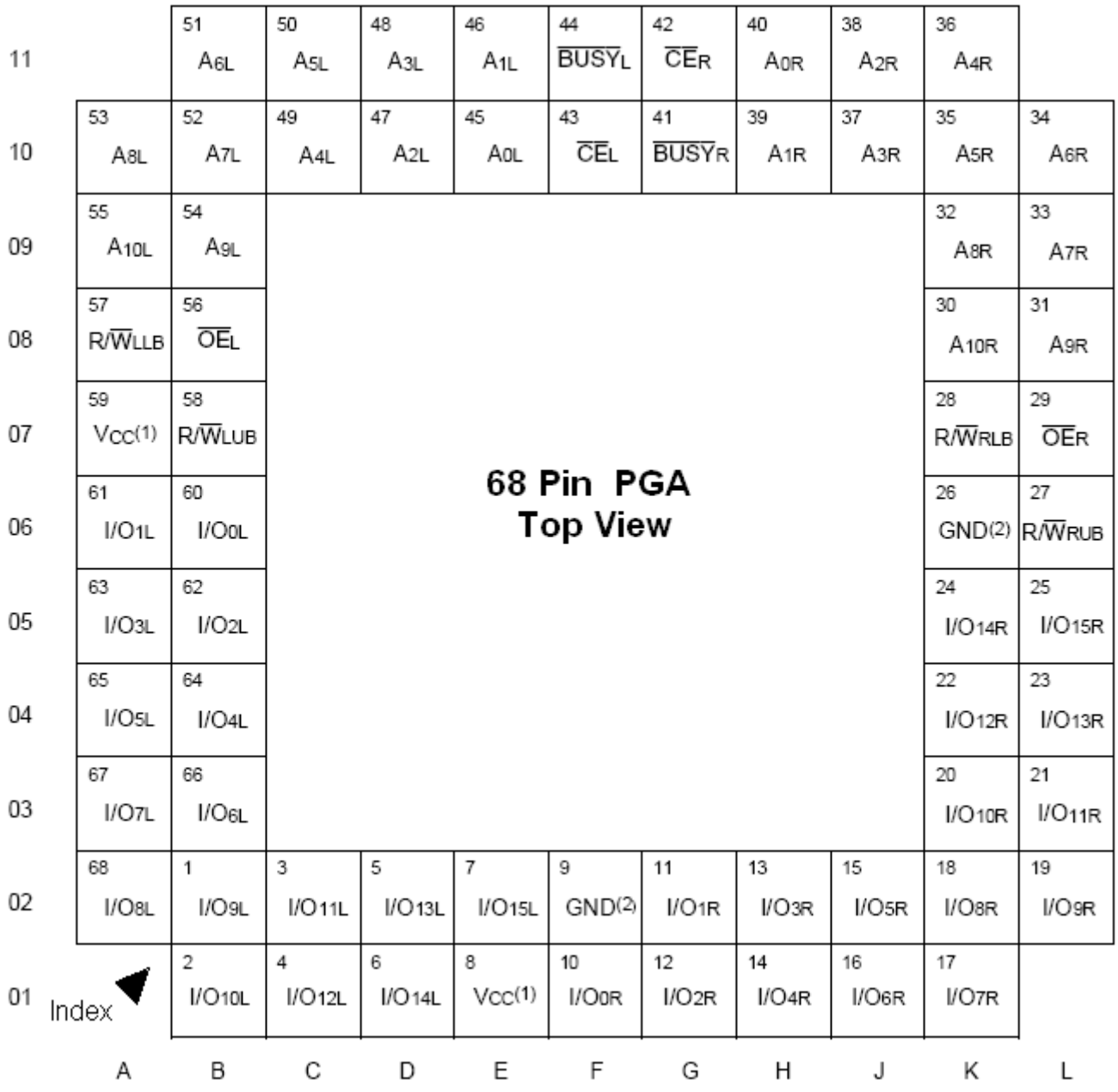
Notes:
$\overline{\text{BUSY}}$ is an open drain output and requires pull-up resistor

Functional Description

Left Port	Right Port	Functional Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_{LUB}$	R/$\overline{W}_{RUB}$	Read/Write Enable-upper byte
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
R/$\overline{W}_{LLB}$	R/$\overline{W}_{RLB}$	Read/Write Enable-lower byte
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} – A_{10L}$	$A_{0R} – A_{10R}$	Address
$I/O_{0L} – I/O_{15L}$	$I/O_{0R} – I/O_{15R}$	Data Input/Output
V_{CC}		Power- All V_{CC} pins must be connected to a power supply
GND		Ground- All GND pins must be connected to a good ground

Connection Diagrams




68 Pin PGA
Top View
Index
11 51 A6L 50 A5L 48 A3L 46 A1L 44 BUSYL 42 CER 40 A0R 38 A2R 36 A4R
10 53 A8L 52 A7L 49 A4L 47 A2L 45 A0L 43 CEL 41 BUSYR 39 A1R 37 A3R 35 A5R 34 A6R
09 55 A10L 54 A9L 32 A8R 33 A7R
08 57 R/WLLB 56 OEL 30 A10R 31 A9R
07 59 VCC(1) 58 R/WLUB 28 R/WRLB 29 OER
06 61 I/O1L 60 I/O0L 26 GND(2) 27 R/WRUB
05 63 I/O3L 62 I/O2L 24 I/O14R 25 I/O15R
04 65 I/O5L 64 I/O4L 22 I/O12R 23 I/O13R
03 67 I/O7L 66 I/O6L 20 I/O10R 21 I/O11R
02 68 I/O8L 1 I/O9L 3 I/O11L 5 I/O13L 7 I/O15L 9 GND(2) 11 I/O1R 13 I/O3R 15 I/O5R 18 I/O8R 19 I/O9R
01 2 I/O10L 4 I/O12L 6 I/O14L 8 VCC(1) 10 I/O0R 12 I/O2R 14 I/O4R 16 I/O6R 17 I/O7R
A B C D E F G H J K L

Absolute Maximum Ratings /1

Condition	Rating	Units
Supply Voltage Range	-0.5 to +7.0	Volts DC
Input Voltage	-0.5 to +6.0	Volts DC
Storage Temperature Range	-65 to +150	°C
Output Current	50	mA
Maximum Power Dissipation (P_D)	2.0	W
Lead Temperature (soldering, 10 seconds)	+260	ºC
Junction Temperature (T_J)	+150	ºC

/1Stresses above the AMR may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. All voltages referenced to GND, unless otherwise specified.

Recommended Operating Conditions /1

Condition	Rating	Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
High-Level Input Voltage (V_{IH})	2.2 to 6.0	Volts DC	
Low-Level Input Voltage (V_{IL})	-0.5 to +0.8	Volts DC	
Case Operating Range (T_c)	-55C to +125	ºC	

/1Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

ELECTRICAL PERFORMANCE CHARACTERISTICS-DC

Test	Symbol	Conditions $-55^oC \le T_A \le +125^oC$ $4.5\ V \le V_{CC} \le 5.5\ V$		Min	Typ	Max	Unit
Output Low Voltage	V_{OL}	V_{CC} = 4.5V, V_{IH} = 2.2V, V_{IL}= 0.8V	I/O_0-I/O_{15} I_{OL}= 4mA,			0.4	V
			$\overline{BUSY}$ I_{OL}= 16mA,			0.5	
Output High Voltage	V_{OH}	V_{CC}= 4.5V, I_{OH}= -4mA, V_{IH}= 2.2V, V_{IL}=0.8V		2.4			V
Input Leakage Current	I_{LI}	V_{CC}= 5.5V $GND \le V_{IN} \le V_{CC}$				5	µA
Output Leakage Current	I_{LO}	V_{CC}= 5.5V, $\overline{CE}$ =V_{IH}, $GND \le V_{OUT} \le V_{CC}$				5	µA
Dynamic Operating Current (both ports active)	I_{CC1}	Outputs Open, V_{CC} = 5.5V, f= f_{max} /1, $\overline{CE}$ = V_{IL}			150	240	mA
Standby Supply Current (both ports) TTL Inputs	I_{SB1}	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$, V_{CC} = 5.5V, f= f_{max} /1			14	65	mA
Standby Supply Current (one port) TTL Inputs	I_{SB2}	Active ports outputs open $\overline{CE}_R$ = $\overline{CE}_L \ge V_{IH}$, V_{CC} = 5.5V, f= f_{max} /1			115	150	mA
Full Standby Supply Current (both ports) CMOS Inputs	I_{SB3}	$\overline{CE}_R$ = $\overline{CE}_L \ge V_{CC}$– 0.2V, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{cc}$ – 0.2V, V_{CC} = 5.5V, f= 0 /2			50	200	µA
Full Standby Supply Current (one port) CMOS Inputs	I_{SB4}	Active ports outputs open $\overline{CE}_R$ = $\overline{CE}_L \ge V_{CC}$– 0.2V, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{cc}$ – 0.2 V, V_{CC} = 5.5V, f= max /1			80	135	mA
Input Capacitance	C_{IN}	V_{IN} = 0 V, V_{CC} = 5.0V, f = 1MHz, T_A = 25°C /3				11	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V, V_{CC} = 5.0 V, f = 1MHz, T_A = 25°C /3				11	pF

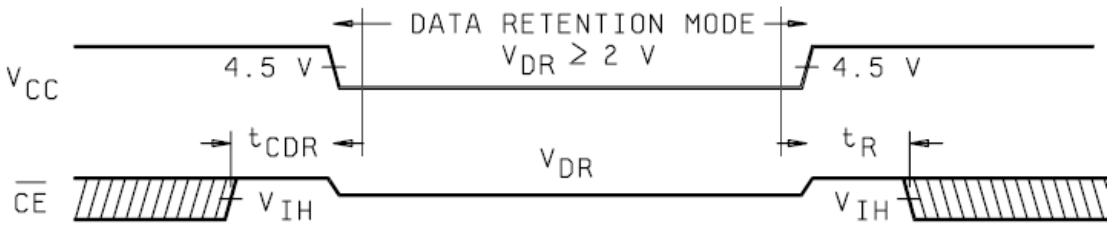
NOTE: Typical values are measured in accordance with load conditions described in the Output test Load sheet herein.

/1 At f_{MAX}, address and data inputs (excluding OE) are cycling at the maximum frequency of read cycle of $1/t_{RC}$, and using AC test conditions of input levels of GND to 3.0 V.
/2 f = 0 means no address or control lines change
/3 Measured at initial qualification only

ELECTRICAL PERFORMANCE CHARACTERISTICS-Data Retention						
Test	**Symbol**	**Conditions** **Conditions** **-55ºC ≤T_A≤+125ºC** **4.5 V ≤ Vcc ≤ 5.5 V**	**Min**	**Typ**	**Max**	**Unit**
V_{CC} Data Retention (QP7133LA only)	V_{DR}	$\overline{CE}$ ≥ V_{CC}– 0.2V, V_{CC} = 2.0 V V_{IN} ≥ V_{CC}– 0.2V or ≤ 0.2 V	2.0			V
Data Retention Current (QP7133LA only)	I_{CCDR}	$\overline{CE}$ ≥ V_{CC}– 0.2V, V_{CC} = 2.0 V V_{IN} ≥ V_{CC}– 0.2V or ≤ 0.2 V		5	100	µA
Chip Deselect to Data Retention Time /4 (QP7133LA only)	t_{CDR}	$\overline{CE}$ ≥ V_{CC} – 0.2V, Vcc = 2.0V V_{IN} ≥ Vcc – 0.2V or ≤ 0.2V /5 See output test load figures	0			ns
Operation Recovery Time /4 (QP7133LA only)	t_R	$\overline{CE}$ ≥ V_{CC} – 0.2V, Vcc = 2.0V V_{IN} ≥ Vcc – 0.2V or ≤ 0.2V /5 See output test load figures	t_{RC}			ns

/4 Parameter tested at initial characterization and after design change. Parameter guaranteed per limits in table.
/5 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Test Conditions shown herein.

Data Retention Mode Timing



ELECTRICAL PERFORMANCE CHARACTERISTICS- Read Cycle

Description	Symbol	Conditions $-55^oC \le T_A \le +125^oC$ $4.5\ V \le Vcc \le 5.5\ V$	Min	Max	Unit
Read Cycle Time /6	t_{RC}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	90 70 55 45 35		ns
Address Access Time /6	t_{AA}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		90 70 55 45 35	ns
Chip Enable Access time	t_{ACE}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		90 70 55 45 35	ns
Chip Enable to Pwr Up /6, /7	t_{PU}	ALL	0		ns
Chip Disable to Pwr Down /6, /7	t_{PD}	ALL		50	ns
Output Enable Access Time	t_{AOE}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		90 70 55 45 35	ns
Output Hold from Addr Change	t_{OH}	ALL	0		ns
Output- Low Z	t_{LZ}	ALL	5		ns
Output- High Z	t_{HZ}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		40 35 20 20 20	ns

/6 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load shown herein.
/7 Parameter tested at initial characterization and after design change. Parameter guaranteed per limits in table.

ELECTRICAL PERFORMANCE CHARACTERISTICS- Write Cycle

Description	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ $4.5\ V \leq Vcc \leq 5.5\ V$	Min	Max	Unit
Write Cycle	t_{WC}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	90 70 55 45 35		ns
Chip Enable to End-of-Write	t_{EW}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	50 50 40 30 25		ns
Address valid to End of Write	t_{AW}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	50 50 40 30 25		ns
Address Set-up	t_{AS}	ALL	0		ns
Write Pulse	t_{WP}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	55 50 40 30 25		ns
Write Recovery	t_{WR}	ALL	0		ns
Data Valid to End of Write	t_{DW}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	30 25 20 20 20		ns
Output High Z /9	t_{HZ}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		25 25 20 20 20	ns
Data Hold Time /8	t_{DH}	ALL	0		ns
Write Enable to Output (in High Z) /9	t_{WZ}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		25 25 20 20 20	ns
Output Active from End of Write /8	t_{OW}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35	0 0 5 5 5		ns

/8 $t_{DH} < t_{OW}$

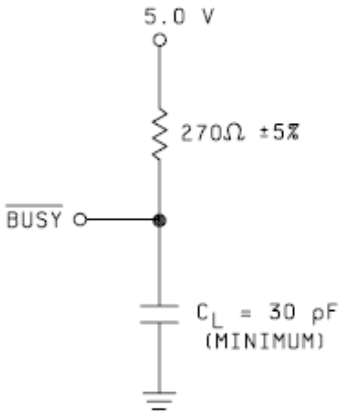
/9 Measurement assumption: transition times ≤ 5 ns, input levels from GND to 3.0 V, timing ref levels of 1.5 V and output load per AC Output Test Load shown herein.

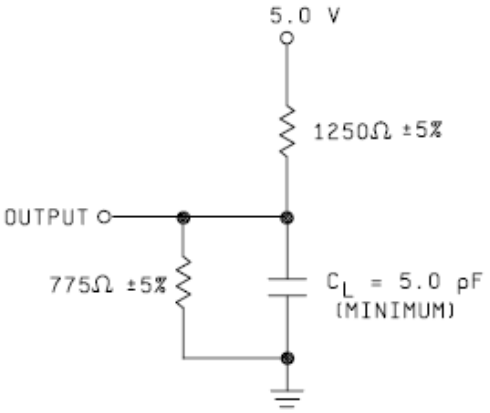
ELECTRICAL PERFORMANCE CHARACTERISTICS- $\overline{\text{BUSY}}$ Timing

Description	Symbol	Conditions -55ºC ≤T_A≤+125ºC 4.5 V ≤ Vcc ≤ 5.5 V	Min	Max	Unit
$\overline{\text{BUSY}}$ Access Time from Address	t_{BAA}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		55 55 50 45 35	ns
$\overline{\text{BUSY}}$ Disable Time from Address	t_{BDA}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		45 45 40 40 30	ns
$\overline{\text{BUSY}}$ Access Time from Chip Enable	T_{BAC}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		45 35 35 30 25	ns
$\overline{\text{BUSY}}$ Disable Time from Chip Enable	T_{BDC}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		45 30 30 25 20	ns
Write Pulse to data Delay /13	T_{WDD}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		90 90 80 60 60	ns
Write Data Valid to Read Data Delay /13	T_{DDD}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		70 70 55 45 45	ns
$\overline{\text{BUSY}}$ Disable to Valid Data /10	T_{BDD}	SA or LA 90 SA or LA 70 SA or LA 55 SA or LA 45 SA or LA 35		40 40 40 40 35	ns
Arbitration priority Set-up Time /11	T_{APS}	ALL	5		ns
Write Hold after $\overline{\text{BUSY}}$ /12	t_{WH}	ALL	30		ns

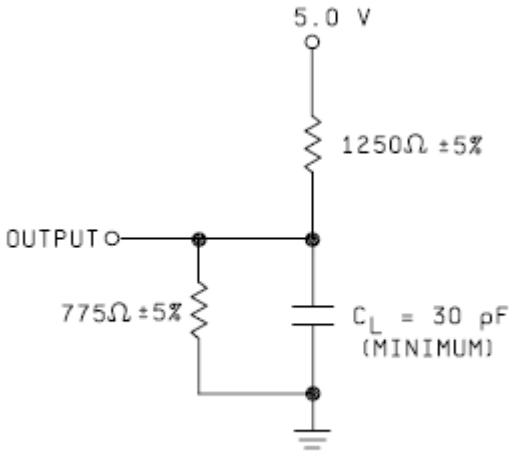
/10 t_{BDD} is calculated parameter and is greater of 0, $t_{WDD} – t_{WP}$ or $t_{DDD} – t_{DW}$
/11 required to ensure that either of the two ports asserted first
/12 To ensure completion of write cycle on either port following contention.
/13 Refer to timing waveform “Write with Port-to-port Read and Busy” for port-to-port delay through RAM cells from write port to read port.

Output Test Load





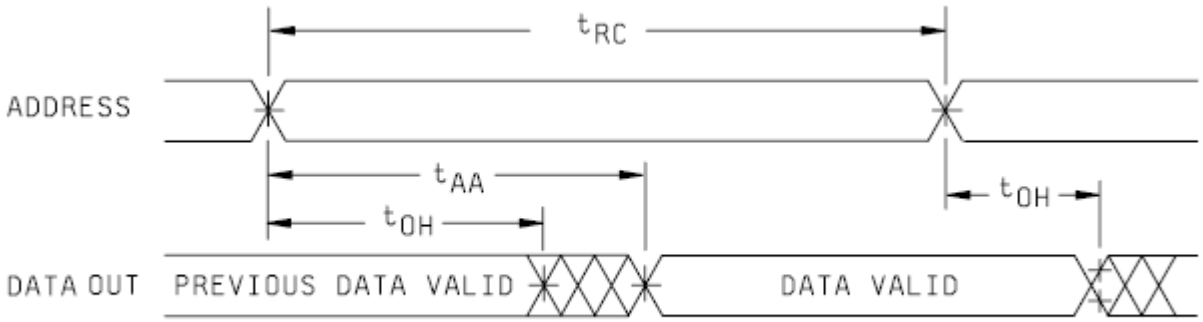
$\overline{\text{BUSY}}$ Output load **Output load: t_{HZ} t_{LZ} t_{WZ} t_{OW}**



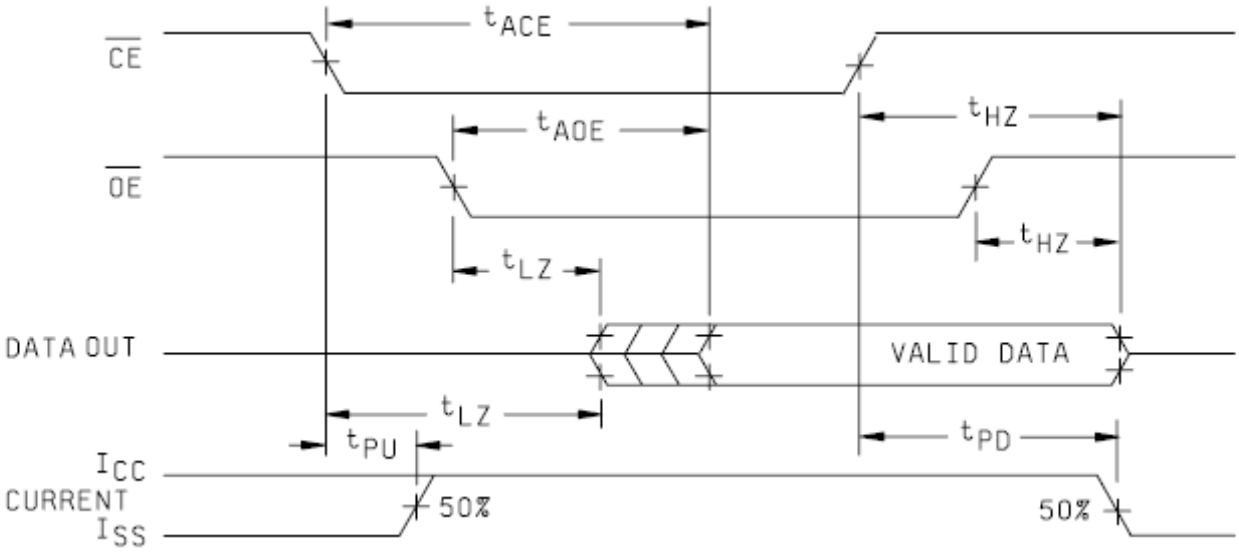
Output test load

AC TEST CONDITIONS	
Input Pulse levels	GND to 3.0 V
Input rise & fall times (t_r & t_f)	≤ 5ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Read Cycle 1 (notes 1,2,4)



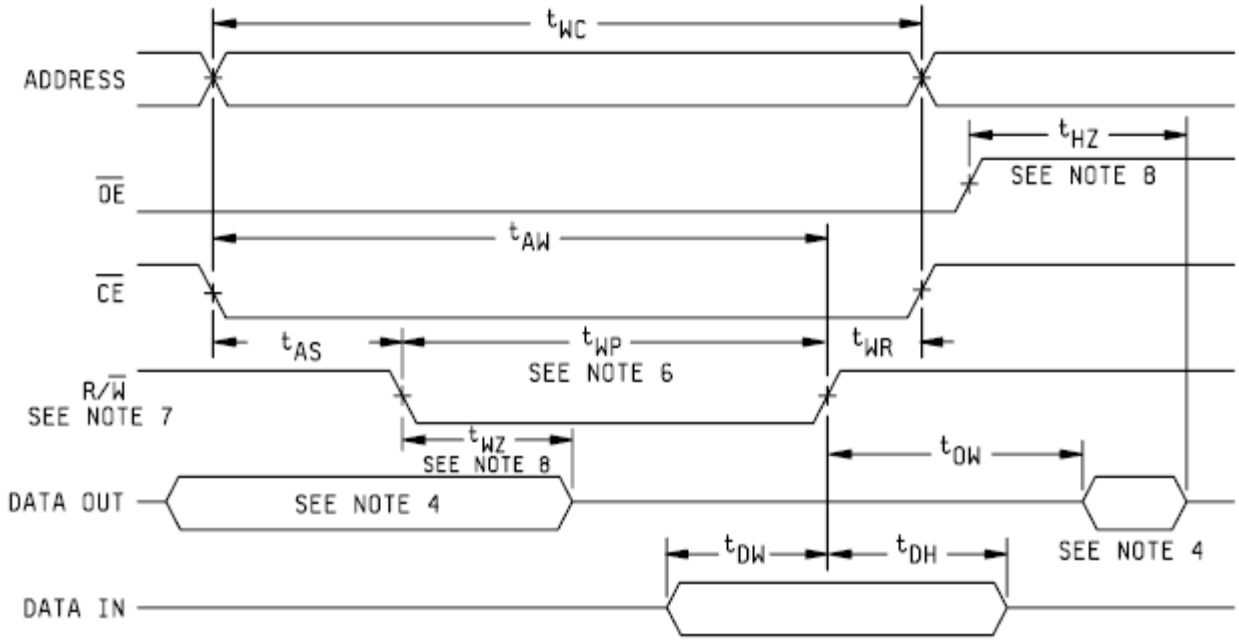
Read Cycle 1 (notes 1,3)



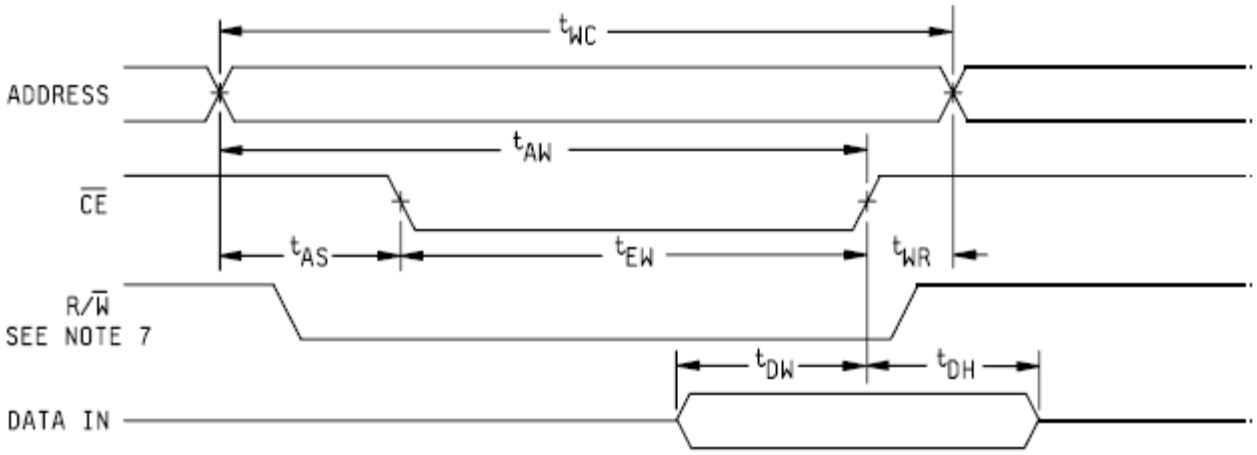
Notes:

1. R/$\overline{W}$ is high for read cycles
2. Device is continuously enabled; $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to, or coincident, with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.

Write Cycle 1 R/$\overline{W}$ Controlled (notes 1 thru 4 & 6 thru 8)



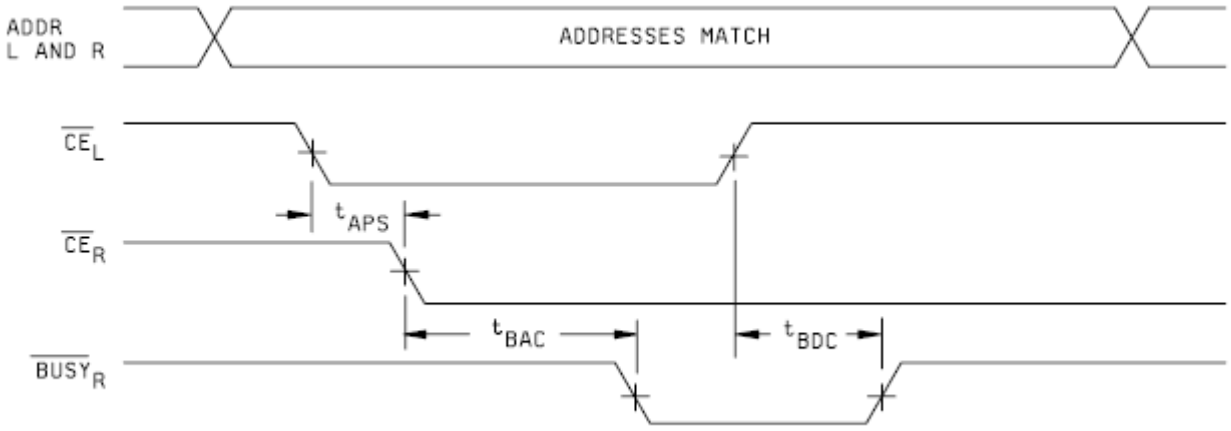
Write Cycle 2 $\overline{CE}$ Controlled (notes 1,2,3,5,7)



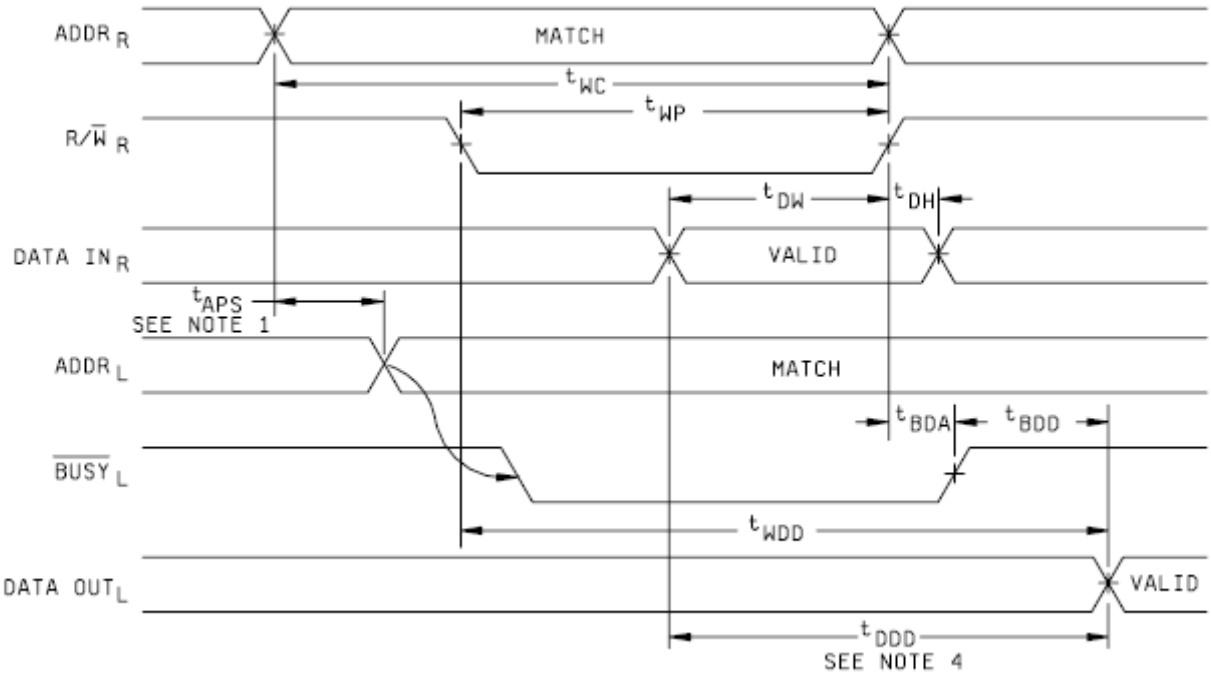
NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
7. R/$\overline{W}$ for either upper or lower byte.
8. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig).

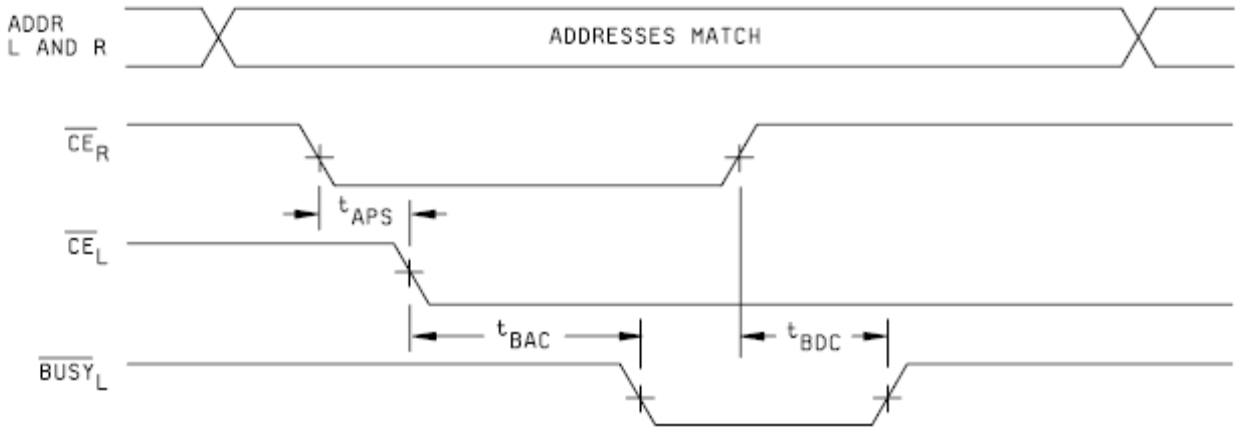
Read Cycle $\overline{BUSY}$ - Controlled by $\overline{CE}$ (notes 1,2,3,)



$\overline{\text{BUSY}}$ Cycle1 $\overline{\text{CE}}$ Arbitration ($\overline{\text{CE}}_L$ first)

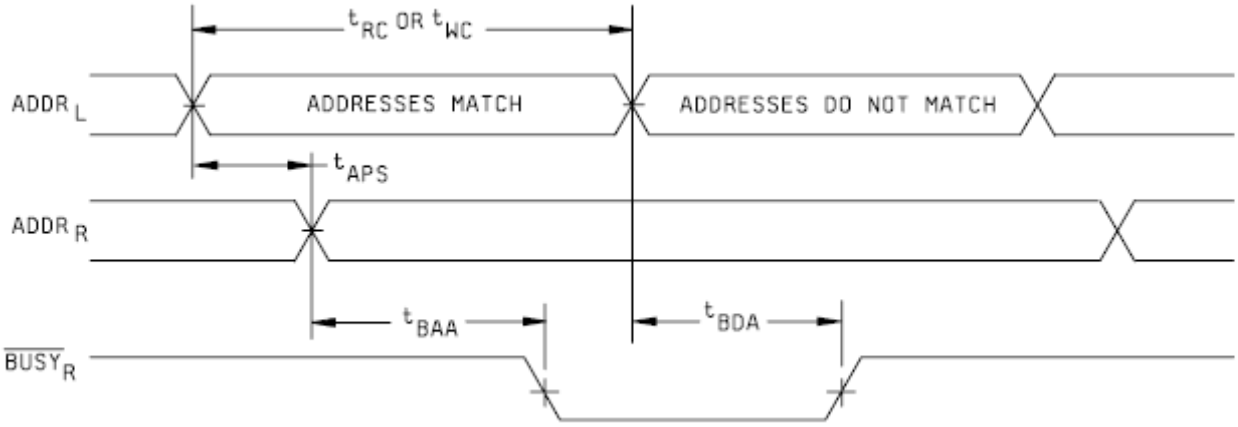


$\overline{\text{BUSY}}$ Cycle1 $\overline{\text{CE}}$ Arbitration ($\overline{\text{CE}}_R$ first)



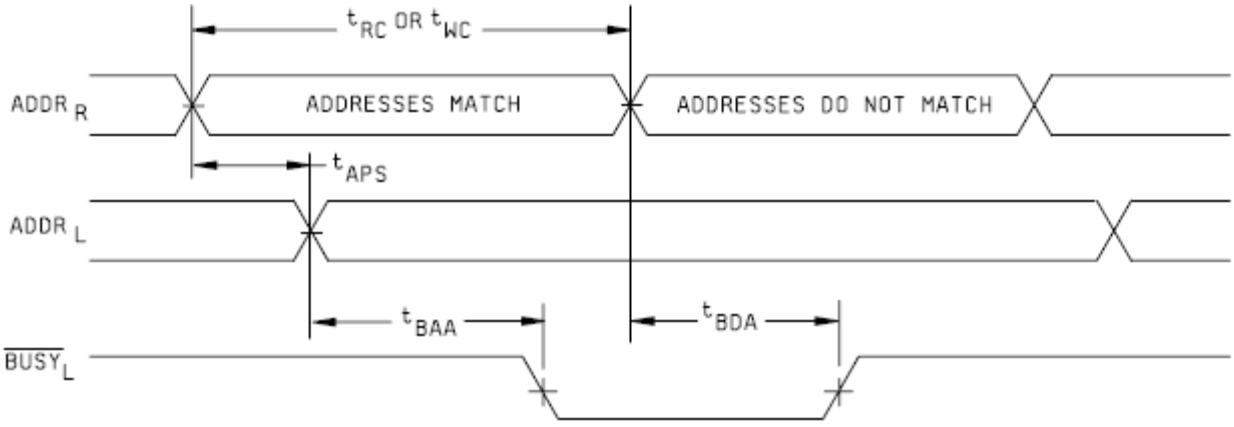
$\overline{\text{BUSY}}$ Cycle2 $\overline{\text{CE}}$ Arbitration (left address valid first)

Address valid arbitration ($\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$)



$\overline{\text{BUSY}}$ Cycle2 $\overline{\text{CE}}$ Arbitration (right address valid first)

Address valid arbitration ($\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$)



Truth Table: Non-contention read write control

Outputs						
R $\overline{W}_{LB}$	R $\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Mode
X	X	H	X	High-Z	High-Z	Port disabled; in power down mode (I_{CC3} I_{CC5})
X	X	H	X	High-Z	High-Z	$\overline{CE}_R$ or $\overline{CE}_L$ = H, power down mode, (I_{CC2} I_{CC3})
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on lower byte and upper byte written /4
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on lower byte written into memory /4 Data in memory output on upper byte /5
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in memory output on lower byte /5 Data on upper byte written into memory /4
L	H	L	H	$DATA_{IN}$	High-Z	Data on lower byte written in memory /4
H	L	L	H	High-Z	$DATA_{IN}$	Data on upper byte written in memory /4
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in memory output on upper byte and lower byte /5
H	H	L	H	High-Z	High-Z	Outputs Disabled

/1 H = high L= low, X = don't care, Z = high impedance, LB = lower byte, UB = upper byte
/2 Read/Write controls are separate for independent left and right address ports (A_{0L} – A_{10L} and A_{0R} – A_{10R})

/4 If $\overline{BUSY}$ = L, data not written

/5 If $\overline{BUSY}$ = L, data may not be valid. See t_{WDD} and t_{DDD} timing. written

Truth Table: Address $\overline{BUSY}$ Arbitration

Inputs			Ouputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L} – A_{10L} A_{0R} – A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	/1	/1	Write Inhibit /2

/1 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = V_{IL} will result $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be Low simultaneously.

/2 Writes to the left port or right port are internally ignored when $\overline{BUSY}_L$ or $\overline{BUSY}_R$ outputs are driving low, respectively.

Ordering Information

Part Nuber	Package (il-Std-1835)	Generic
5962-8866503ZA	CGA3-PN	QP7133LA70GB
5962-8866503UA	CQFP68 –See Note 2	QP7133LA70FB
5962-8866505ZA	CGA3-PN	QP7133LA55GB
5962-8866505UA	CQFP68 –See Note 2	QP7133LA55FB
5962-8866509ZA	CGA3-PN	QP7133LA70GB
5962-8866509UA	CQFP68 –See Note 2	QP7133LA70FB
5962-8866511ZA	CGA3-PN	QP7133LA55GB
5962-8866511UA	CQFP68 –See Note 2	QP7133LA55FB
5962-8866513ZA	CGA3-PN	QP7133LA45GB
5962-8866513UA	CQFP68 –See Note 2	QP7133LA45FB
5962-8866515ZA	CGA3-PN	QP7133LA35GB
5962-8866515UA	CQFP68 –See Note 2	QP7133LA35FB
5962-8861001ZA	CGA3-PN	QP7133SA90GB
5962-8861001UA	CQFP68 –See Note 2	QP7133SA90FB
5962-8861003ZA	CGA3-PN	QP7133SA70GB
5962-8861003UA	CQFP68 –See Note 2	QP7133SA70FB
5962-8861005ZA	CGA3-PN	QP7133SA55GB
5962-8861005UA	CQFP68 –See Note 2	QP7133SA55FB
5962-8861007ZA	CGA3-PN	QP7133SA90GB
5962-8861007UA	CQFP68 –See Note 2	QP7133SA90FB
5962-8861009ZA	CGA3-PN	QP7133SA70GB
5962-8861009UA	CQFP68 –See Note 2	QP7133SA70FB
5962-8861011ZA	CGA3-PN	QP7133SA55GB
5962-8861011UA	CQFP68 –See Note 2	QP7133SA55FB

Notes:

1. Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.
2. Reference Fig 1 of SMD 5962-88610 for CQFP68 case outline.
3. QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.
4. The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/
5. Additional information is available at our website http://www.qpsemi.com

Document Revision History

Date	Revision Level	Description
04 Aug 2010	0	Initial release