

## 54F/74F378 Parallel D Register with Enable

### General Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

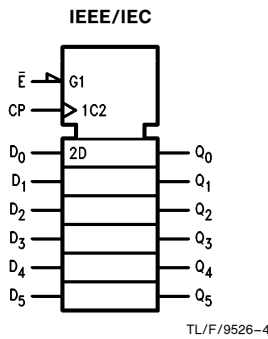
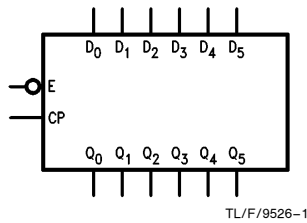
### Features

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Full TTL and CMOS compatible

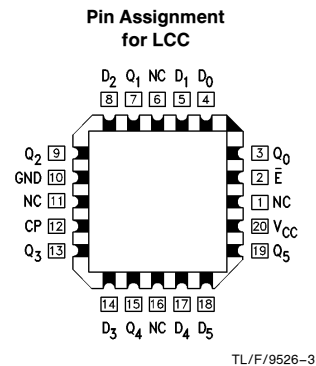
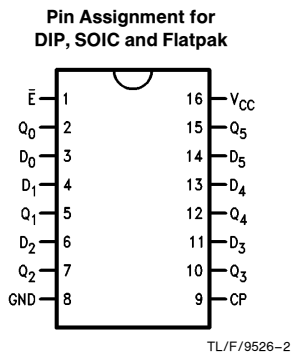
Commercial	Military	Package Number	Package Description
74F378PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F378DM (QB)	J16A	16-Lead Ceramic Dual-In-Line
74F378SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F378SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F378FM (QB)	W16A	16-Lead Cerpack
	54F378LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

### Logic Symbols



### Connection Diagrams



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## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$D_0$ - $D_5$	Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0$ - $Q_5$	Outputs	50/33.3	-1 mA/20 mA

## Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops.

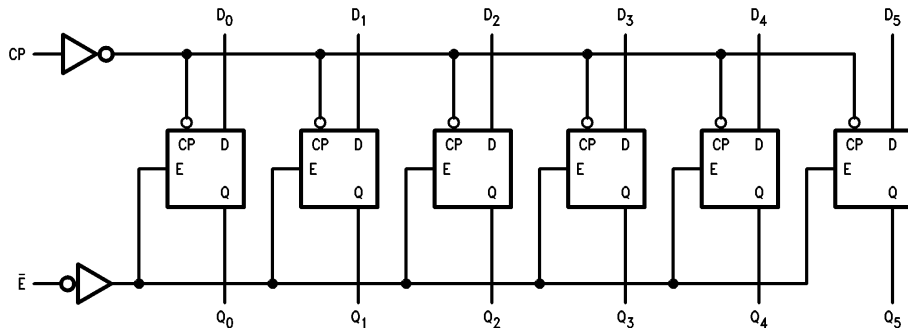
When the  $\bar{E}$  input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the  $\bar{E}$  input is HIGH the register will retain the present data independent of the CP input.

## Truth Table

Inputs			Output
$\bar{E}$	CP	$D_n$	$Q_n$
H	—	X	No Change
L	↗	H	H
L	↘	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition

## Logic Diagram



TL/F/9526-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>		2.5 2.5 2.7	V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		30	45	mA	Max	V <sub>O</sub> = LOW

## AC Electrical Characteristics

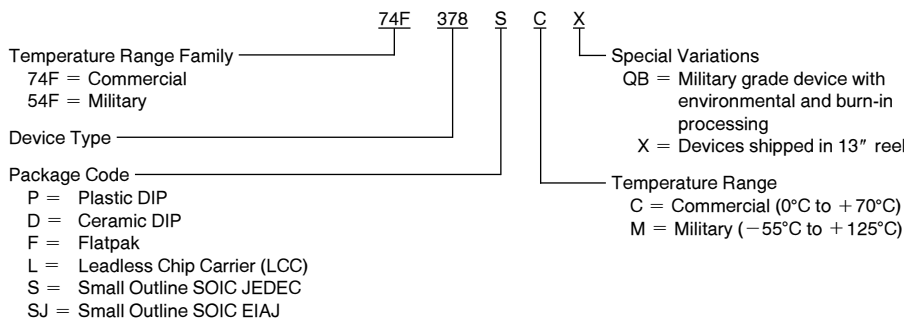
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Input Frequency	80	100		70		80		MHz
t <sub>PLH</sub>	Propagation Delay	3.0	5.5	7.5	3.0	10.0	3.0	8.5	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub>	3.5	6.0	8.5	3.5	10.5	3.5	9.5	

## AC Operating Requirements

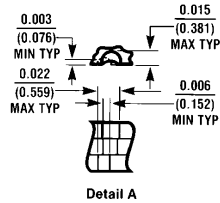
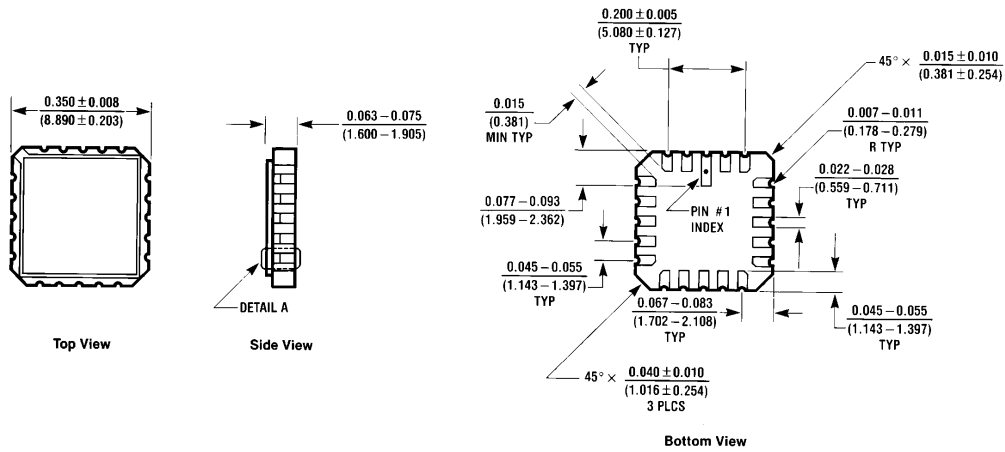
Symbol	Parameter	74F		54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		
		Min	Max	Min	Max	Min	Max	
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	4.0		5.0		4.0		ns
t <sub>s</sub> (L)	D <sub>n</sub> to CP	4.0		5.0		4.0		
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		2.0		0		ns
t <sub>h</sub> (L)	D <sub>n</sub> to CP	0		2.0		0		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	6.0		4.5		6.0		ns
t <sub>s</sub> (L)	E to CP	10.0		13.0		10.0		
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	0		0		0		ns
t <sub>h</sub> (L)	E to CP	0		0		0		
t <sub>w</sub> (H)	CP Pulse Width	4.0		5.0		4.0		ns
t <sub>w</sub> (L)	HIGH or LOW	6.0		7.5		6.0		

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

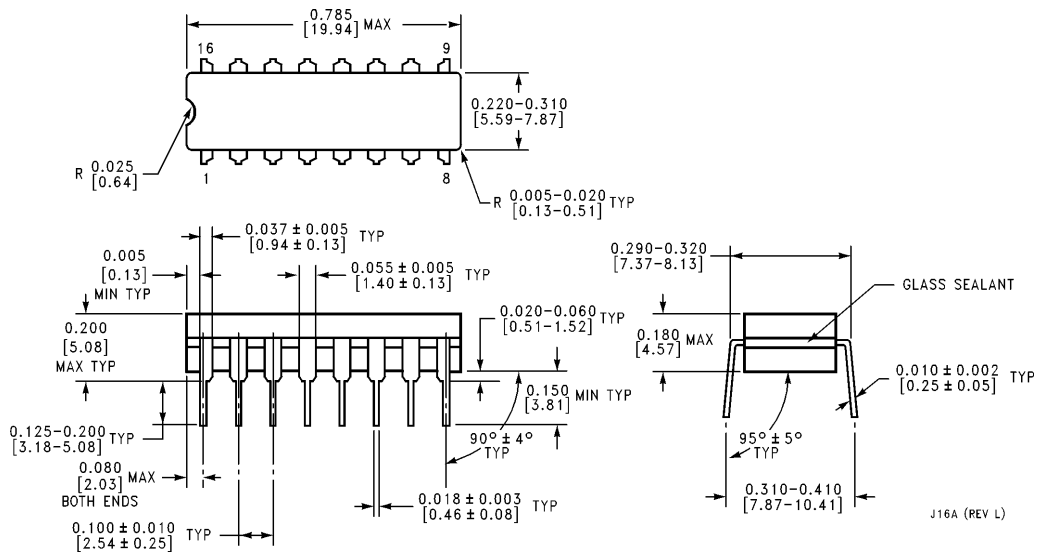


**Physical Dimensions** inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)**  
**NS Package Number E20A**

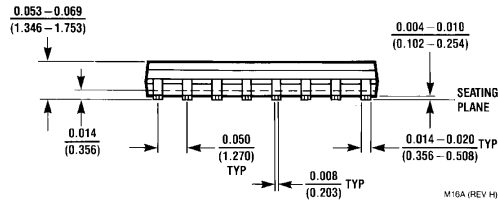
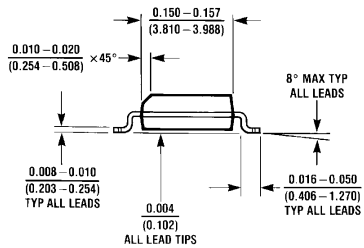
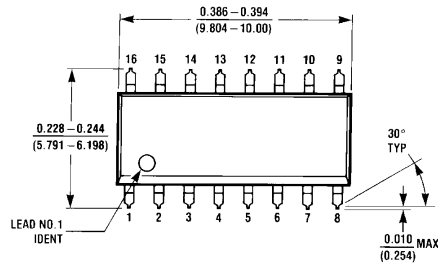
E20A (REV D)



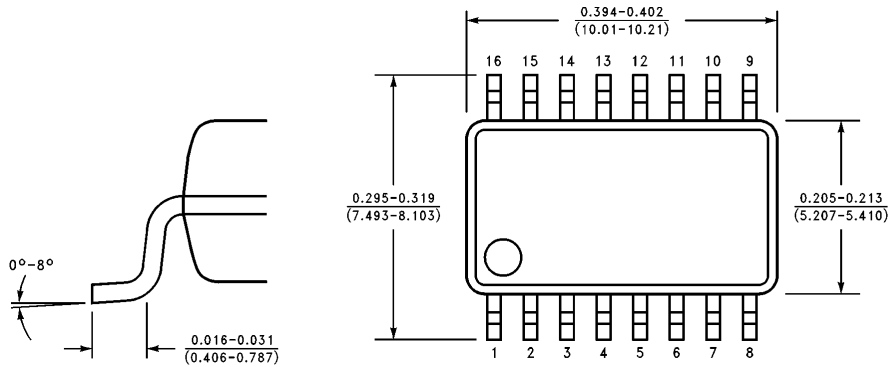
**16-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J16A**

J16A (REV L)

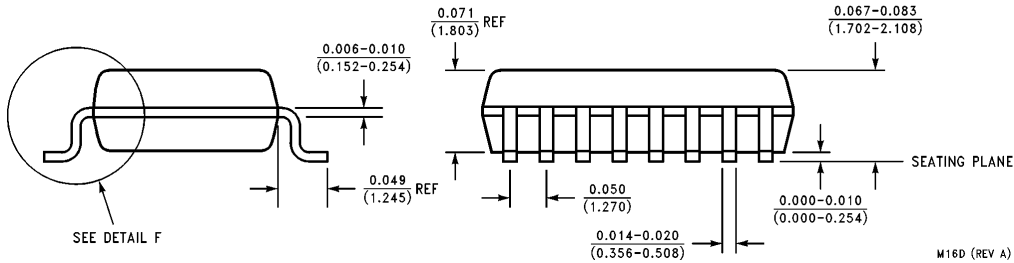
**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC  
NS Package Number M16A**

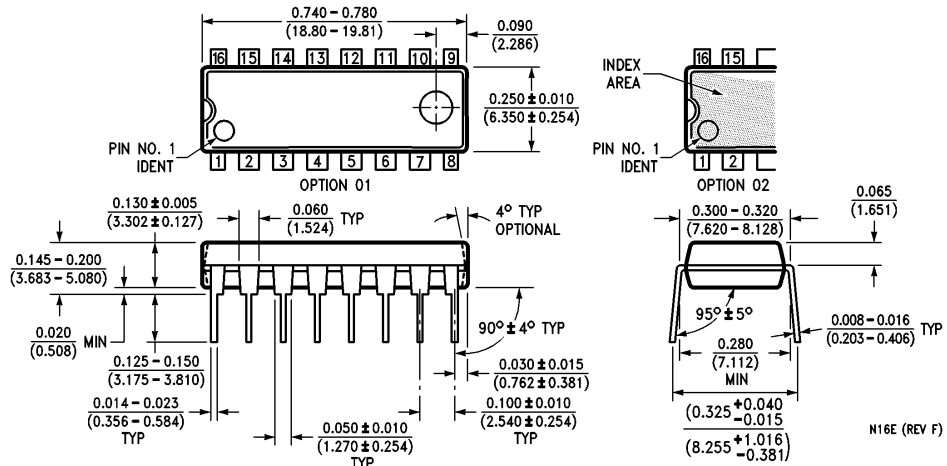


**DETAIL F**



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
NS Package Number M16D**

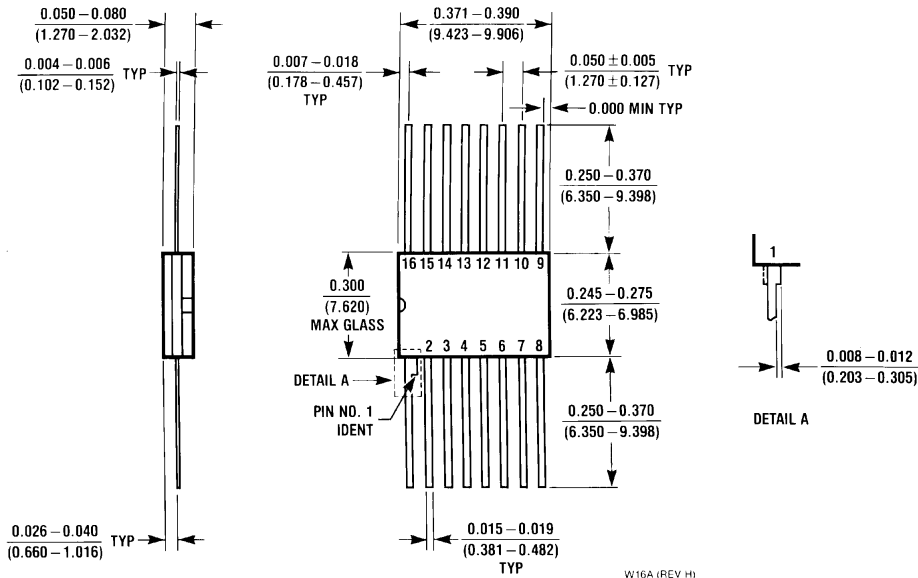
**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
**NS Package Number N16E**

N16E (REV F)

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)  
NS Package Number W16A**

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**National Semiconductor Corporation**  
2900 Semiconductor Drive  
P.O. Box 58090  
Santa Clara, CA 95052-8090  
Tel: (1800) 272-9959  
TWX: (910) 339-9240

**National Semiconductor GmbH**  
Livry-Gargan-Str. 10  
D-82256 Fürstenfeldbruck  
Germany  
Tel: (81-41) 35-0  
Telex: 527849  
Fax: (81-41) 35-1

**National Semiconductor Japan Ltd.**  
Sumitomo Chemical  
Engineering Center  
Bldg. 7F  
1-7-1, Nakase, Mihama-Ku  
Chiba-City,  
Ciba Prefecture 261  
Tel: (043) 299-2300  
Fax: (043) 299-2500

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semicondutores Do Brazil Ltda.**  
Rue Deputado Lacorda Franco  
120-3A  
Sao Paulo-SP  
Brazil 05418-000  
Tel: (55-11) 212-5066  
Telex: 391-1131931 NSBR BR  
Fax: (55-11) 212-1181

**National Semiconductor (Australia) Pty. Ltd.**  
Building 16  
Business Park Drive  
Monash Business Park  
Nottingham, Melbourne  
Victoria 3168 Australia  
Tel: (3) 558-9999  
Fax: (3) 558-9998

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