

54F/74F377 Octal D Flip-Flop with Clock Enable

General Description

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

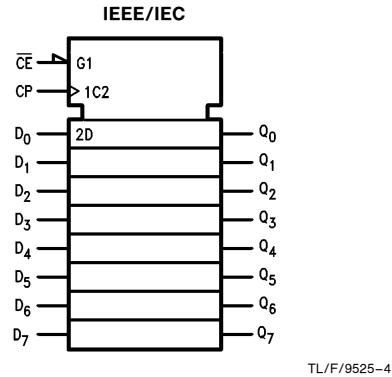
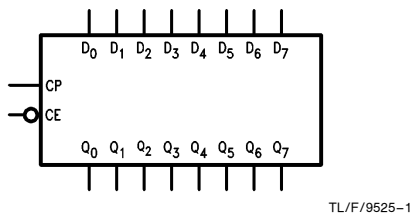
Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for master reset version
- See 'F373 for transparent latch version
- See 'F374 for TRI-STATE® version
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F377PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F377DM (QB)	J20A	20-Lead Ceramic Dual-In-Line
74F377SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F377SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F377FM (QB)	W20A	20-Lead Cerpack
	54F377LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

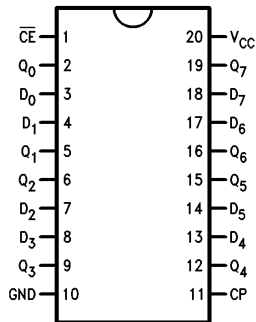
Logic Symbols



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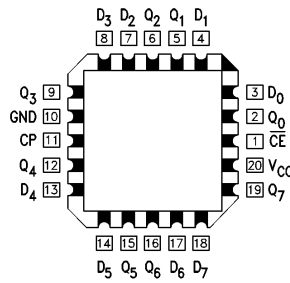
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/9525-2

Pin Assignment
for LCC



TL/F/9525-3

Unit Loading/Fan Out

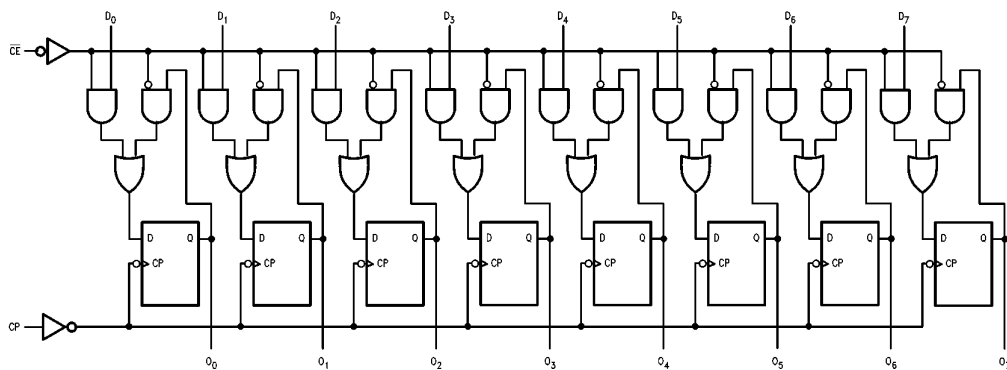
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_7	Data Inputs	1.0/1.0	20 μA / -0.6 mA
\overline{CE}	Clock Enable (Active LOW)	1.0/1.0	20 μA / -0.6 mA
CP	Clock Pulse Input	1.0/1.0	20 μA / -0.6 mA
Q_0-Q_7	Data Outputs	50/33.3	-1 mA / 20 mA

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	\overline{CE}	D_n	Q_n
Load "1"	↗	l	h	H
Load "0"	↘	l	l	L
Hold (Do Nothing)	↗	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9525-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V


Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			
I _{IH}	Input HIGH Current				μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test				μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current				mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CEx}	Output HIGH Leakage Current				μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current				μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{CCCH} I _{CCCL}	Power Supply Current		35 44	46 56	mA	Max	CP =  D _n = MR = HIGH

AC Electrical Characteristics

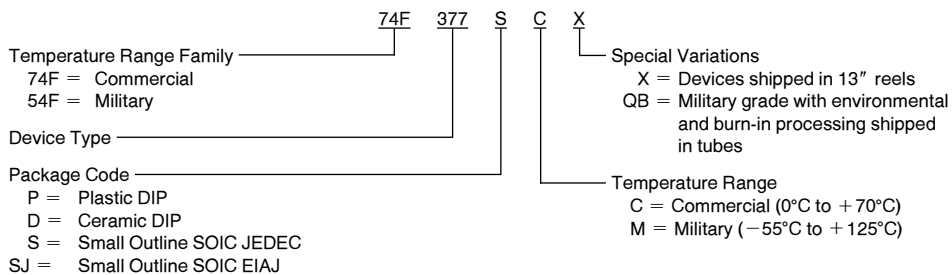
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{Max}	Maximum Clock Frequency	130			85		105		MHz
t _{PLH}	Propagation Delay	3.0			2.0		2.5		ns
t _{PHL}	CP to Q _n	4.0			3.0		3.5		

AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns
t _s (L)	D _n to CP	3.5		4.0		3.5		
t _h (H)	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns
t _h (L)	D _n to CP	1.0		1.0		1.0		
t _s (H)	Setup Time, HIGH or LOW	4.1		4.0		4.1		ns
t _s (L)	CE to CP	3.5		5.0		4.0		
t _h (H)	Hold Time, HIGH to LOW	0.5		1.5		0.5		ns
t _h (L)	\overline{CE} to CP	2.0		2.5		2.0		
t _w (H)	Clock Pulse Width,	6.0		5.0		6.0		ns
t _w (L)	HIGH or LOW	6.0		5.0		6.0		

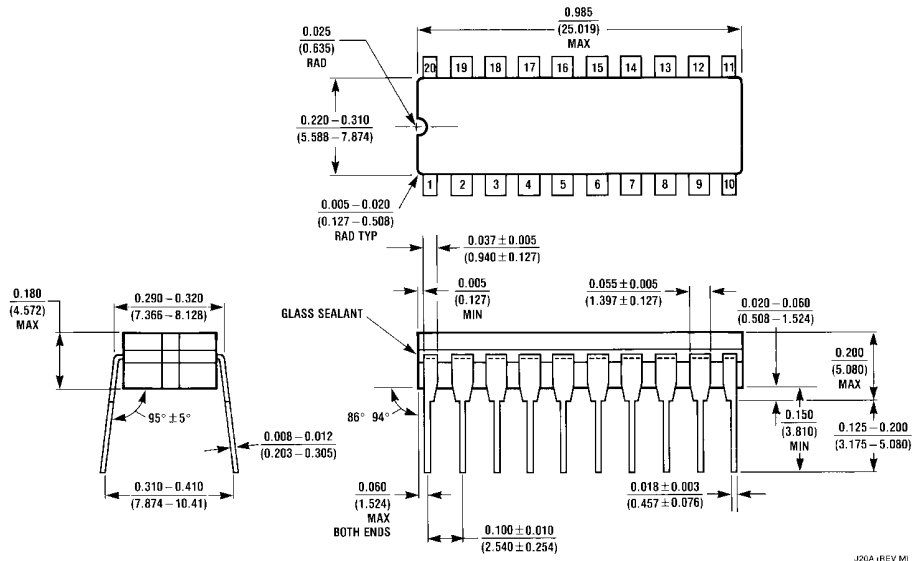
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

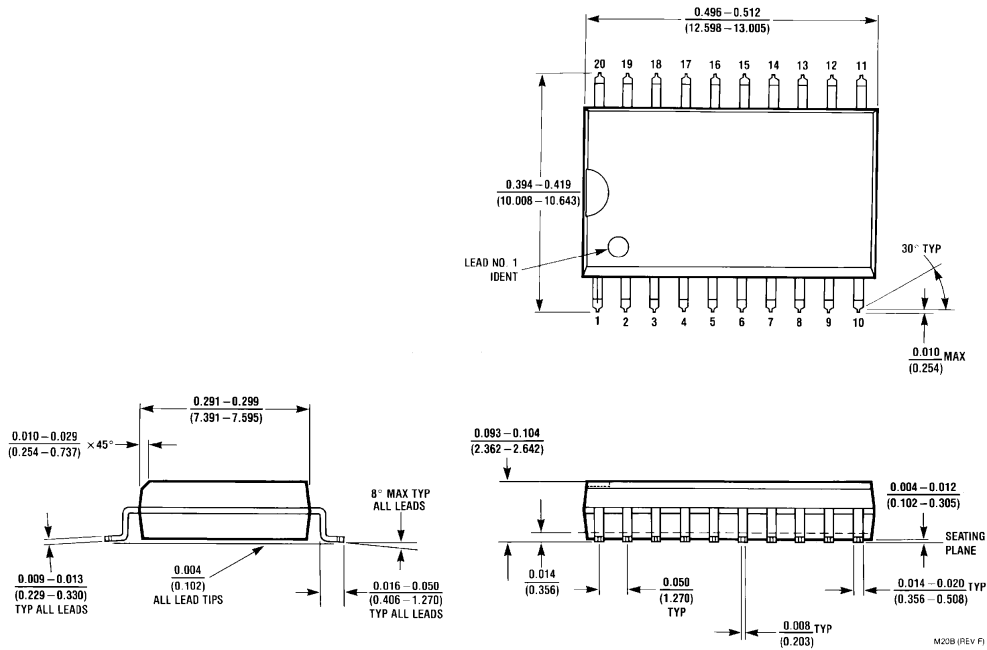




Physical Dimensions inches (millimeters)

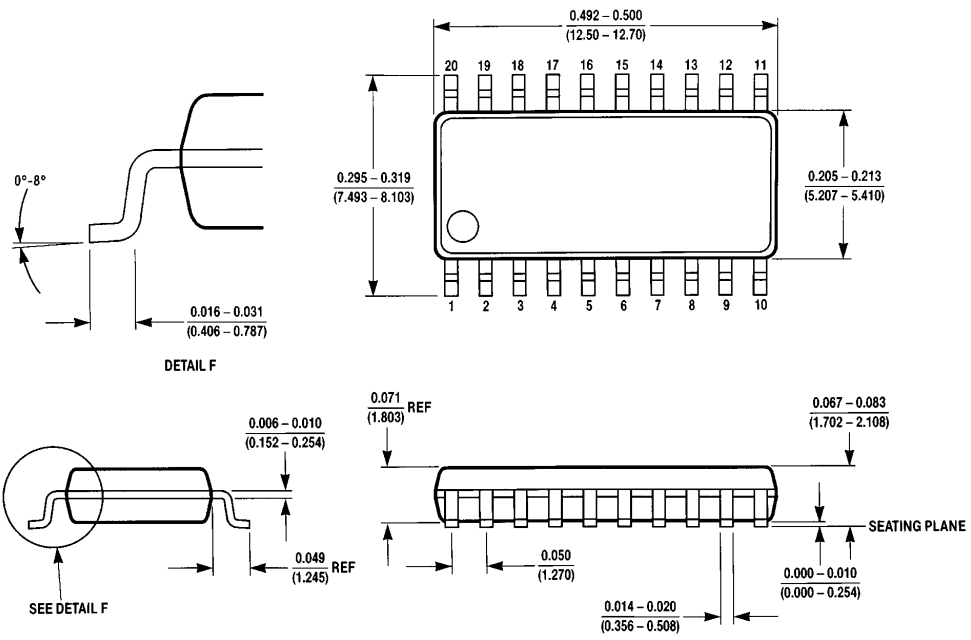


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

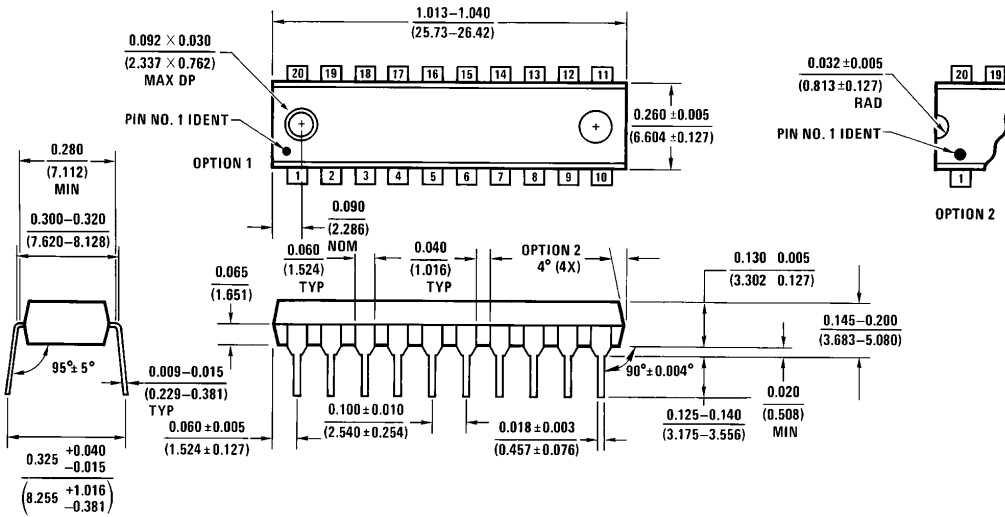
Physical Dimensions inches (millimeters) (Continued)



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D**

M20D (REV A)

Physical Dimensions inches (millimeters) (Continued)



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A**

N20A (REV G)

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