

# 54ACTQ821

## Quiet Series 10-Bit D Flip-Flop with TRI-STATE® Outputs

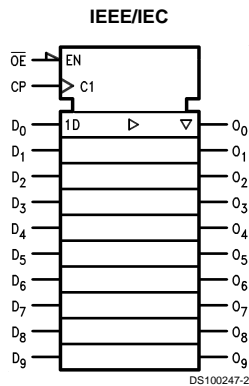
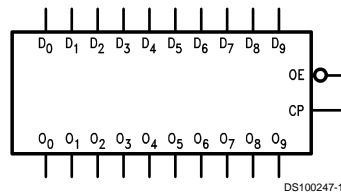
### General Description

The ACTQ821 is a 10-bit D flip-flop with non-inverting TRI-STATE outputs arranged in a broadside pinout. The ACTQ821 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### Features

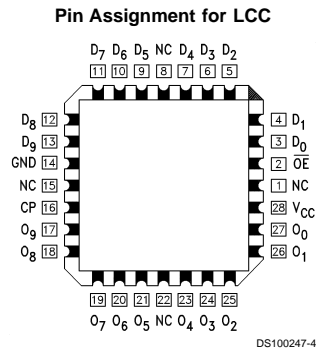
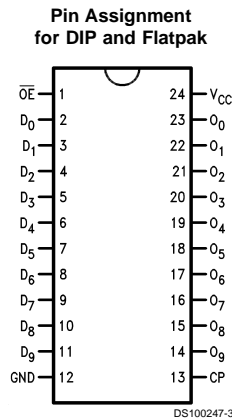
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Non-inverting TRI-STATE outputs for bus interfacing
- 4 kV minimum ESD immunity
- Outputs source/sink 24 mA
- Functionally identical to the AM29821

### Logic Symbols



Pin Names	Description
D <sub>0</sub> -D <sub>9</sub>	Data Inputs
O <sub>0</sub> -O <sub>9</sub>	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

### Connection Diagrams



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## Functional Description

The ACTQ821 consists of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}$  LOW the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

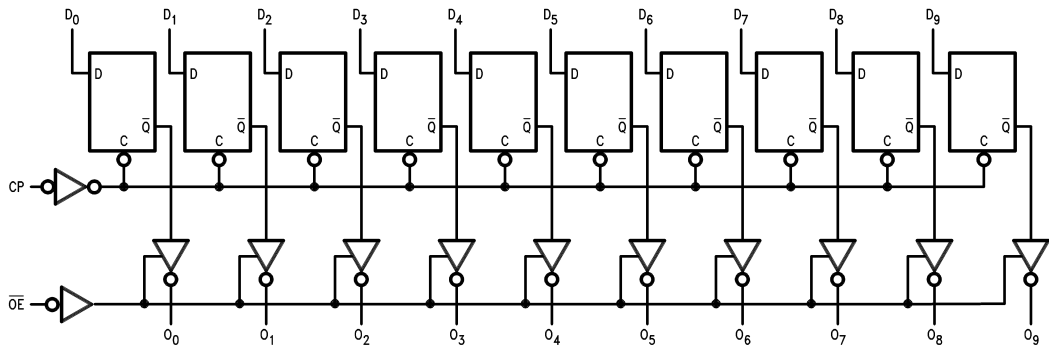
The ACTQ821 is functionally and pin compatible with the AM29821.

## Function Table

$\overline{OE}$	Inputs		Internal	Outputs	Function
	CP	D	Q	O	
H	↗	L	L	Z	High Z
H	↗	H	H	Z	High Z
L	↗	L	L	L	Load
L	↗	H	H	H	Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = HIGH Impedance  
 ↗ = LOW-to-HIGH Clock Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100247-5

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current	
per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

DC Latch-Up Source	
or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

## DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACTQ	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.70		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, \text{ GND}$
$I_{OZ}$	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{ GND}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	(Note 4) Minimum Dynamic Output Current	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$		5.5	-50	mA	$V_{OHD} = 3.85V \text{ Min}$

## DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	160.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 5)
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0			V	(Notes 6, 7)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0			V	(Notes 6, 7)

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 6:** Plastic DIP package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

**Note 8:** Maximum number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 9)	54ACTQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	95		MHz	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	2.5	11.5	ns	
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time OE to O <sub>n</sub>	5.0	2.5	13.0	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time OE to O <sub>n</sub>	5.0	1.0	9.0	ns	

**Note 9:** Voltage Range 5.0 is 5.0V ±0.5V

**Note 10:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design. Not tested.

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 11)	54ACTQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	3.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	2.0		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	4.0		ns	

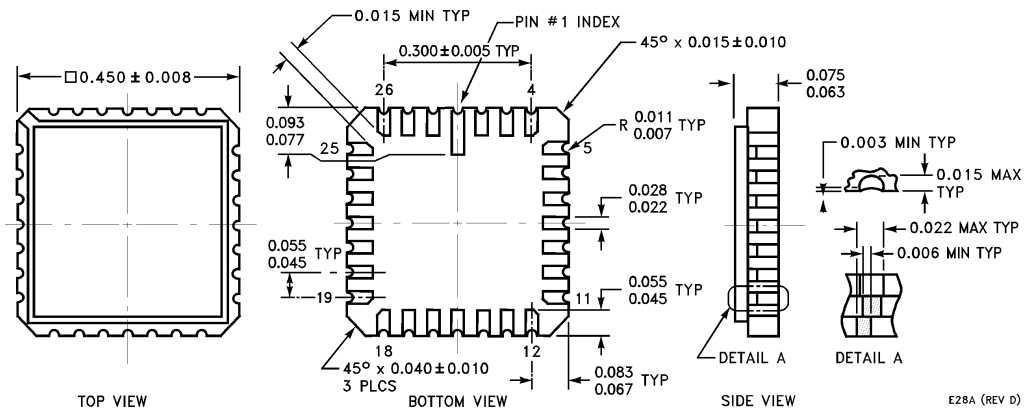
**Note 11:** Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

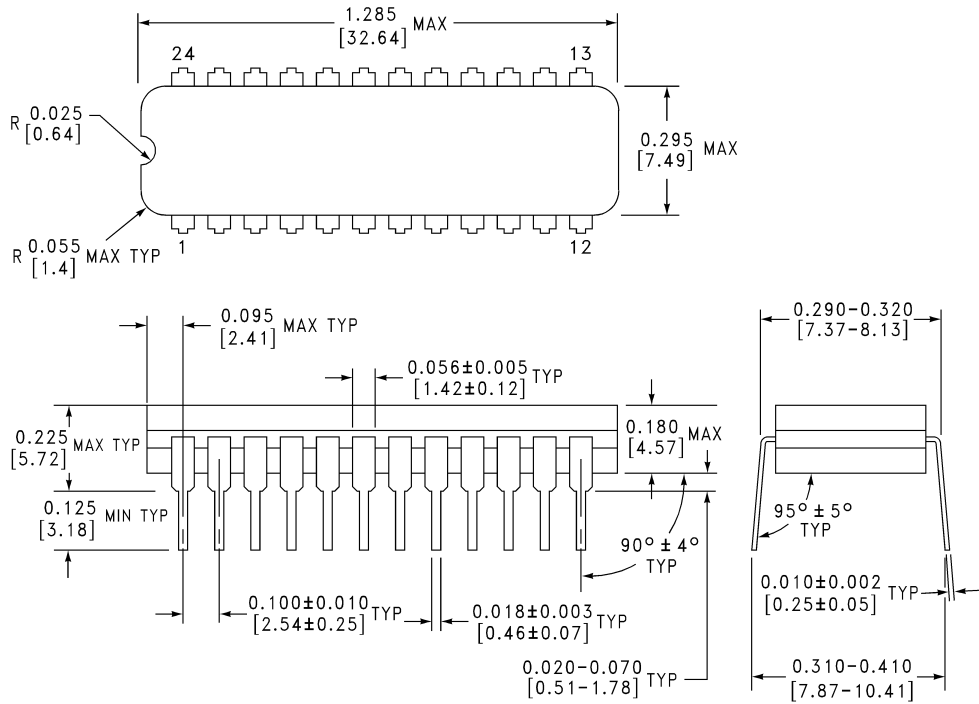
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	55.0	pF	V <sub>CC</sub> = 5.0V



**Physical Dimensions** inches (millimeters) unless otherwise noted

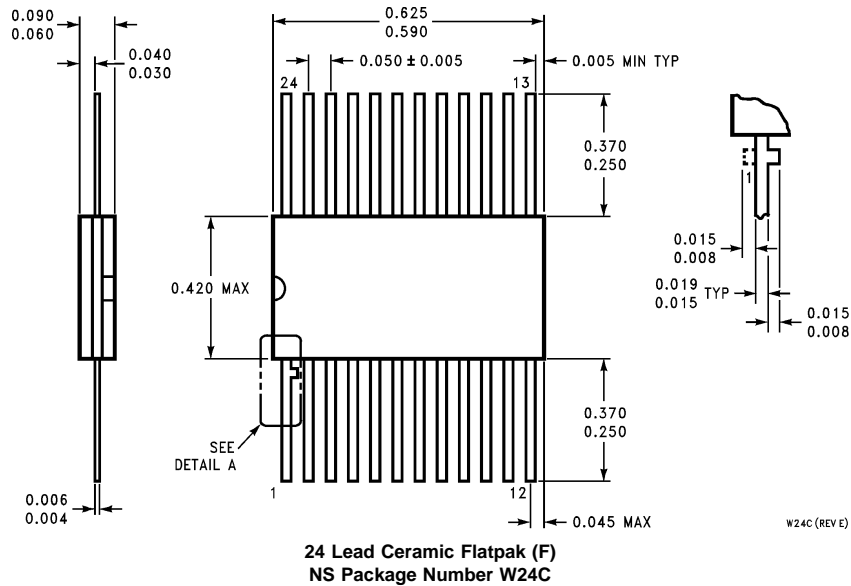


**28 Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E28A



**24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)**  
NS Package Number J24F

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
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