National Semiconductor

September 1998

54ACT564
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

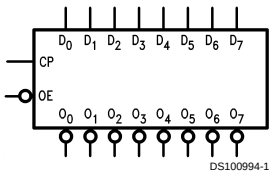
The 'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'ACT564 is functionally identical to the 'ACT574, but with inverted outputs.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT574 but with inverted outputs
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT564 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD) 5962-89557

Logic Symbols



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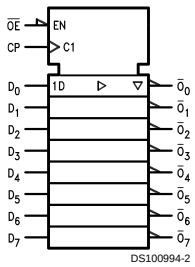
IEEE/IEC



DS100994-2

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

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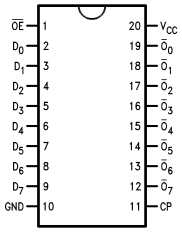
FACT™ is a trademark of Fairchild Semiconductor Corporation.

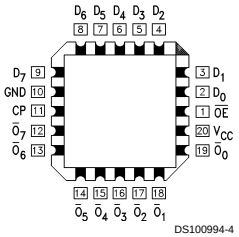
Connection Diagrams

Pin Assignment for DIP, and Flatpak



DS100994-3

Pin Assignment for LCC



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Functional Description

The'ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complement outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the complement of the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	H	Data Available
L	N	H	H	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
N = LOW-to-HIGH Transition
NC = No Change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified) (ACT)	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V
		5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V
		5.5	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.4	V	I_{OUT} = −50 μA
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} −24 mA
		5.5	4.70		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 μA
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±10.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices (Continued)

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V) (Note 4)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	65		ns
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	12.5	ns
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	11.5	ns
t_{PZH}	Output Enable Time	5.0	1.0	10.5	ns
t_{PZL}	Output Enable Time	5.0	1.0	10.5	ns
t_{PHZ}	Output Disable Time	5.0	1.0	12.5	ns
t_{PLZ}	Output Disable Time	5.0	1.0	9.5	ns

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

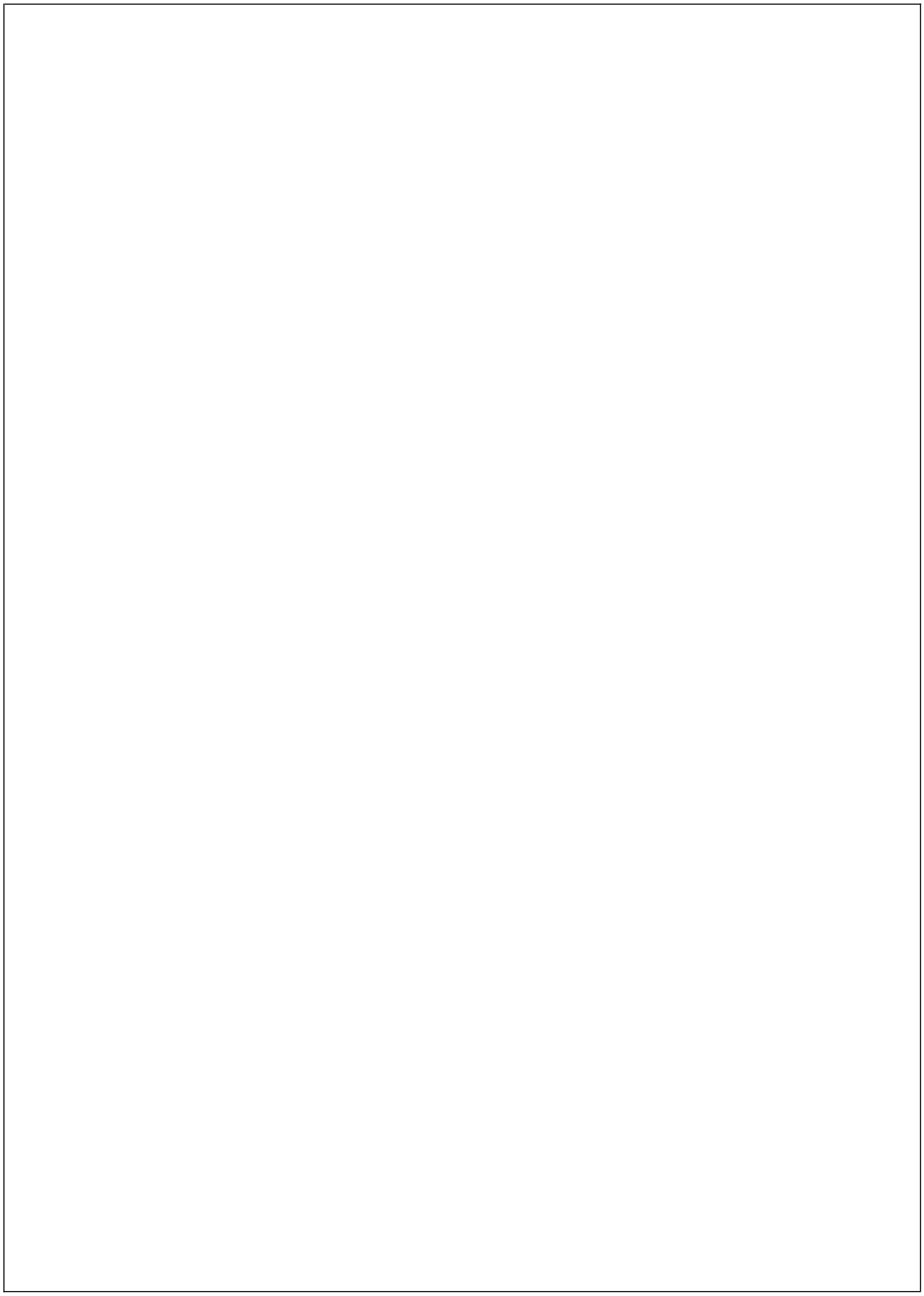
AC Operating Requirements for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V) (Note 5)	54ACT $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF	Units
			Guaranteed Minimum	
t_s	Set-Up Time, HIGH or LOW D_n to CP	5.0	3.5	ns
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	2.5	ns
t_w	CP Pulse Width HIGH or LOW	5.0	5.0	ns

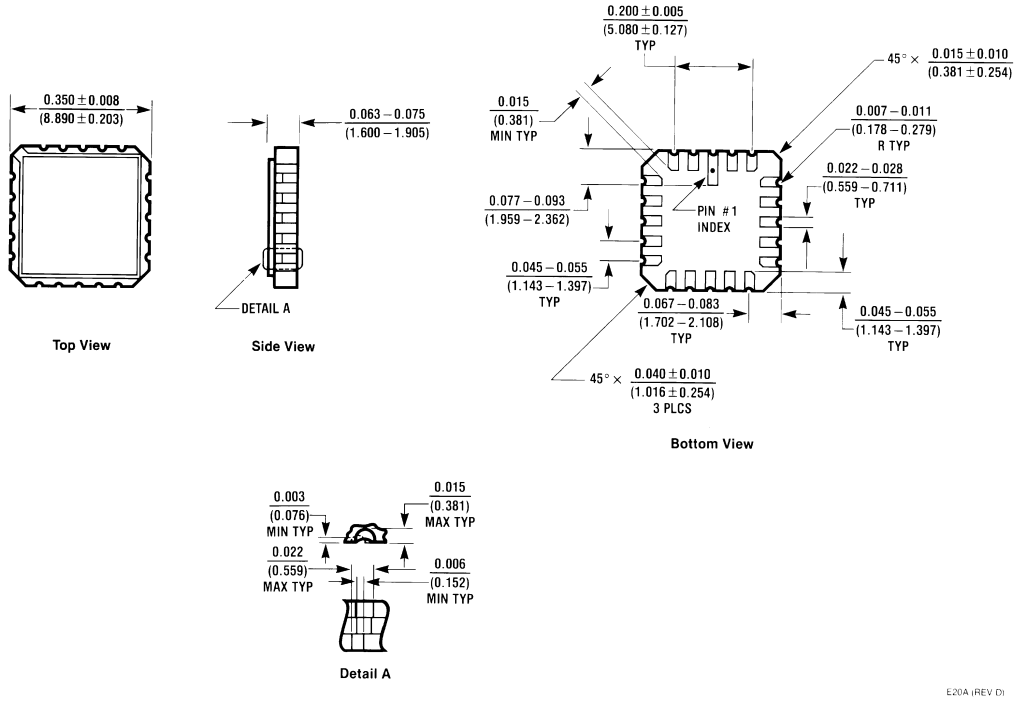
Note 5: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

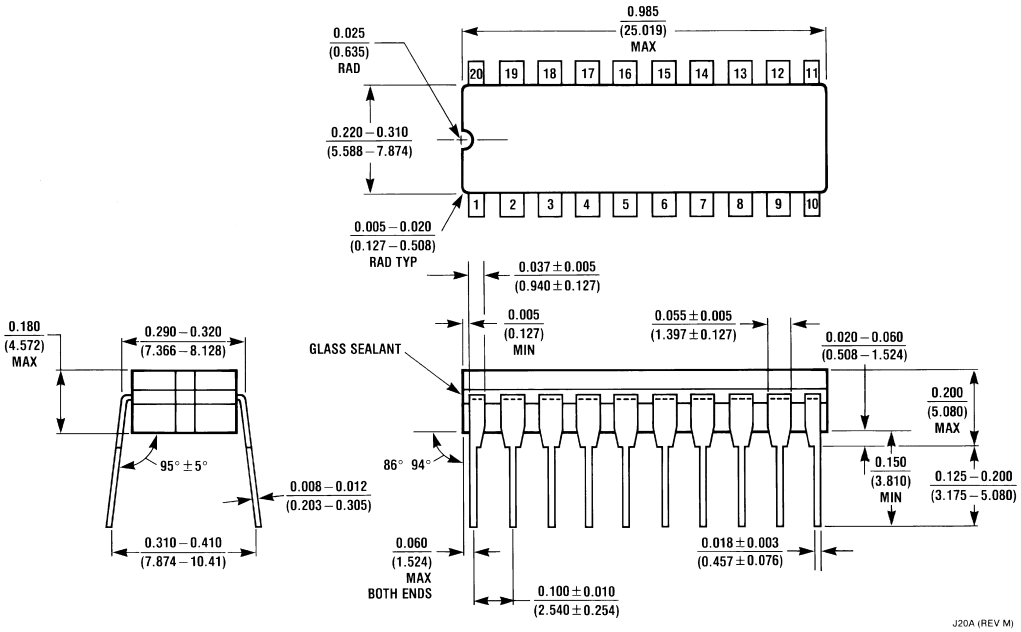


Physical Dimensions inches (millimeters) unless otherwise noted

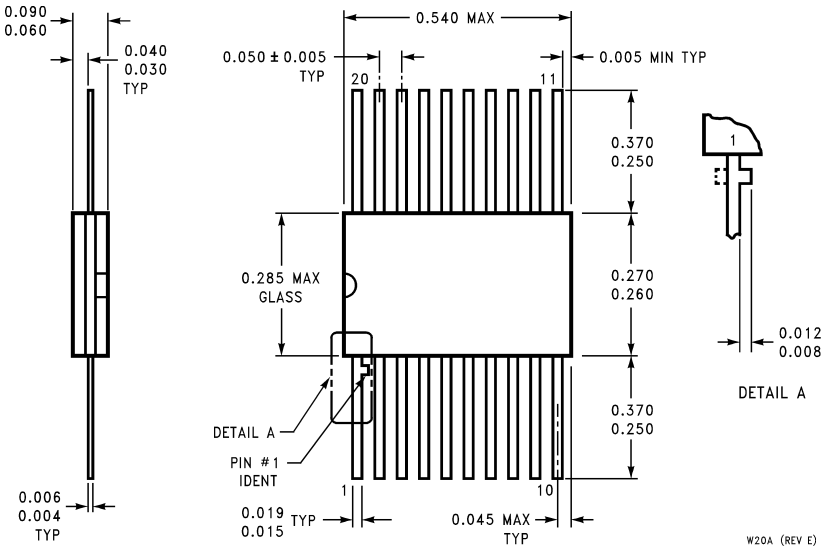


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20 Lead Ceramic Flatpak (F)
NS Package Number W20A

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