

## 54ACQ240 • 54ACTQ240

### Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

#### General Description

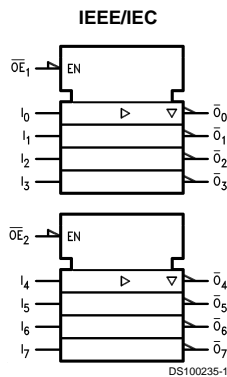
The 'ACQ/'ACTQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT240
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD)  
'ACTQ240: 5962-92184

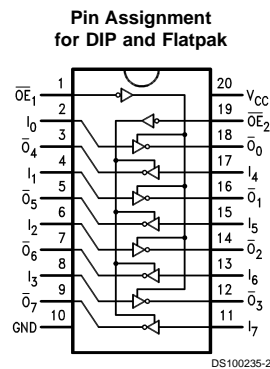
#### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%

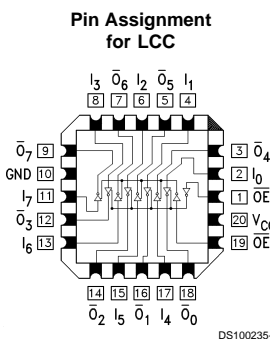
#### Logic Symbol



#### Connection Diagrams



Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs



GTO™ is a trademark of National Semiconductor Corporation.  
 TRI-STATE® is a registered trademark of National Semiconductor Corporation.  
 FACT® is a registered trademark of Fairchild Semiconductor Corporation.  
 FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

## Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature ( $T_J$ )	
CDIP	175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACQ/ACTQ	-55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACQ Devices	
$V_{IN}$ from 30% to 70% of $V_{CC}$	
$V_{CC}$ @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

**Note 2:** All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

## DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACQ	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	3.15		
		5.5	3.85		
$V_{IL}$	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.35		
		5.5	1.65		
$V_{OH}$	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.4		
		5.5	5.4		
		3.0	2.4	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		4.5	3.7		
		5.5	4.7		
$V_{OL}$	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.1		
		5.5	0.1		
		3.0	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		4.5	0.50		
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, GND$ (Note 5)

## DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACQ	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
I <sub>OLD</sub>	Minimum Dynamic (Note 4)	5.5	50	mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50	mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 5)
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5	±5.0	μA	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> V <sub>I</sub> = V <sub>CC</sub> , GND V <sub>O</sub> = V <sub>CC</sub> , GND
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5V	V	(Notes 6, 7)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2V	V	(Notes 6, 7)

**Note 3:** All outputs loaded; thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

**Note 6:** Plastic DIP package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

**Note 8:** Max number of data inputs (n) switching. (n - 1) inputs switching 0V to 5V (ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ	Units	Conditions
			T <sub>A</sub> = -55°C to +125°C		
			Guaranteed Limits		
V <sub>IH</sub>	Minimum High Level Input Voltage	4.5	2.0	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	4.5	0.8	V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V
		5.5	0.8		
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5	4.4	V	I <sub>OUT</sub> = -50 μA
		5.5	5.4		
		4.5	3.70	V	(Note 9) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -24 mA
		5.5	4.70		
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5	0.1	V	I <sub>OUT</sub> = 50 μA
		5.5	0.1		
		4.5	0.50	V	(Note 9) V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 24 mA
		5.5	0.50		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	±1.0	μA	V <sub>I</sub> = V <sub>CC</sub> , GND
I <sub>OZ</sub>	Maximum TRI-STATE Leakage Current	5.5	±5.0	μA	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> , GND

## DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	54ACTQ		Units	Conditions
			T <sub>A</sub> = -55°C to +125°C			
			Guaranteed Limits			
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	1.6		mA	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
I <sub>OLD</sub>	Minimum Dynamic (Note 10)	5.5	50		mA	V <sub>OLD</sub> = 1.65V Max
I <sub>OHD</sub>	Output Current	5.5	-50		mA	V <sub>OHD</sub> = 3.85V Min
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	80.0		μA	V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 11)
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	1.5V		V	(Notes 12, 13)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-1.2V		V	(Notes 12, 13)

**Note 9:** All outputs loaded; thresholds on input associated with output under test.

**Note 10:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 11:** I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

**Note 12:** Plastic DIP package.

**Note 13:** Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 3V. One Data Input @ V<sub>IN</sub> = GND.

**Note 14:** Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 15)	54ACQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	3.3	1.0	12.5	ns	
		5.0	1.0	9.0		
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	3.3	1.0	13.5	ns	
		5.0	1.0	10.0		
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	3.3	1.0	11.0	ns	
		5.0	1.0	9.0		

**Note 15:** Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3 ±0.3V.

**Note 16:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 17)	54ACTQ		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Data to Output	5.0	1.5	9.0	ns	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	5.0	1.5	11.0	ns	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	10.0	ns	

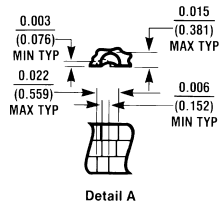
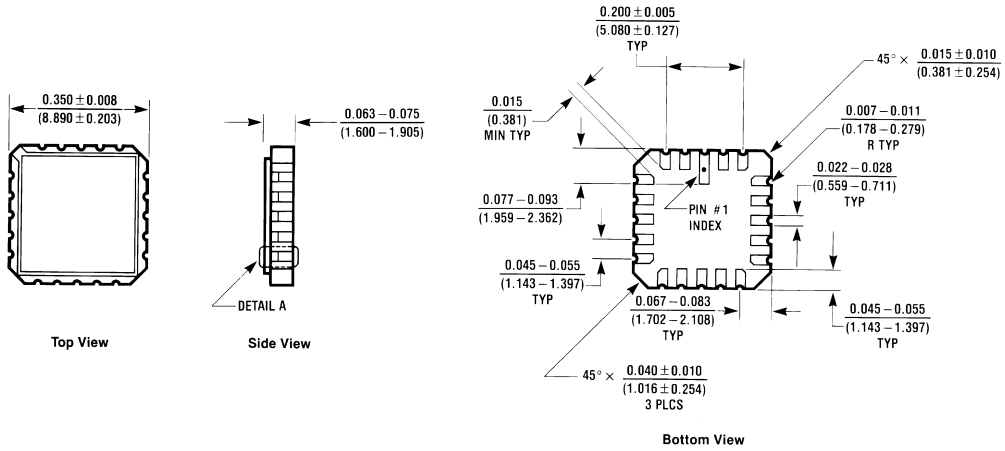
**Note 17:** Voltage Range 5.0 is 5.0V ±0.5V

**Note 18:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

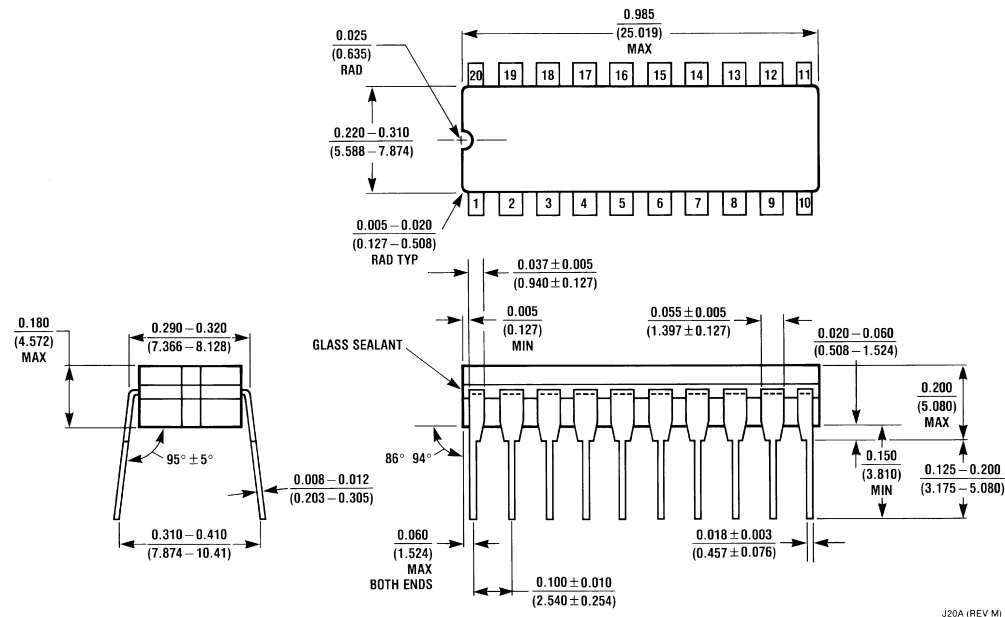
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	70	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E20A

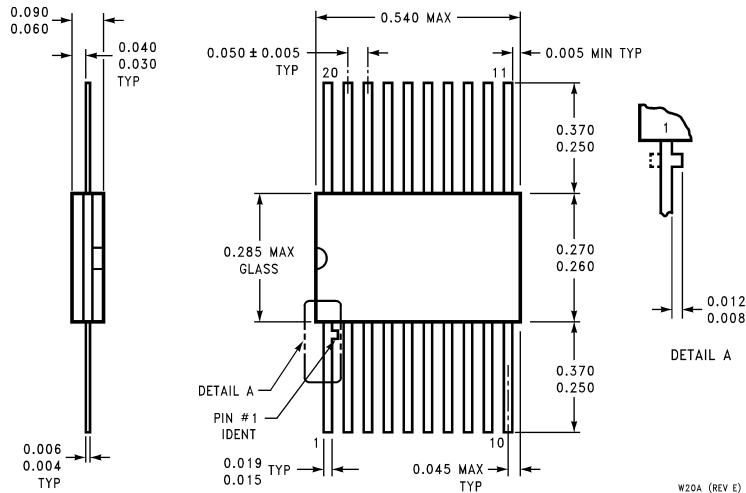
E20A (REV D)



**20-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507

www.national.com