National Semiconductor

July 1998

54ABT16646
16-Bit Transceivers and Registers with TRI-STATE® Outputs

General Description

The 'ABT16646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is Active LOW. In the isolation mode (control $\overline{OE}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

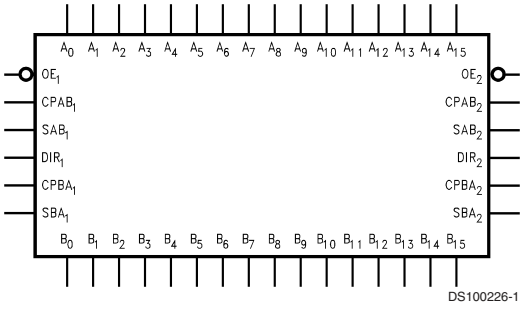
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9450202

Ordering Code

Military	Package Number	Package Description
54ABT16646W-QML	WA56A	56-Lead Cerpack

Logic Symbol



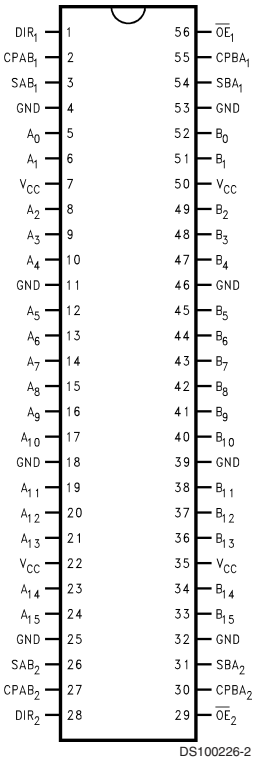
DS100226-1

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/ TRI-STATE Outputs
B_0–B_{15}	Data Register B Inputs/ TRI-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
SAB_n, SBA_n	Select Inputs
$\overline{OE}_n$	Output Enable Input
DIR	Direction Control Input

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

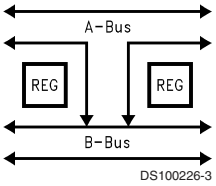
Connection Diagram

Pin Assignment for Cerpack



DS100226-2

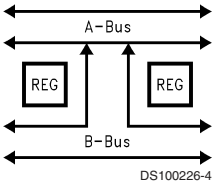
Real Time Transfer A-Bus to B-Bus



DS100226-3

FIGURE 1.

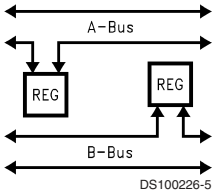
Real Time Transfer B-Bus to A-Bus



DS100226-4

FIGURE 2.

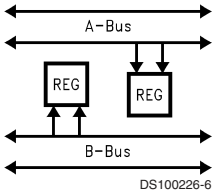
Storage from Bus to Register



DS100226-5

FIGURE 3.

Transfer from Register to Bus



DS100226-6

FIGURE 4.

Function Table

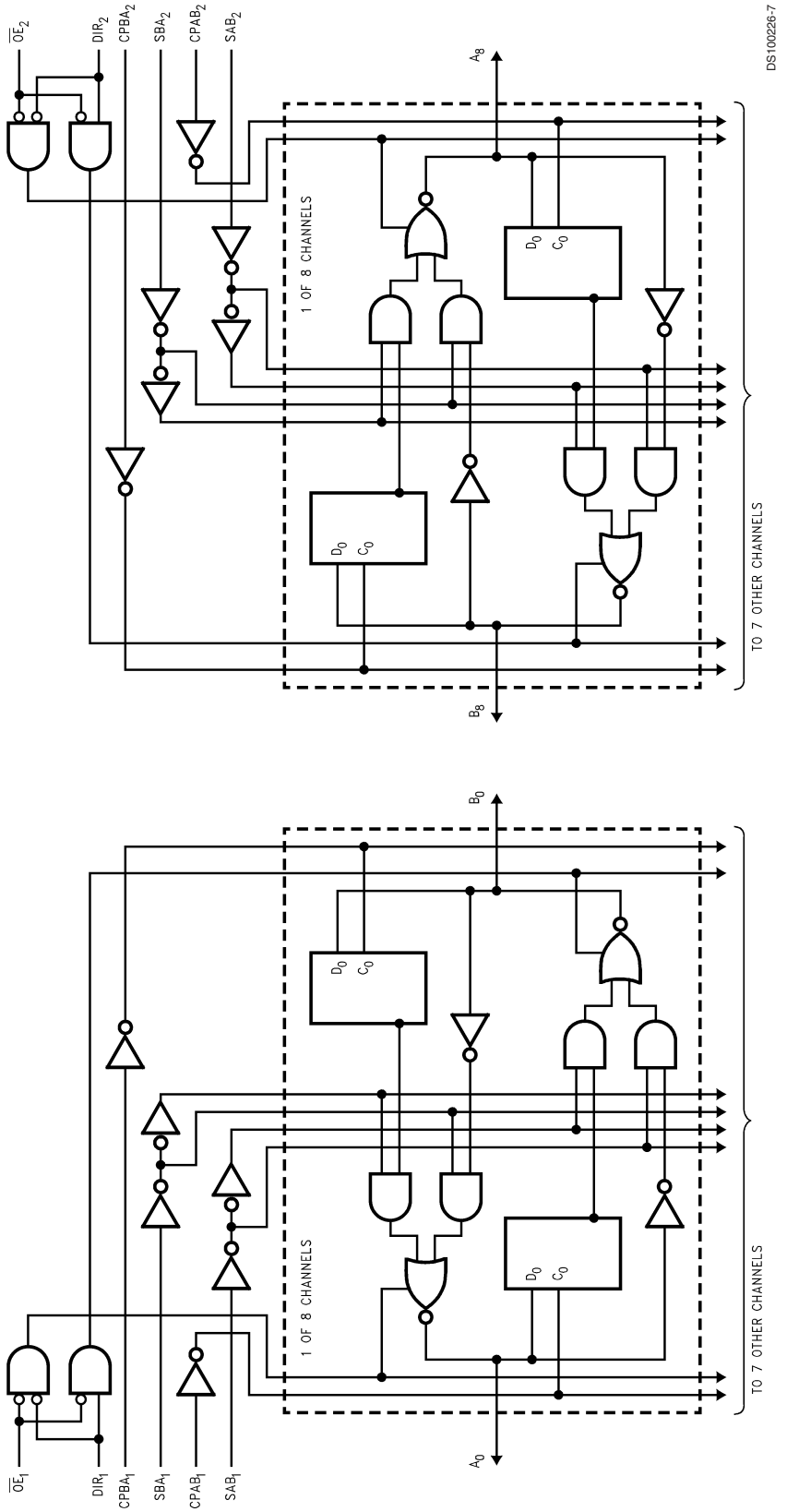
Inputs						Data I/O (Note 1)		Output Operation Mode
$\overline{OE}_1$	DIR_1	$CPAB_1$	$CPBA_1$	SAB_1	SBA_1	A_{0-7}	B_{0-7}	
H	X	H or L	H or L	X	X			Isolation
H	X	N	X	X	X	Input	Input	Clock An Data into A Register
H	X	X	N	X	X			Clock Bn Data Into B Register
L	H	X	X	L	X			An to Bn — Real Time (Transparent Mode)
L	H	N	X	L	X	Input	Output	Clock An Data to A Register
L	H	H or L	X	H	X			A Register to Bn (Stored Mode)
L	H	N	X	H	X			Clock An Data into A Register and Output to Bn
L	L	X	X	X	L			Bn to An — Real Time (Transparent Mode)
L	L	X	N	X	L	Output	Input	Clock Bn Data into B Register
L	L	X	H or L	X	H			B Register to An (Stored Mode)
L	L	X	N	X	H			Clock Bn into B Register and Output to An

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level N = LOW-to-HIGH Transition.

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

Logic Diagram



Absolute Maximum Ratings (Note 2)

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT16646			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage 54ABT	2.5					I_{OH} = −3 mA, (A_n, B_n)
	54ABT	2.0					I_{OH} = −24 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage 54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 5)
							V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−5	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 5)
							V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			50	µA	0V−5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{IL} + I_{OZL}	Output Leakage Current			−50	µA	0V−5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			2.0	mA	Max	Outputs TRI-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V All Other Outputs at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 5)			0.23	mA/MHz	Max	Outputs Open $\overline{OE}$, DIR, and SEL = GND, Non-I/O = GND or V_{CC} (Note 4) One Bit toggling, 50% duty cycle

DC Electrical Characteristics (Continued)

Note 4: For 8-bit toggling, I_{CCD} < 1.4 mA/MHz.

Note 5: Guaranteed but not tested.

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.0	V	5.0	T_A = 25˚C (Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		−1.5	V	5.0	T_A = 25˚C (Note 6)

Note 6: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT T_A = −55˚C to +125˚C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Max	
f_{max}	Max Clock Frequency	125		MHz
t_{PLH}	Propagation Delay	1.0	6.9	ns
t_{PHL}	Clock to Bus	1.0	7.7	
t_{PLH}	Propagation Delay	1.0	5.8	ns
t_{PHL}	Bus to Bus	1.0	7.0	
t_{PLH}	Propagation Delay	1.0	7.1	ns
t_{PHL}	SBA_n or SAB_n to A_n to B_n	1.0	7.2	
t_{PZH}	Enable Time	1.0	6.4	ns
t_{PZL}	$\overline{OE}_n$ to A_n or B_n	1.0	6.5	
t_{PHZ}	Disable Time	1.0	7.6	ns
t_{PLZ}	$\overline{OE}_n$ to A_n or B_n	1.0	6.5	
t_{PZH}	Enable Time	1.0	6.4	ns
t_{PZL}	DIR_n to A_n or B_n	1.0	6.7	
t_{PHZ}	Disable Time	1.0	8.1	ns
t_{PLZ}	DIR_n to A_n or B_n	1.0	7.1	

AC Operating Requirements

Symbol	Parameter	54ABT T_A = −55˚C to +125˚C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Max	
t_S(H)	Setup Time, HIGH	4.0		ns
t_S(L)	or LOW Bus to Clock			
t_H(H)	Hold Time, HIGH	0.5		ns
t_H(L)	or LOW Bus to Clock			
t_W(H)	Pulse Width,	4.3		ns
t_W(L)	HIGH or LOW			

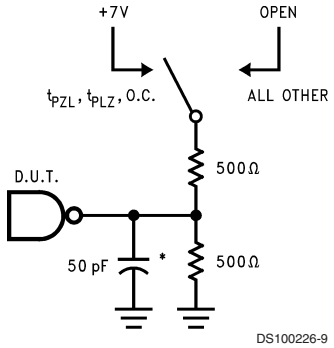
Capacitance

Symbol	Parameter	Typ	Units	Conditions T_A = 25˚C
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 7)	Output Capacitance	11	pF	V_{CC} = 5.0V (A_n, B_n)

Capacitance (Continued)

Note 7: $C_{I/O}$ is measured at frequency, f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 5. Standard AC Test Load

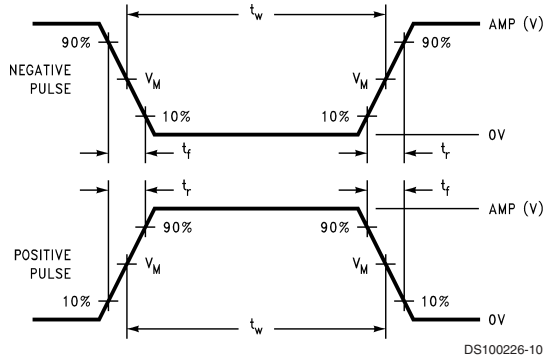


FIGURE 6. V_M = 1.5V Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7. Test Input Signal Requirements

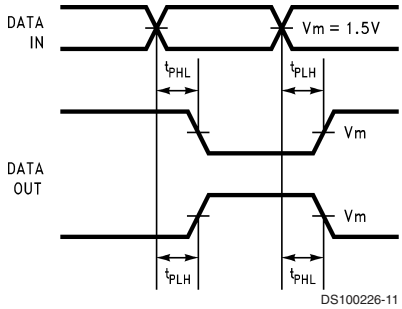


FIGURE 8. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

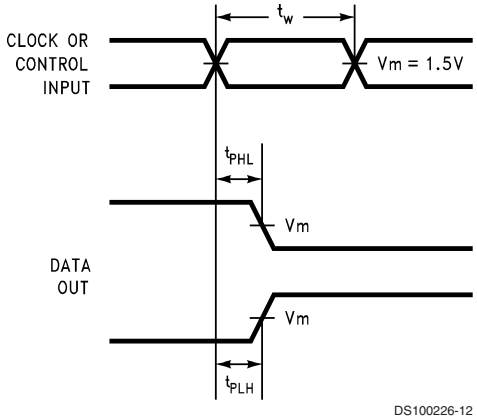


FIGURE 9. Propagation Delay, Pulse Width Waveforms

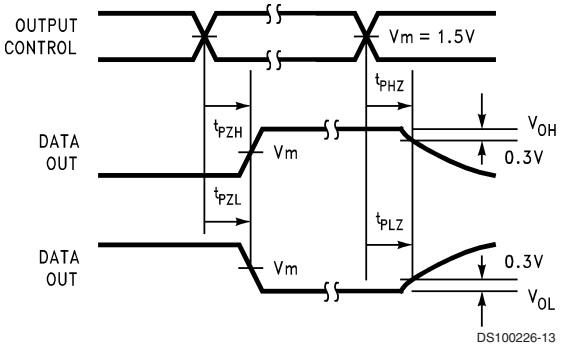


FIGURE 10. TRI-STATE Output HIGH and LOW Enable and Disable Times

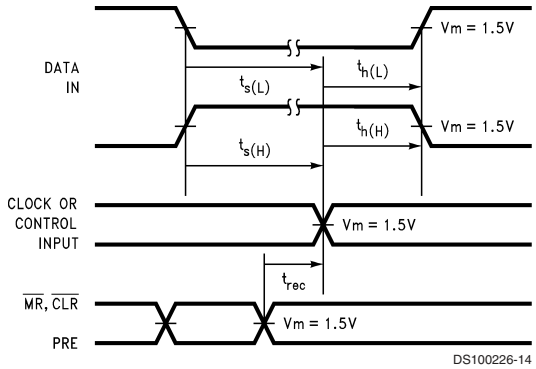
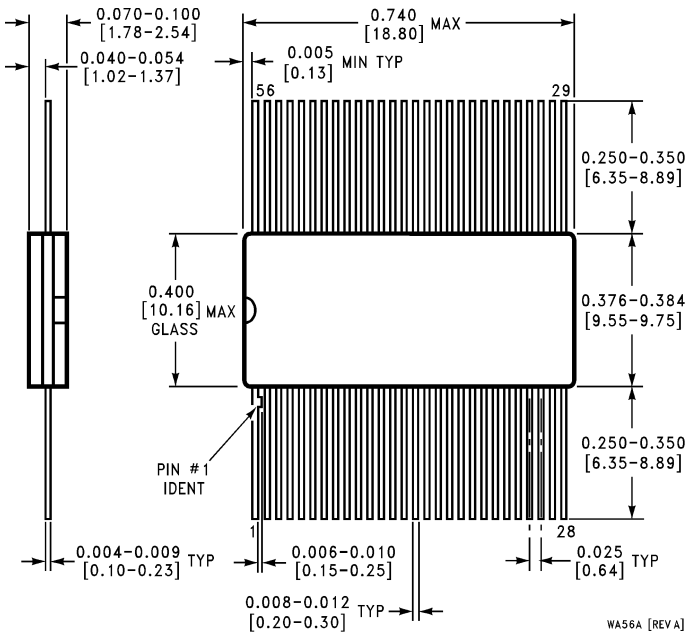


FIGURE 11. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Cerpack
NS Package Number WA56A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560