4-Bit Binary Counter

Military 10H416

ELECTRICALLY TESTED PER:
5962-8759001

The 10H416 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

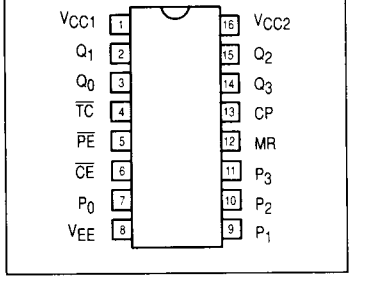
1) JAN: N/A
2) SMD: 5962-8759001
3) 883: 10H416/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

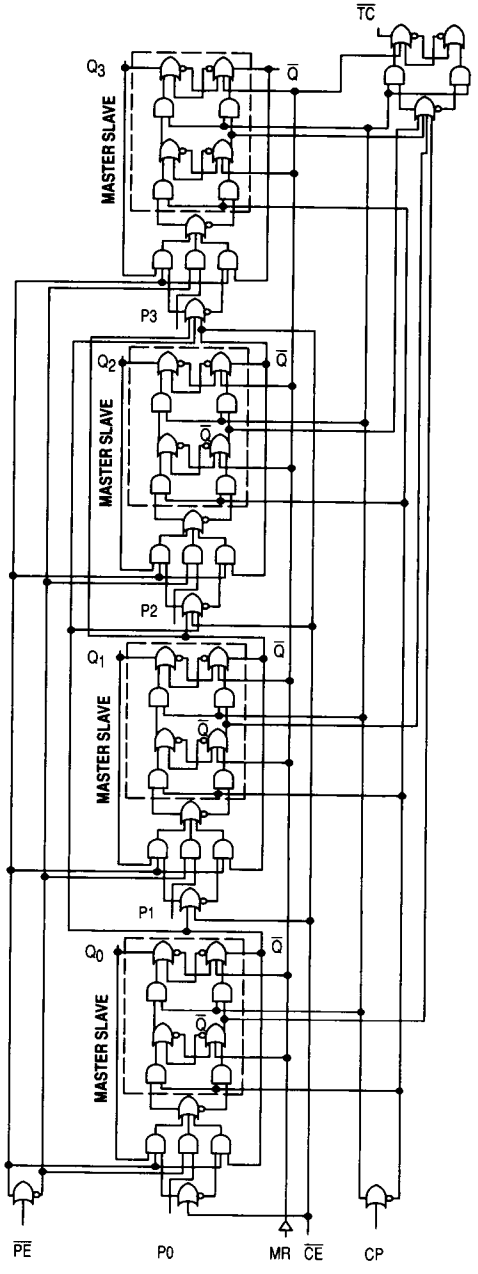
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
Q_0	3	7	4	51 Ω to V_{TT}
$\overline{TC}$	4	8	5	51 Ω to V_{TT}
$\overline{PE}$	5	9	7	OPEN
$\overline{CE}$	6	10	8	OPEN
P_0	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
P_1	9	13	12	GND
P_2	10	14	13	GND
P_3	11	15	14	GND
MR	12	16	15	OPEN
CP	13	1	17	CP1
Q_3	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

PIN NAMES

NAME	FUNCTION
$\overline{PE}$	Parallel Load Enable (Active Low)
P_n	Parallel Inputs
CP	Clock Inputs (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (Low to Count)
MR	Master Reset (High forces all Q Outputs Low)
TC	Terminal Count (10010, Low at HLLH; 10016 Low at HHHH)
Q_n	Counter Outputs



NOTE: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delay$ as many gate functions are achieved internally without incurring a full gate delay.

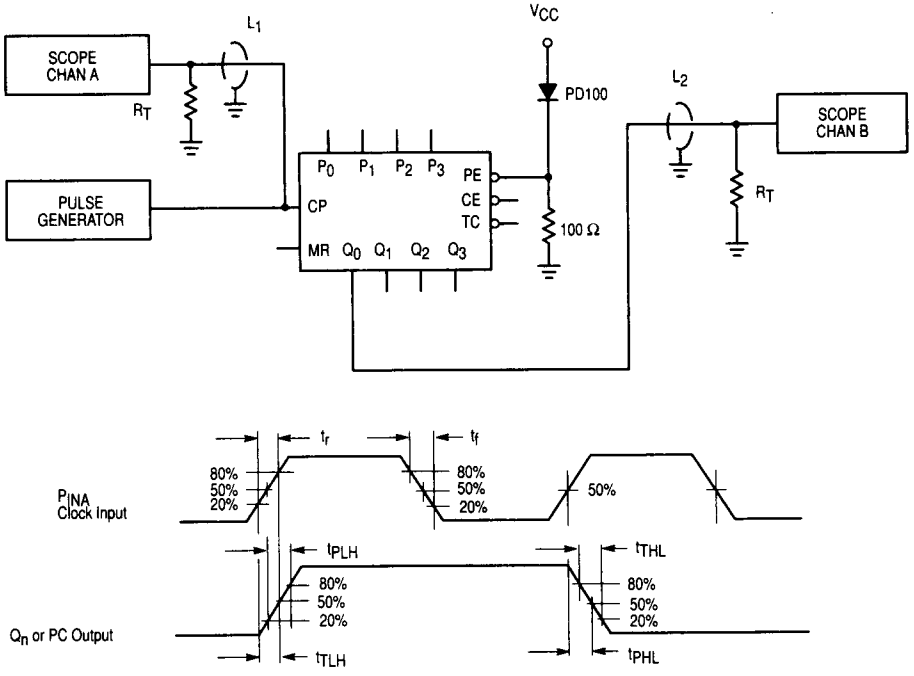
Figure 1. 4-Bit Binary Counter Logic Diagram

TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	FUNCTION
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Master Respond; Slave Hold
X	X	H	X	Reset (Q_n = Low, $\overline{TC}$ = High)

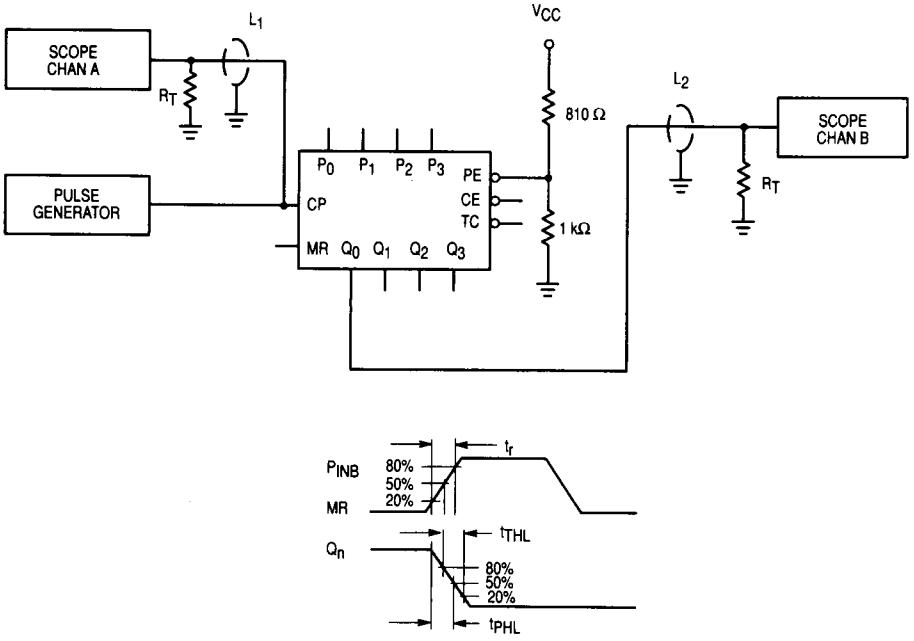
L = Low
H = High Voltage Level
X = Don't Care
Z = Clock Pulse (Low to High)
ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.



NOTES
1. L_1 and L_2 = equal length of 50 Ω impedance line, < 5.0 pF.
2. R_T = 50 Ω termination of scope.
3. Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}.
4. $V_{CC1} = V_{CC2} = 2.0$ V.
5. $V_{EE} = -3.2$ V.

Figure 2. Test Circuit and Waveforms (Clock to Output)



NOTES

1. L_1 and L_2 = equal length of 50 Ω impedance line.
2. R_T = 50 Ω termination of scope.
3. C_L = Jig and stray capacitance < 5.0 pF
3. Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}.
4. $V_{CC1} = V_{CC2} = 2.0$ V.
5. $V_{EE} = -3.2$ V.

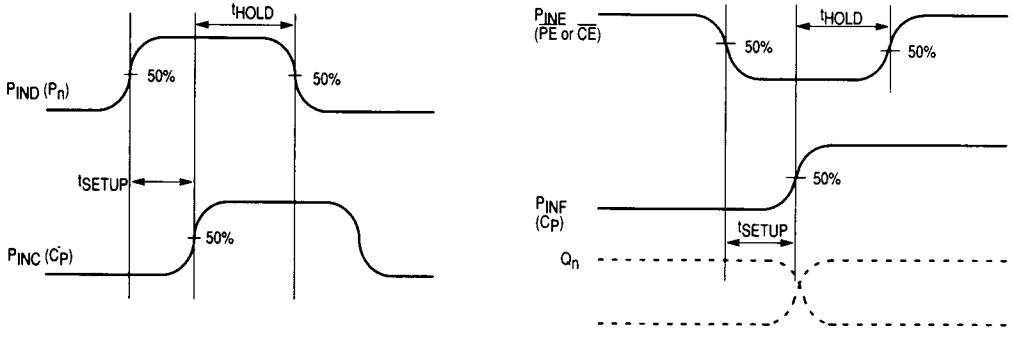


Figure 3. Test Circuit and Waveforms (Master Reset to Output)

10H416
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	9 - 11, 7, 13	13	8		1, 16	2 - 4, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	12, 13	13	8		1, 16	2 - 4, 14, 15
V_{OHA}	High Output Voltage	- 1.01	- 0.78	-0.65	- 0.65	- 1.06	- 0.84	V			8	8	1, 16	2 - 4, 14, 15
V_{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			8	8	1, 16	2 - 4, 14, 15
I_{EE}	Power Supply Current	- 115		- 126		- 126		mA			8		1, 16	8
I_{IH}	Input Current High		265		450		450	µA	5 - 7, 9 - 11		8		1, 16	5 - 7, 9 - 11
I_{IH1}	Input Current High		700		1190		1190	µA	912		8		1, 16	12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 13		8	1, 16	5 - 7, 9 - 13

10H416
QUIESCENT LIMIT TABLE *

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Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	Clk	P.U.T.
t_{TLH}	Rise Time	0.5	2.1	0.5	2.2	0.5	2.0	ns	5 - 13	4	9 - 11	7	1, 16	8		2, 3, 14, 15
t_{THL}	Fall Time	0.5	2.1	0.5	2.2	0.5	2.0	ns	5 - 13	4	9 - 11	7	1, 16	8		2, 3, 14, 15
t_{pd}	Propagation Delay															
	Clk to Q	1.0	2.6	1.0	2.9	1.0	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
	Clk to TC	0.7	2.6	0.7	2.9	0.7	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
	MR to Q	0.7	2.6	0.7	2.9	0.7	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
t_{SET}	Setup Time															
	P_n to Clk	2.0		2.0		2.0		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
	CE or PE to Clk	2.5		2.5		2.5		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
t_{HOLD}	Hold Time															
	Clk to P_n	1.0		1.0		1.0		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
	Clk to PE or CE	0.5		0.5		0.5		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
f_{Count}	Count Frequency	200		200		200		MHz	13	3	9		1, 16	8		2, 4, 14, 15