

## 4-Bit Binary Counter

The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible
- Positive Edge Triggered

### MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ( $V_{CC} = 0$ )	$V_{EE}$	-8.0 to 0	Vdc
Input Voltage ( $V_{CC} = 0$ )	$V_I$	0 to $V_{EE}$	Vdc
Output Current — Continuous	$I_{out}$	50	mA
— Surge		100	
Operating Temperature Range	$T_A$	0 to +75	°C
Storage Temperature Range — Plastic	$T_{stg}$	-55 to +150	°C
— Ceramic		-55 to +165	

### ELECTRICAL CHARACTERISTICS ( $V_{EE} = -5.2 V \pm 5\%$ ) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	$I_E$	—	126	—	115	—	126	mA
Input Current High All Except MR Pin 12 MR	$I_{inH}$	—	450 1190	—	265 700	—	265 700	$\mu A$
Input Current Low	$I_{inL}$	0.5	—	0.5	—	0.3	—	$\mu A$
High Output Voltage	$V_{OH}$	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	$V_{OL}$	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	$V_{IH}$	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	$V_{IL}$	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

### AC PARAMETERS

Propagation Delay Clock to Q Clock to $\overline{TC}$ MR to Q	$t_{pd}$	1.0	2.4	1.0	2.5	1.0	2.7	ns
		0.7	2.4	0.7	2.5	0.7	2.6	
		0.7	2.4	0.7	2.5	0.7	2.6	
Set-up Time $P_n$ to Clock $\overline{CE}$ or $\overline{PE}$ to Clock	$t_{set}$	2.0	—	2.0	—	2.0	—	ns
		2.5	—	2.5	—	2.5	—	
Hold Time Clock to $P_n$ Clock to $\overline{CE}$ or $\overline{PE}$	$t_{hold}$	1.0	—	1.0	—	1.0	—	ns
		0.5	—	0.5	—	0.5	—	
Counting Frequency	$f_{count}$	200	—	200	—	200	—	MHz
Rise Time	$t_r$	0.5	2.0	0.5	2.1	0.5	2.2	ns
Fall Time	$t_f$	0.5	2.0	0.5	2.1	0.5	2.2	ns

#### NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

## MC10H016



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

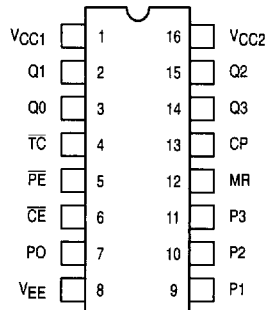


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**FN SUFFIX**  
PLCC  
CASE 775-02

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.

### TRUTH TABLE

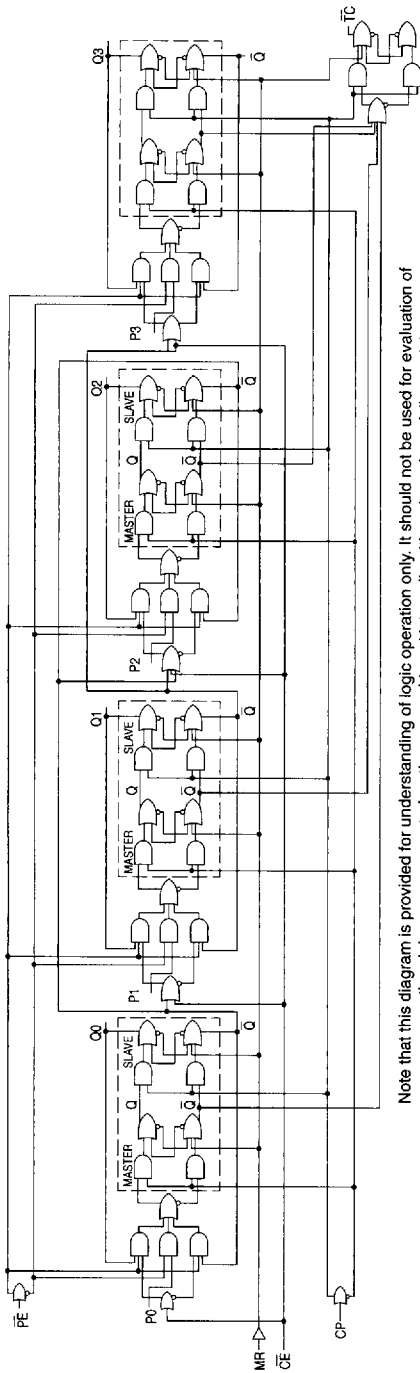
$\overline{CE}$	$\overline{PE}$	MR	CP	Function
L	L	L	Z	Load Parallel ( $P_n$ to $Q_n$ )
H	L	L	Z	Load Parallel ( $P_n$ to $Q_n$ )
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Masters Respond; Slaves Hold
X	X	H	X	Reset ( $Q_n = LOW$ , $\overline{TC} = HIGH$ )

Z = Clock Pulse (Low to High); ZZ = Clock Pulse (High to Low)

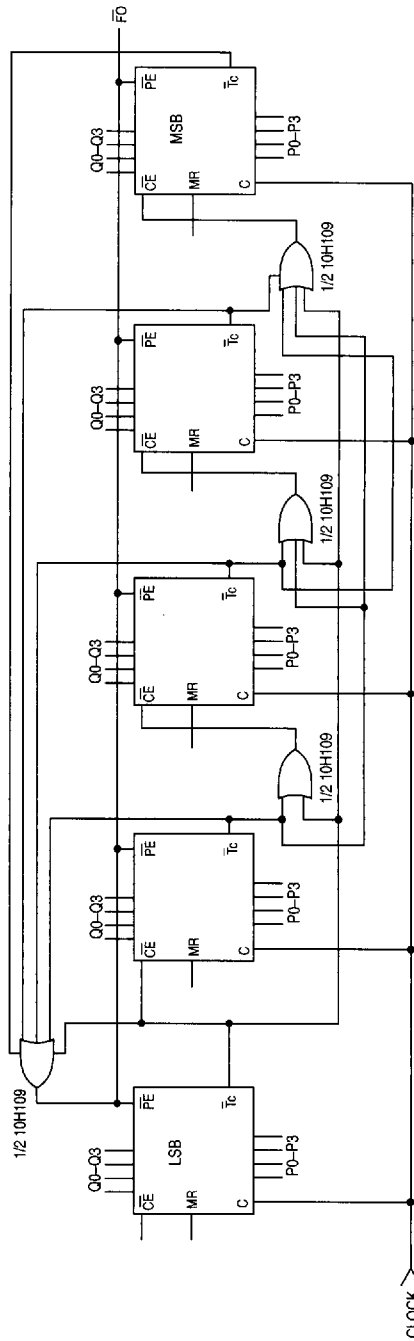
Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.



4-Bit Binary Counter Logic Diagram



Note that this diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.



+ N Counter 1 to 16 5  
**MC10H016 Cascaded for 5 Stage Presettable Counter**  
 Max freq. is only OR gate delay below max when counting alone.