MOTOROLA

High Speed Dual D Type Master Slave Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/06102

The 10631 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

3

- 375 mW Max/Pkg (No Load)
- f_{Tog} = 225 MHz typ
- t_{pd} = 2.0 ns typ (All Output Loaded)
- t_r, t_f = 2.0 ns typ (20% - 80%)

	PIN ASSIGNMENTS			
FUNCTION	**DIL**	**FLATS**	**LCC**	**BURN-IN (CONDITION C)**
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_C	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

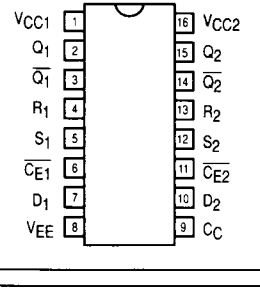
Military 10631

AVAILABLE AS:

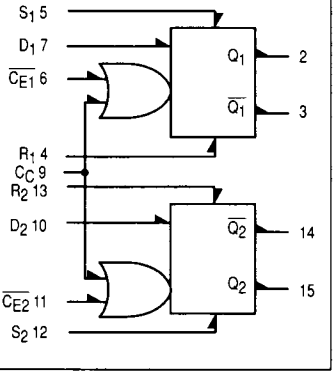
1) JAN: JM 38510/06102
2) SMD: N/A
3) 883: 10631/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



R-S TRUTH TABLE

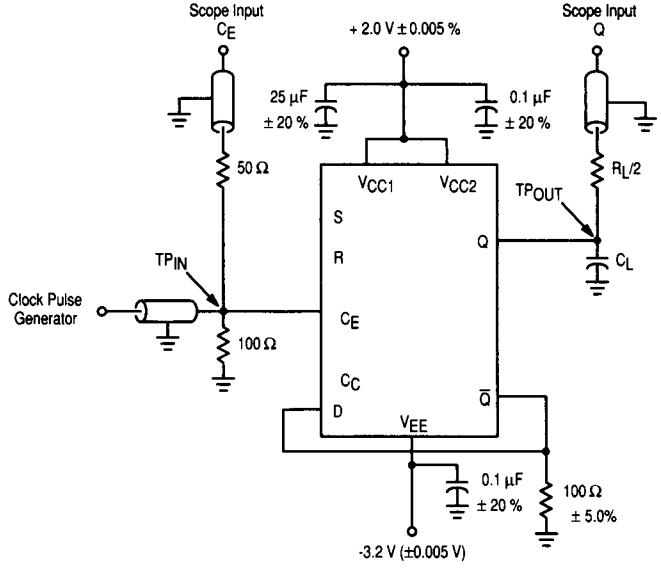
R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N. D.

N.D. = Not Defined
A clock H is a clock transition from a Low to a High state

CLOCKED TRUTH TABLE

C	D	$Q_n + 1$
L	∅	Q_n
H	L	L
H	H	H

∅ = Don't Care
$C = C_E + C_C$



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $t_r = t_f = 2.0$ ns (20% - 80%).
7. Scope Input = 50 Ω GND.
8. C_L (test Jig) ≤ 5.0 pF.

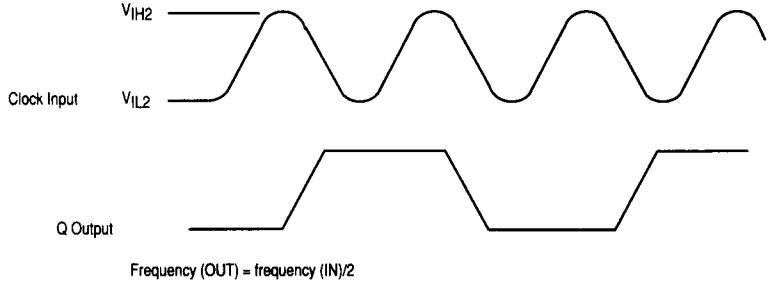
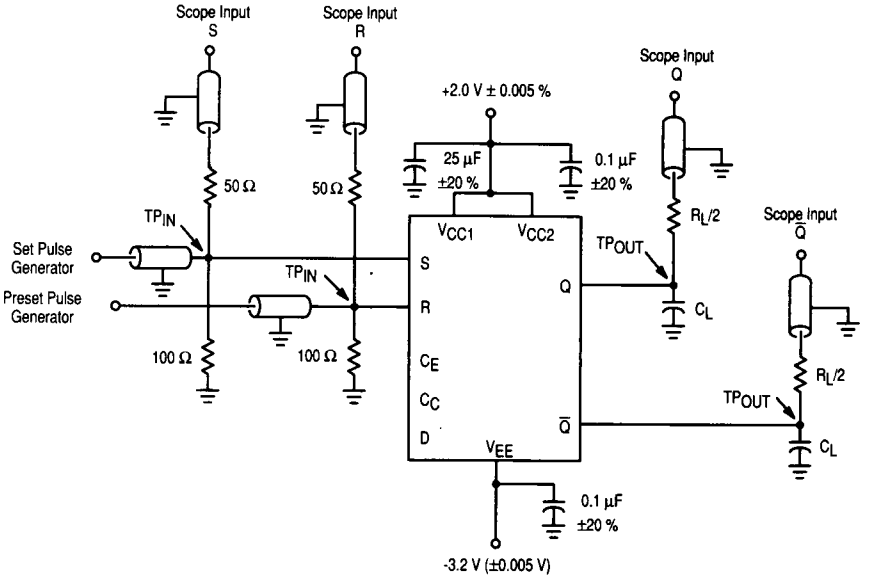
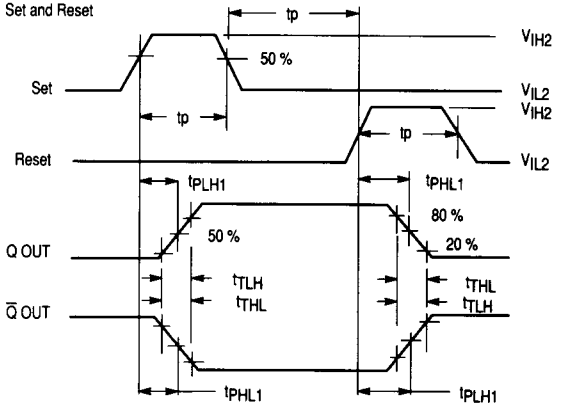


Figure 1. F_{MAX} Test Circuit and Clock Input Sinewave





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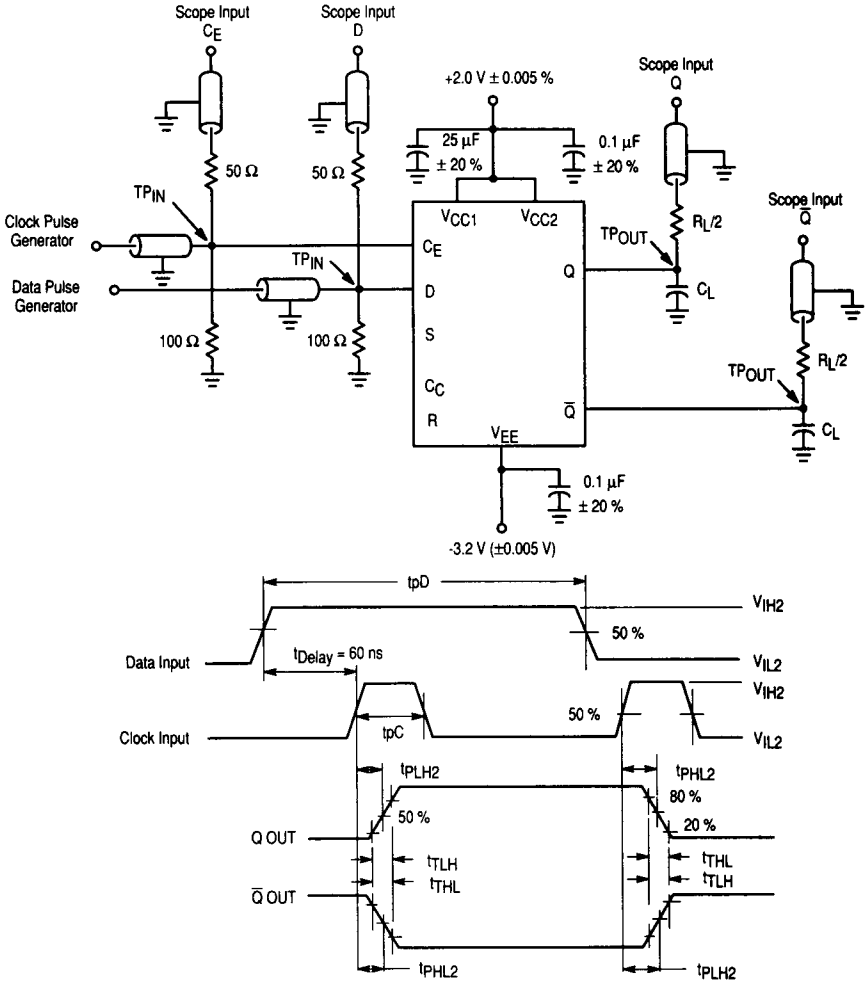
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_{REC} (Set & Reset) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

Figure 2. Set and Reset Switching Test Circuit



NOTES

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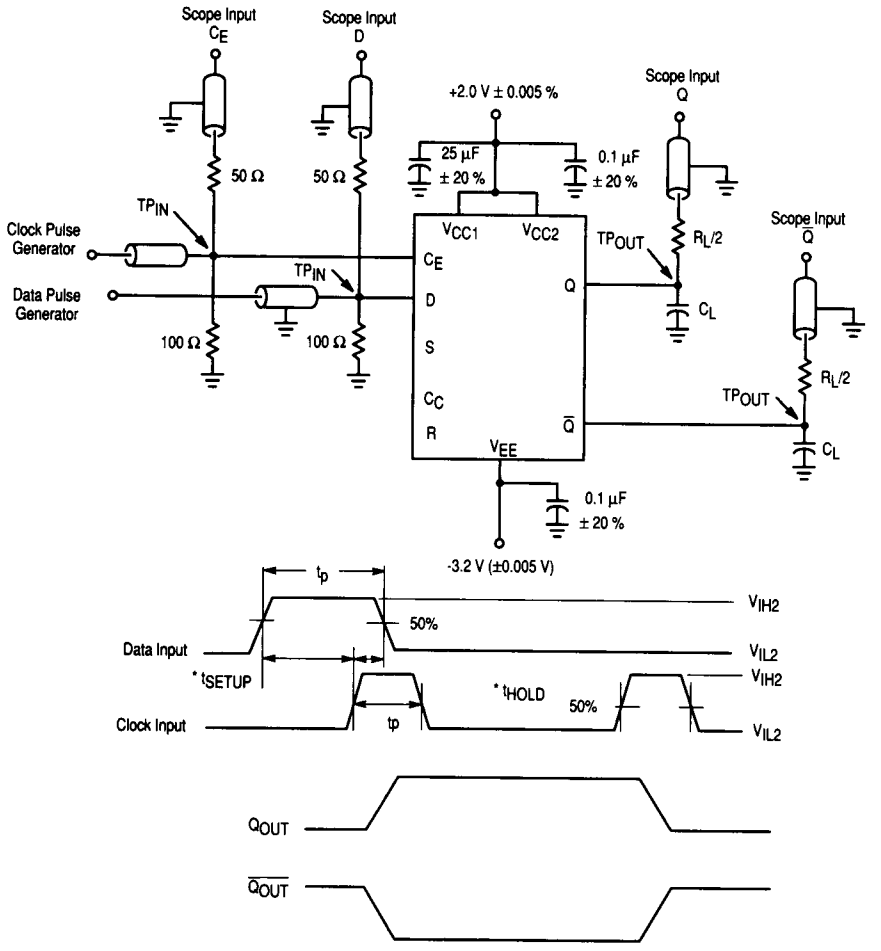
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_{pD}(Data) = 150 ns, t_{pC} (Clock) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

Figure 3. Synchronous Switching Test Circuit and Waveform



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.36 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $Z_{OUT} = 50\ \Omega$.
7. t_p(Data & Clock) = 40 ns.
8. Scope Input = 50 Ω to GND.
9. C_L (test Jig) ≤ 5.0 pF.
* 10. For information only; not tested: $t_{setup} \geq 1.0$ ns, $t_{hold} \geq 0.75$ ns.

Figure 4. Setup and Hold Test Circuit and Waveform

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.78	- 1.85	+ 1.11	+ 0.31	- 1.105	- 1.475	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	+ 1.24	+ 0.36	- 1.000	- 1.400	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	+ 1.01	+ 0.28	- 1.255	- 1.510	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 12, 13	4 - 7 9 - 13			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 12, 13	4 - 7 9 - 13			8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	4, 5, 12, 13	4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	4, 5, 12, 13	4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	- 65		- 72		- 72		mA					8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	6, 11				8	1, 16	6, 11
I_{IH1}	Input Current High		410		700		700	µA	4, 5, 12, 13				8	1, 16	4, 5, 12, 13
I_{IH2}	Input Current High		220		375		375	µA	7, 10				8	1, 16	7, 10
I_{IH3}	Input Current High		290		495		495	µA	9				8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 13			8	1, 16	4 - 7, 9 - 13

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T_A = 125 °C	- 0.63	- 1.82	+ 1.24	+ 0.36	- 1.000	- 1.400	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	+ 1.01	+ 0.28	- 1.255	- 1.510	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P. U. T.
t_{TLH}	Rise Time	1.0	3.1	1.1	3.6	0.9	3.4	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 6	8	2, 3, 14, 15
t_{THL}	Fall Time	1.0	3.1	1.1	3.6	0.9	3.4	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 6	8	2, 3, 14, 15
t_{PLH1}	Propagation Delay	1.1	3.3	1.0	3.9	1.0	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2}	Propagation Delay	1.5	3.3	1.2	3.9	1.3	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL1}	Propagation Delay	1.1	3.3	1.0	3.9	1.0	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL2}	Propagation Delay	1.5	3.3	1.2	3.9	1.3	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
$f_{(max)}$	Toggle Frequency (max)	200		200		200		MHz	6, 11	2, 15	1, 16	8	2, 3, 14, 15