



Quad TTL-to-MECL Translator

**ELECTRICALLY TESTED PER:
MIL-M-38510/06301**

The 10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MECL 10524 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the logic low level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, + 5.0 Volts, and - 5.2 Volts. Propagation delay of the 10524 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the 10515 or 10516 differential receivers. The 10524 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communication systems.

- 205 mW Max/Pkg (No Load)
- $t_{pd} = 3.5$ ns typ (1.5 Vdc in to 50% out)
- $t_r, t_f = 2.5$ ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
BOUT	1	5	2	50 Ω to V_{TT}
AOUT	2	6	3	51 Ω to V_{TT}
\overline{BOUT}	3	7	4	50 Ω to V_{TT}
\overline{AOUT}	4	8	5	50 Ω to V_{TT}
A _{IN}	5	9	7	V_{CC}
Common Strobe	6	10	8	V_{CC}
B _{IN}	7	11	9	V_{CC}
VEE	8	12	10	V_{EE}
VCC	9	13	12	V_{CC}
C _{IN}	10	14	13	V_{CC}
D _{IN}	11	15	14	V_{CC}
\overline{COUT}	12	16	15	51 Ω to V_{TT}
\overline{DOUT}	13	1	17	51 Ω to V_{TT}
DOUT	14	2	18	51 Ω to V_{TT}
COUT	15	3	19	GND
GND	16	4	20	GND

BURN - IN CONDITIONS:

$V_{TT} = -2.0$ V MAX / -2.2 V MIN
 $V_{EE} = -5.7$ V MAX / -5.2 V MIN

Military 10524

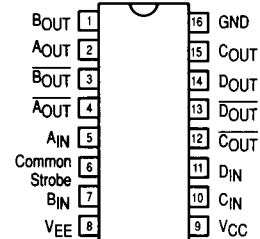


AVAILABLE AS

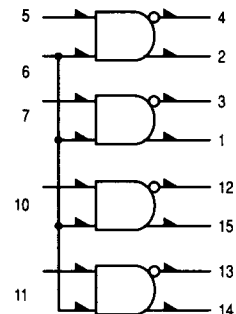
- 1) JAN: JM 38510/06301
 - 2) SMD: N/A
 - 3) 883: 10524/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

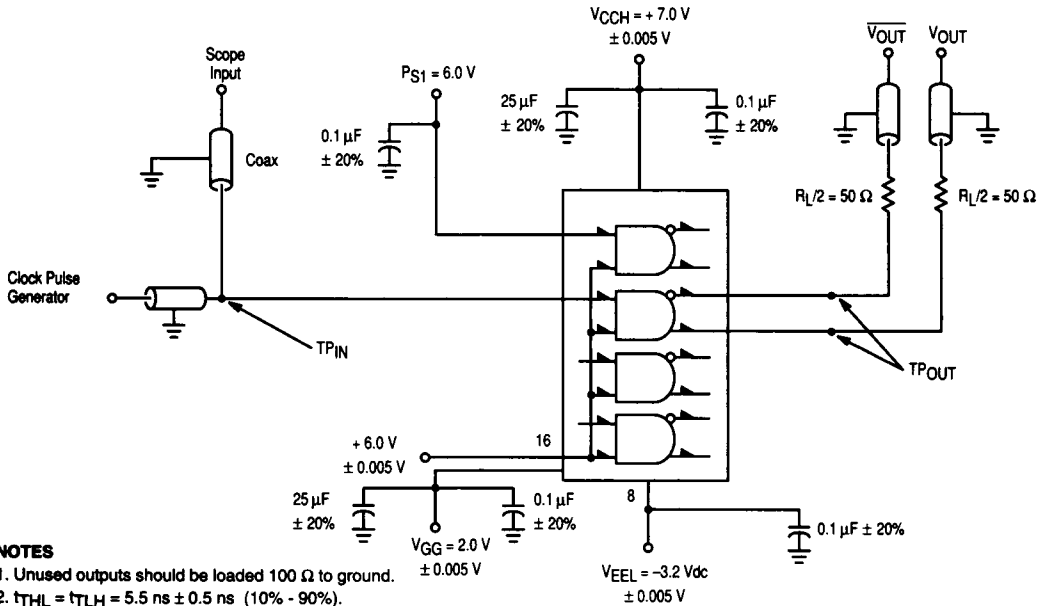
PACKAGE: CERDIP: E
 CERFLAT: F
 LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Unused outputs should be loaded 100 Ω to ground.
2. $t_{THL} = t_{TLH} = 5.5 \text{ ns} \pm 0.5 \text{ ns}$ (10% - 90%).
3. $t_p = 40 \text{ ns} \pm 2.0 \text{ ns}$.
4. $Z_{OUT} = 50 \Omega$.
5. $C_L = \text{Jig and stray capacitance} \leq 5.0 \text{ pF}$.

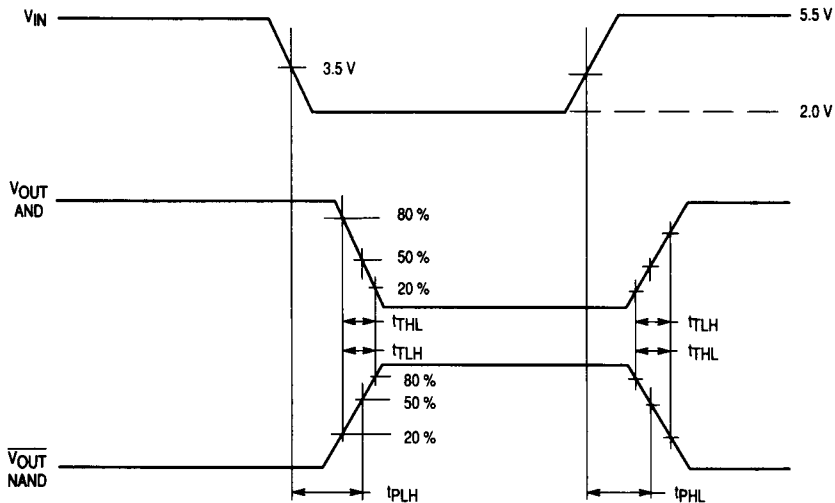


Figure 1. Switching Test Circuit and Waveforms

NOTES

1. 50 Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TPIN to input pin and TPOUT to output pin.

10524 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{TTL}	V _{ITH}	V _{VCH}	V _{VGG}	V _{VEE}	V _{VEEL}
T _A = 25 °C	+2.4	+0.4	+1.10	+1.80	+7.0	+2.0	-5.2	-3.2
T _A = 125 °C	+2.4	+0.4	+0.80	+1.80	+7.0	+2.0	-5.2	-3.2
T _A = -55 °C	+2.4	+0.4	+1.10	+2.00	+7.0	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 5.0 V, I _{IN} = 10 mA, Output Load = 100 Ω to -2.0 V								
		Subgroup 1 Min	Subgroup 1 Max	Subgroup 2 Min	Subgroup 2 Max	Subgroup 3 Min	Subgroup 3 Max		V _{IH1}	V _{IL1}	V _{ITH}	V _{TTL}	V _{IN}	GND	V _{EE}	V _{CC}	P. U. T.
V _{OH}	High Output Voltage	-0.93	-0.76	-0.825	-0.63	-1.08	-0.88	V	5, 6, 7, 10, 11	6			16	8	9	1-4, 12-15	
V _{OL}	Low Output Voltage	-1.85	-1.62	-1.82	-1.545	-1.92	-1.655	V	5, 6, 7, 10, 11	6			16	8	9	1-4, 12-15	
V _{OH1}	High Output Voltage	-0.95		-0.845		-1.10		V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11	16	8	9	1-4, 12-15	
V _{OL1}	Low Output Voltage		-1.60		-1.525		-1.635	V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11	16	8	9	1-4, 12-15	
I _{EE}	Power Supply Current		-66		-73		-73	mA					16	8	9	8	
I _{IH1}	Input Current High		50		85		85	μ A	5, 7, 10, 11				6, 16	8	9	5, 7, 10, 11	
I _{IL1}	Input Current Low	-3.2		-5.5		-3.2		mA	6	5, 7, 10, 11			16	8	9	5, 7, 10, 11	
I _{IH2}	Input Current High		200		340		340	μ A	6				5, 7, 10, 11, 16	8	9	6	
I _{IL2}	Input Current Low	-12.8		-22		-12.8		mA		6			16	8	9	6	
V _{IC}	Input Clamp Voltage	-1.5						V					5-7, 10, 11	16	8	9	5-7, 10, 11

10524 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{ITL}	V _{ITH}	V _{ICL}	V _{ICH}	V _{GG}	V _{VEE}
T _A = 25 °C	+2.4	+0.4	+1.10	+1.80	+7.0	+2.0	+2.0	-3.2
T _A = 125 °C	+2.4	+0.4	+0.80	+1.80	+7.0	+2.0	+2.0	-3.2
T _A = -55 °C	+2.4	+0.4	+1.10	+2.00	+7.0	+2.0	+2.0	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 5.0 V, I _{IN} = 1.0 mA, Output Load = 100 Ω to - 2.0 V									
Functional Parameters:		Subgroup 1	Subgroup 2	Subgroup 2	Subgroup 3	Subgroup 3		V _{IH1}	V _{IL1}	V _{ITH}	V _{ITL}	I _{IN}	GND	V _{EE}	V _{CC}	P. U. T.		
ICCL ICCH	Positive Power Supply Current Drain	Min Max	25 16	Min Max	28 18	Min Max	28 18						5, 7, 10, 11, 16	8	5 - 7, 9, 10, 11	9		
BV _{IN}	Input Break-down Voltage	Min	5.5	Min	5.5	Min	5.5	V	6			5 - 7, 10, 11	16	8	9	5 - 7 10, 11		

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 5.0 V, I _{IN} = - 10 mA or - 20 mA Output Load = 100 Ω to GND									
Functional Parameters:		Subgroup 9	Subgroup 10	Subgroup 10	Subgroup 11	Subgroup 11		V _{IN}	V _{OUT}	V _{ICL}	V _{ICH}	V _{VEE}	V _{GG}	+ 6.0 V	P. U. T.			
t _{TLH}	Rise Time	Min Max	1.1 3.9	Min Max	1.0 5.0	Min Max	1.0 5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15			
t _{FHL}	Fall Time	Min Max	1.1 3.9	Min Max	1.0 5.0	Min Max	1.0 5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15			
t _{pHL}	Propagation Delay High to Low	Min Max	1.0 6.0	Min Max	1.0 8.0	Min Max	1.0 8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15			
t _{pLH}	Propagation Delay Low to High	Min Max	1.0 6.0	Min Max	1.0 8.0	Min Max	1.0 8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15			

PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

L SUFFIX CERAMIC PACKAGE CASE 620-09

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.95	19.81	0.790	0.780
B	6.22	6.30	0.245	0.275
C	4.08	5.00	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.08	0.125	0.160
L	2.27	2.87	0.290	0.310
M	15°		15°	
N	0.51	1.02	0.020	0.040

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

L SUFFIX CERAMIC PACKAGE CASE 623-05 (LW SUFFIX FOR MC10H181 ONLY)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.08	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.08	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0° 15°		0° 15°	
N	0.51	1.27	0.020	0.050

NOTES:

- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

P SUFFIX PLASTIC PACKAGE CASE 626-04

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.78	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.51	0.78	0.020	0.030

NOTES:

- LEAD POSITIONAL TOLERANCE: $\textcircled{\text{M}} \textcircled{\text{L}} 0.13 (0.005) \textcircled{\text{M}} \textcircled{\text{T}} \textcircled{\text{A}} \textcircled{\text{B}} \textcircled{\text{D}}$
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
- DIMENSIONS A AND B ARE DATUMS.
- DIMENSIONS G AND TOLERANCING PER ANSI Y14.5M, 1982.

L SUFFIX CERAMIC PACKAGE CASE 632-08

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.01	0.020	0.040

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION; INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

PACKAGE OUTLINE DIMENSIONS (continued)

**P SUFFIX
PLASTIC PACKAGE
CASE 646-06**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.29	1.01	0.015	0.039

NOTE 4: LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

**P SUFFIX
PLASTIC PACKAGE
CASE 648-08**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

NOTE 4: LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

**P SUFFIX
PLASTIC PACKAGE
CASE 649-03**

**(PW SUFFIX
FOR MC10H181
ONLY)**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	10°		10°	
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

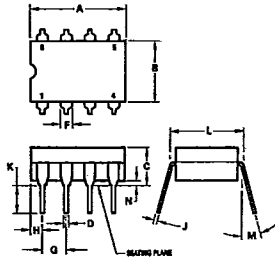
NOTE 4: LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

**F SUFFIX
CERAMIC PACKAGE
CASE 650-05**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.73	6.80	0.265	0.269
C	1.53	2.15	0.060	0.085
D	0.38	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

NOTE 4: LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

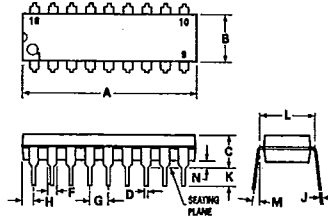
**L SUFFIX
CERAMIC PACKAGE
CASE 693-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.91	10.92	0.350	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	2.18	4.08	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

- NOTES:
 1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

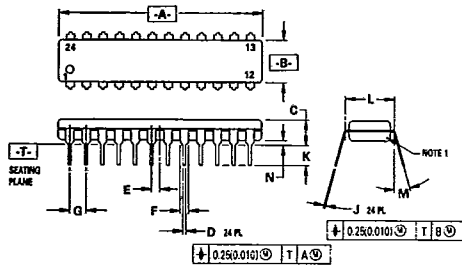
**P SUFFIX
PLASTIC PACKAGE
CASE 707-02**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:
 1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

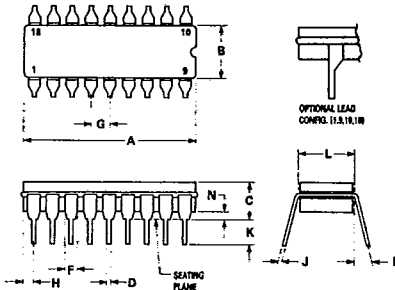
**P SUFFIX
PLASTIC PACKAGE
CASE 724-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.68	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:
 1. CHAMFERED CONTOUR OPTIONAL.
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSIONS AND TOLERANCES PER ANSI Y14.34, 1982.
 4. CONTROLLING DIMENSION: INCH.

**L SUFFIX
CERAMIC PACKAGE
CASE 726-04**



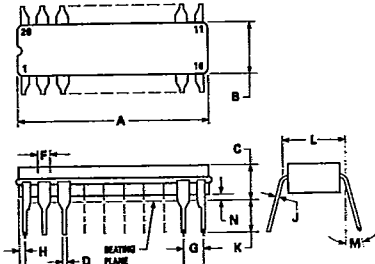
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:
 1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM "A" & "B" INCLUDES MENISCUS.
 4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

PACKAGE OUTLINE DIMENSIONS (continued)

1

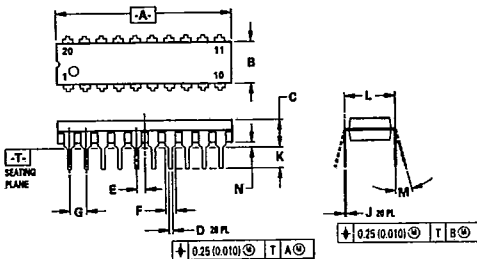
**L SUFFIX
CERAMIC PACKAGE
CASE 732-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.80	7.43	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

- NOTES:
 1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIM A AND B INCLUDES MENISCUS.

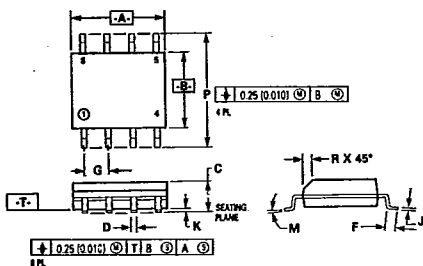
**P SUFFIX
PLASTIC PACKAGE
CASE 738-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.55	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.38	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

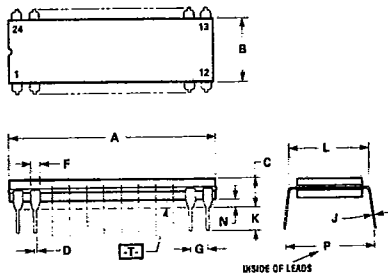
**D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-03**



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.90	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.015	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

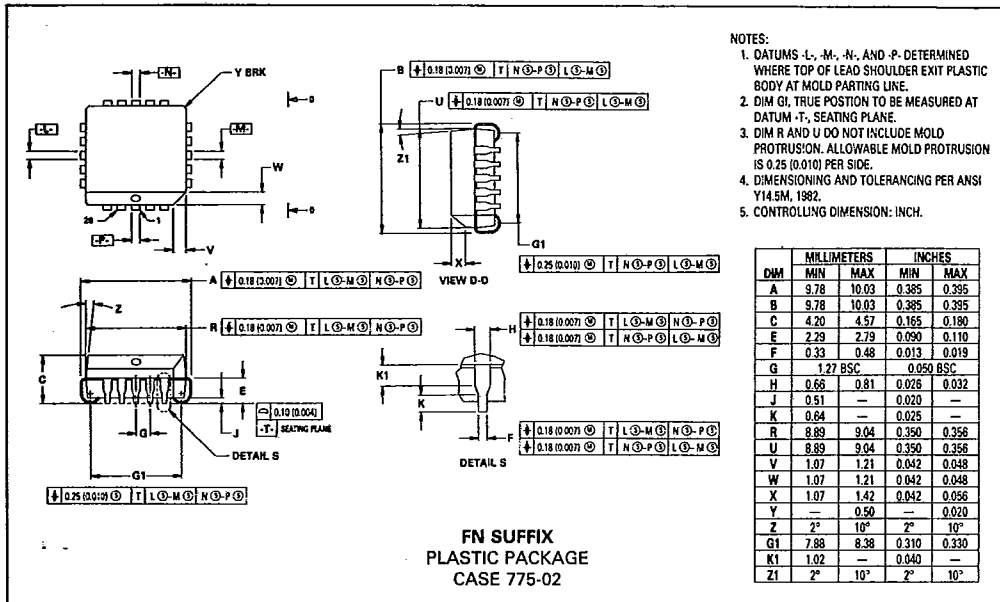
- NOTES:
 1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. CONTROLLING DIM: MILLIMETER.
 4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

**L SUFFIX
CERAMIC PACKAGE
CASE 758-01**

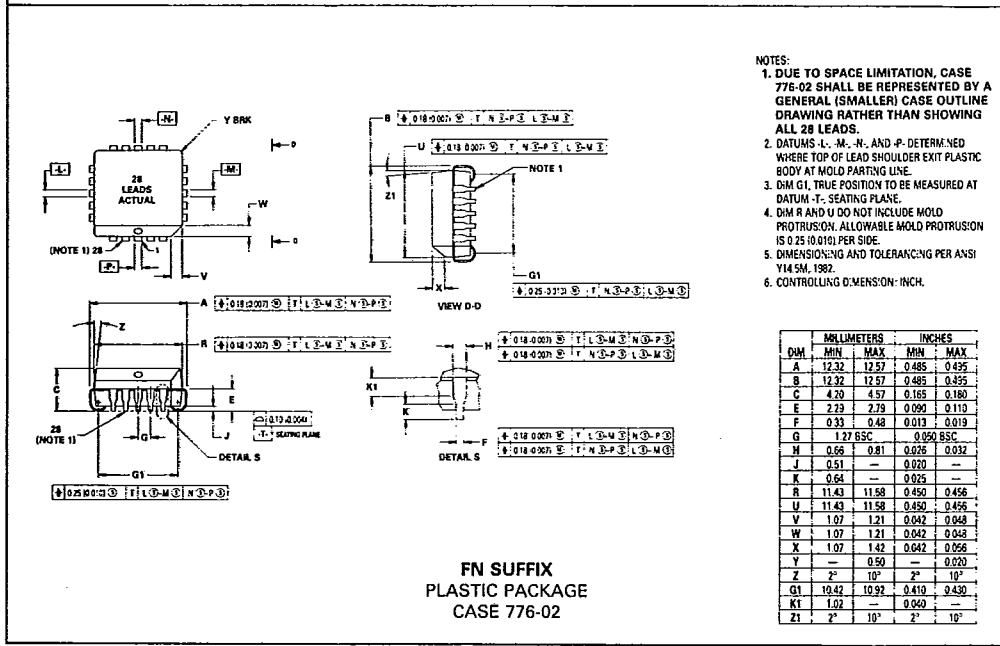


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.97	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

- NOTES:
 1. DIMENSION A IS DATUM.
 2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
 $\pm 0.25 (0.010) \text{ TIA } \text{M}$
 3. T IS SEATING PLANE.
 4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



- NOTES:
- DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
 - DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 - DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.



- NOTES:
- DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
 - DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
 - DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 - DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.

MECL Logic Surface Mount

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

TAPE AND REEL

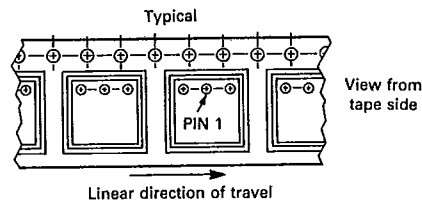
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to

the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

ORDERING CODE

- MC10100FN
- MC10100FNR2
- MC10H100FN
- MC10H100FNR2
- MC12015D
- MC12015DR2

SHIPMENT METHOD

- Magazines (Rails)
- 13 inch Tape and Reel
- Magazines (Rails)
- 13 inch Tape and Reel
- Magazines (Rails)
- 13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28