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GaN Systems

AN-009 HiRel Power Application Brief

PCB Layout Considerations with GaN E-HEMTs

October 23, 2020

Overview

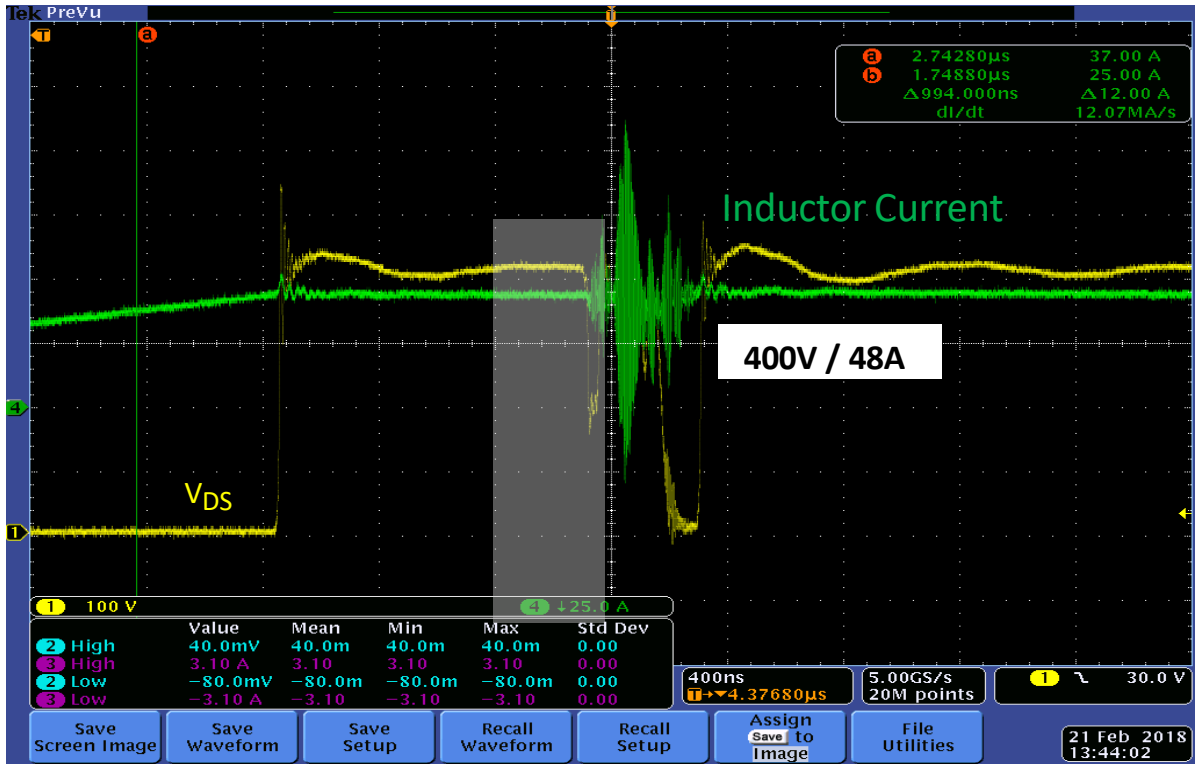
- This guide provides an overview of the good engineering practice for PCB layout of designs using GaN Systems' embedded GaN*PX*® packaged E-HEMTs.
- Layout guidelines are introduced for the following four circuit configurations
  1) Isolated gate driver circuit for single GaN E-HEMTs
  2) Isolated gate driver circuit for paralleled GaN E-HEMTs
  3) Half-bridge Booststrap gate driver circuit
  4) EZDrive^{SM} circuit
- With optimum board layout combined with low GaNPX® package inductance, GaN E-HEMTs exhibit optimum switching performance

Introduction

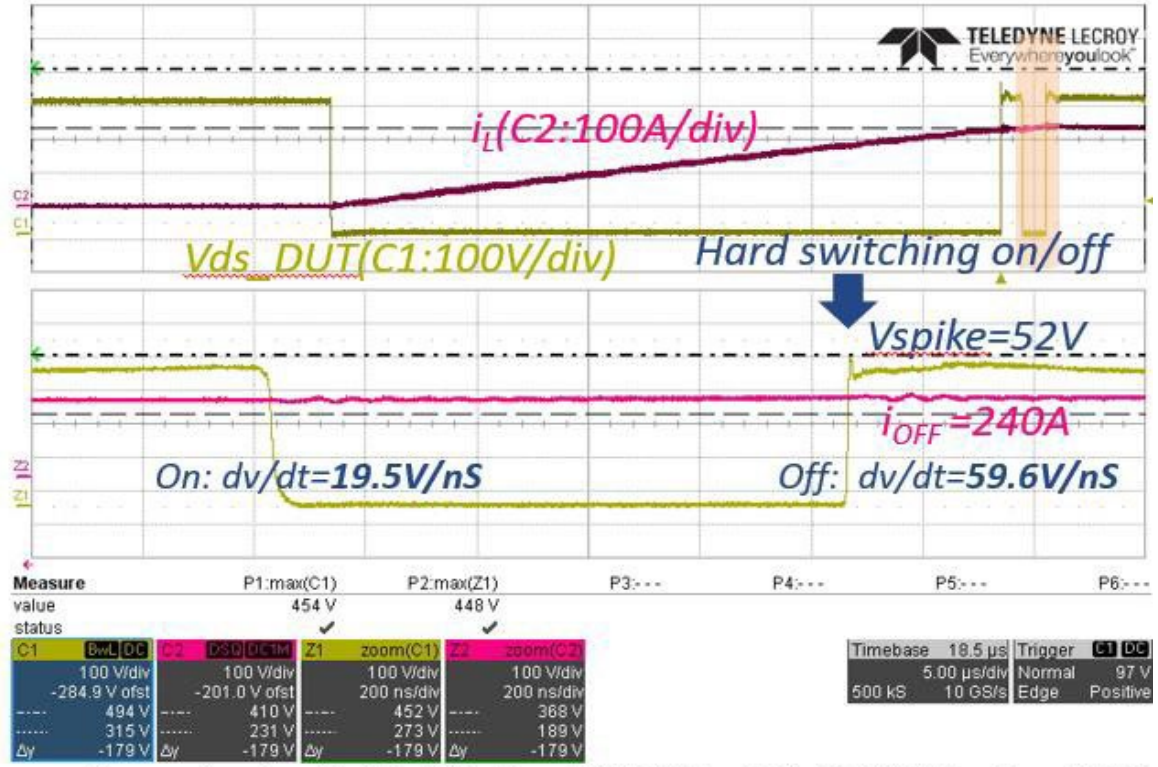
- GaN Systems' E-HEMTs have very low packaging inductance, while enabling ultra-low inductance PCB power loops.
- Good engineering practice of layout techniques are required to minimize parasitic inductance and fully utilize the benefit of GaN Systems' E-HEMTs.
- This application note shows key steps to design an optimal PCB layout with GaN to maximize converter performance.

Motivation

- GaN E-HEMTs switch much faster than Si MOSFETs, and require proper engineering consideration of PCB layout design to minimize parasitic inductances.
- Parasitic inductances can cause higher overshoot voltages, ringing/oscillation, EMC issues, which can lead to overstressing the E-HEMTs.



Example of an unsuccessful design caused by unbalanced quasi-common source inductance



Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

Example of clean switching waveforms when good PCB layout practices are used (400 V/240 A DPT)

PCB Layout Steps

- **Step 1:** Prepare the schematics and identify the components of each critical loop
  - Isolated gate driver circuit for single GaN HEMTs
  - Isolated gate driver circuit for paralleled GaN HEMTs
  - Half-bridge Bootstrap gate driver circuit
  - EZDrive^{SM} circuit
- **Step 2:** Place the components according to the design priority and current direction
  - Put components as close as possible
  - According to the current direction, set the component in sequence
  - If there is a conflict for minimizing all the loops, refer to the priority listed on slides 7/8/9/10.
- **Step 3:** Connect the components optimally to achieve low parasitics with flux cancellation techniques

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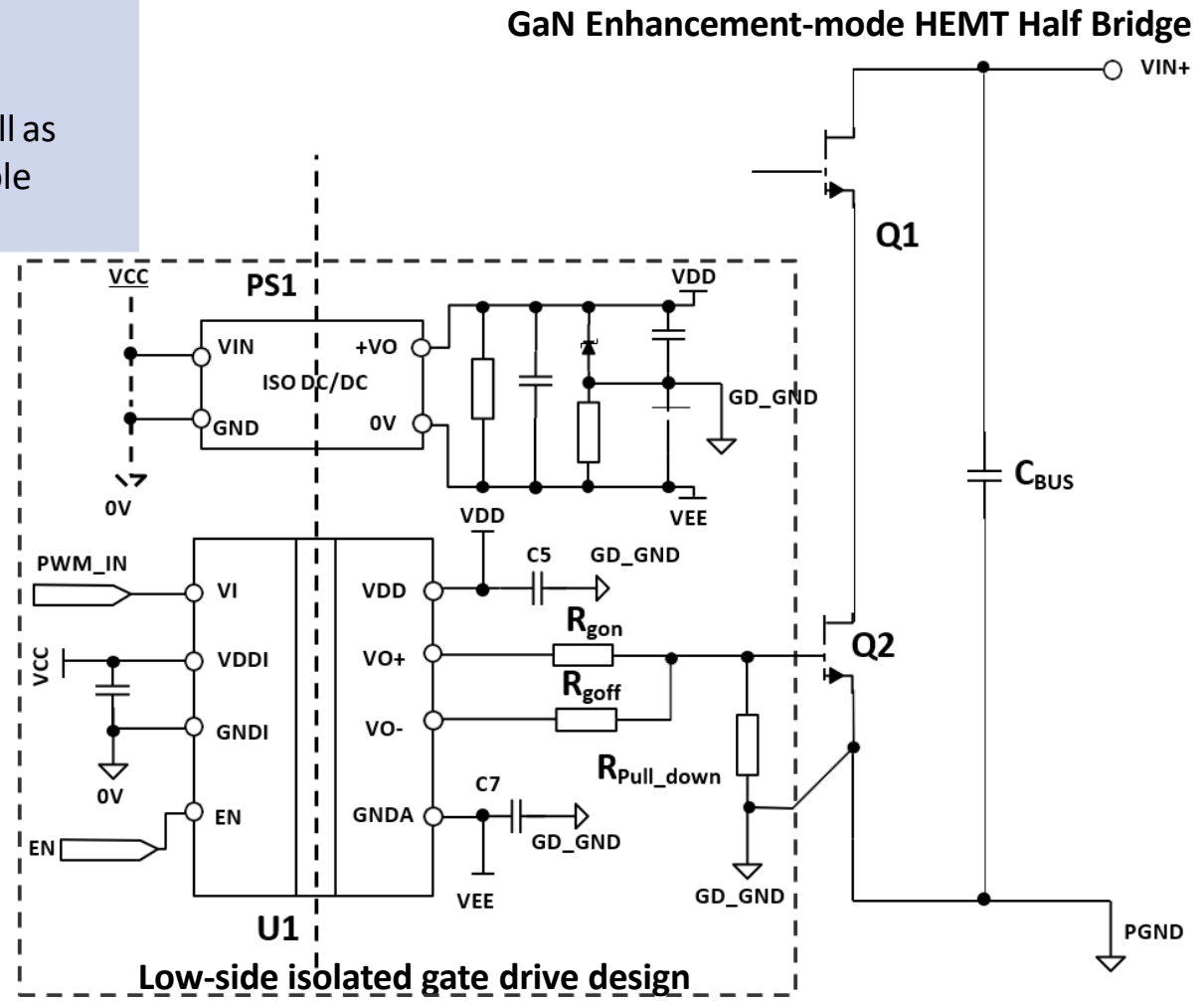
Isolated gate driver circuit for single GaN HEMT

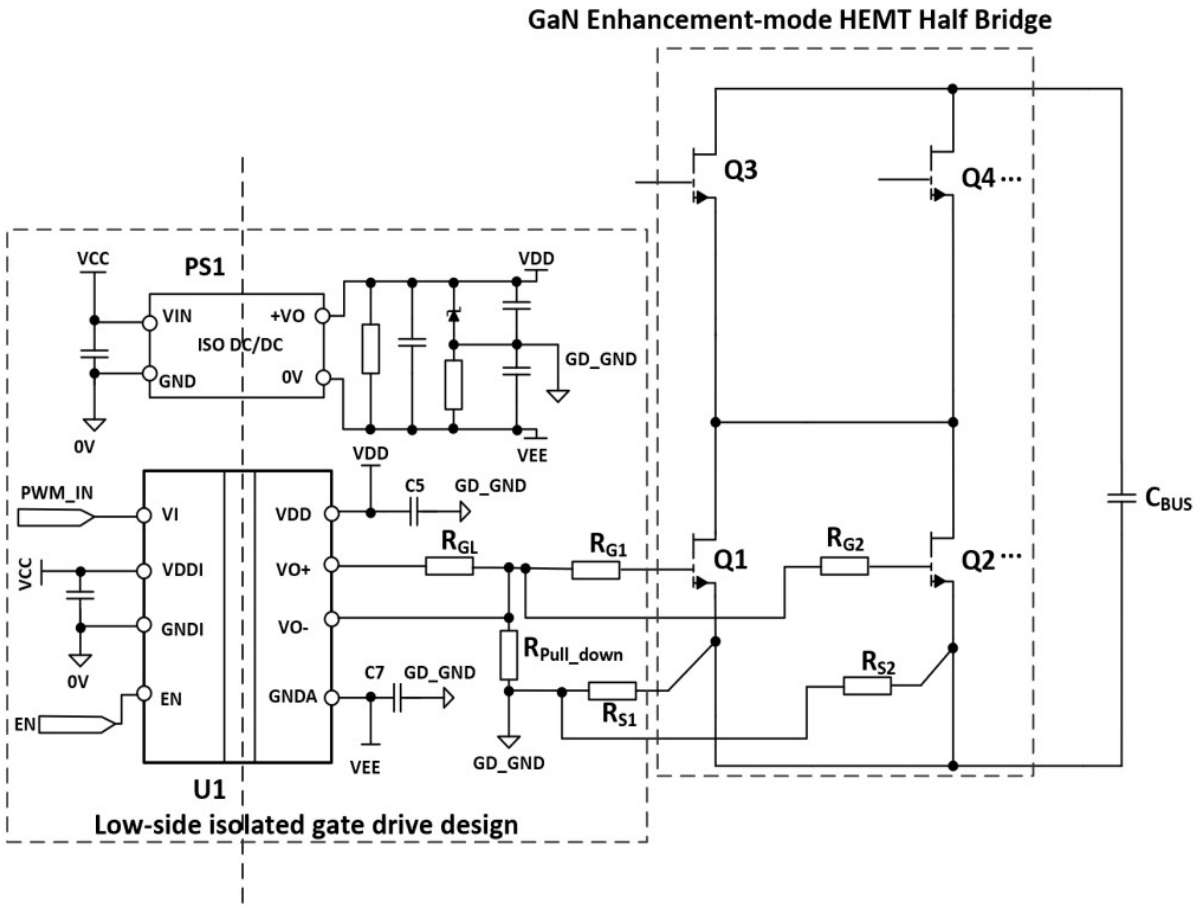
Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation loop	Q1,Q2,C_{BUS}	As small as possible
2a	LS Gate Driver loop (turn-on)	C5,U1,R_{gon},Q2	
2b	LS Gate Driver loop (turn-off)	C7,U1,R_{goff},Q2	

- High-side isolated gate drive design is symmetric as Low-side, not shown in the diagram
- Priority of HS gate driver loop is same as LS



Isolated gate driver circuit for paralleled GaN HEMTs

Priority	Critical Loops	Components	Critical Loops Design Rule
1a	Quasi-common source loop (high-side)	Q3, Q4	As small and symmetric for each of paralleled devices as possible
1b	Quasi-common source loop (low-side)	Q1, Q2	
2	Power Commutation loop	C_{BUS}, Q3/Q4, Q1/Q2	
3a	LS Gate Driver loop (turn-on)	C5, U1, RGL, R_{G1}/Q1/R_{S1}, R_{G2}/Q2/R_{S2}	
3b	LS Gate Driver loop (turn-off)	C7, U1, R_{G1}/Q1/R_{S1}, R_{G2}/Q2/R_{S2}	

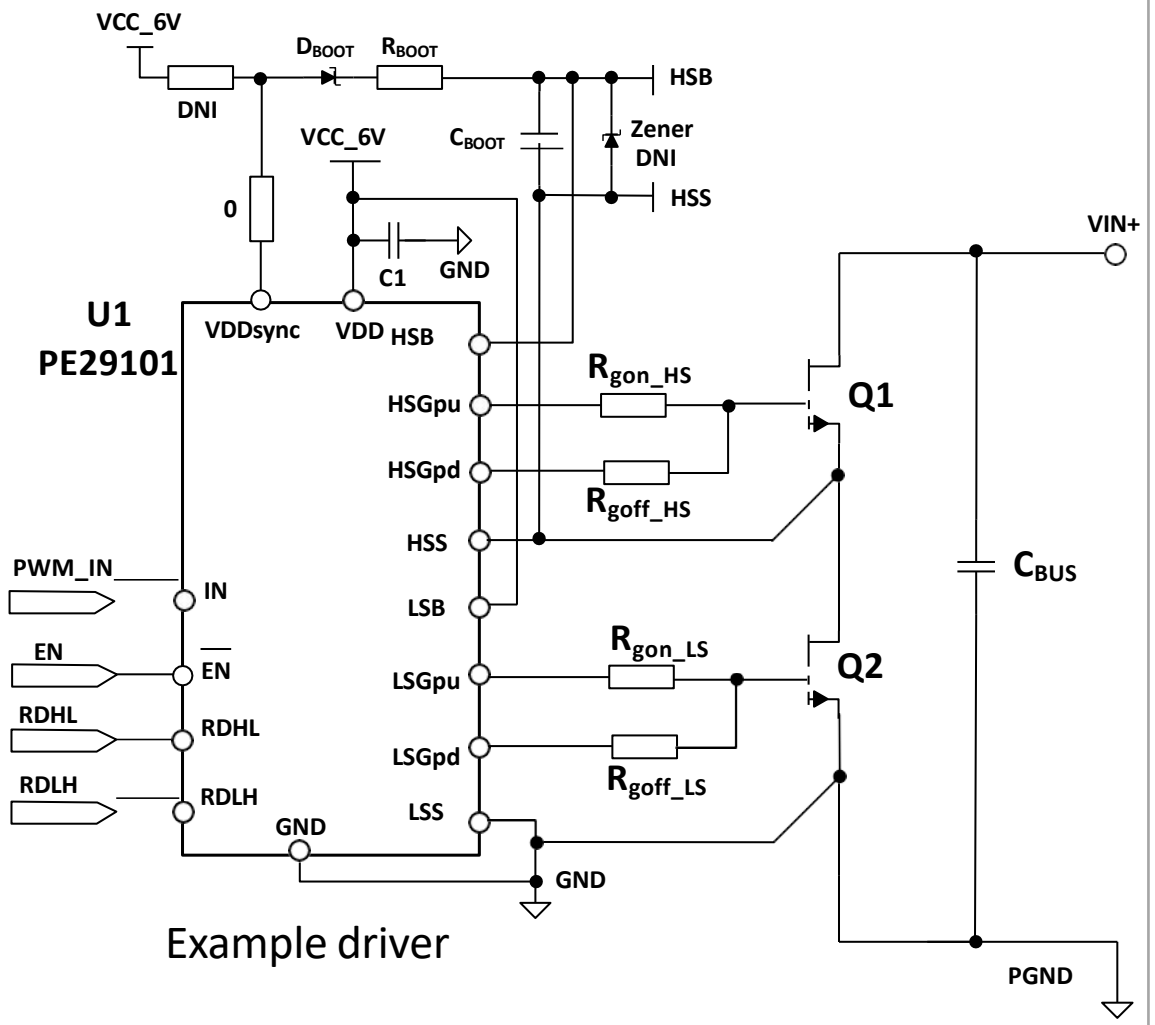


- High-side isolated gate drive design is symmetric as Low-side, not shown in the diagram
- Priority of HS gate driver loop is same as LS
- **Distributed gate and source resistance R_{G1}/ R_{G2} and R_{S1}/ R_{S2} needs to be separated**

Half-bridge Bootstrap Gate Driver Circuit (Non-isolated)

Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation loop	Q1, Q2, C_{BUS}	As small as possible
2a	HS Gate Driver Loop (turn-on)	D_{BOOT}, R_{BOOT}, C_{BOOT}, U1, R_{gon_HS}, Q1	
2b	HS Gate Driver Loop (turn-off)	Q1, R_{goff_HS}, U1	
2c	LS Gate Driver Loop (turn-on)	C1, U1, R_{gon_LS}, Q2	
2d	LS Gate Driver Loop (turn-off)	Q2, R_{goff_LS}, U1	

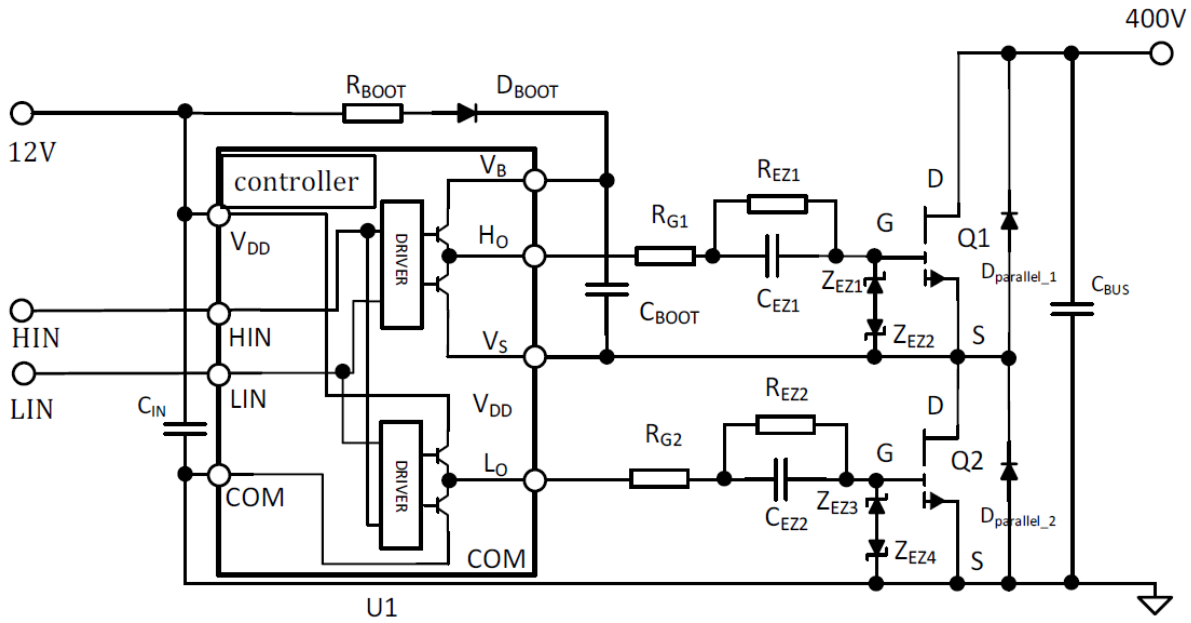
Use above table to identify critical loop, components and priority



Example driver

EZDrive^{SM} circuit (Non-isolated half-bridge)

Priority	Critical Loops	Components	Critical Loops Design Rule
1	Power Commutation Loop	Q1, Q2, C_{BUS}	As small as possible
2a	HS Gate Driver Loop (turn-on)	R_{BOOT}, D_{BOOT}, C_{BOOT}, U1, R_{G1}, R_{EZ1}, C_{EZ1}, Z_{EZ1}, Z_{EZ2}, Q1	
2b	HS Gate Driver Loop (turn-off)	Q1, Z_{EZ1}, Z_{EZ2}, R_{EZ1}, C_{EZ1}, R_{G1}, U1	
2c	LS Gate Driver Loop (turn-on)	U1, R_{G2}, R_{EZ2}, C_{EZ2}, Z_{EZ3}, Z_{EZ4}, Q2	
2d	LS Gate Driver Loop (turn-off)	Q2, Z_{EZ3}, Z_{EZ4}, R_{EZ2}, C_{EZ2}, R_{G2}, U1	



Simplified diagram: controller w/ integrated driver

Use above table to identify critical loop, components and priority

Note: more details about EZDrive^{SM} is available from the link:
https://gansystems.com/wp-content/uploads/2018/12/GN010-EZDrive-Solution-for-GaN-Systems-E-HEMTs-_20181221.pdf

PCB Layout Steps

- **Step 1:** Prepare the schematics and identify the components of each critical loop
  - Isolated gate driver circuit for single GaN HEMTs
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- **Step 2:** Place the components according to the design priority and current direction
  - Put components as close as possible
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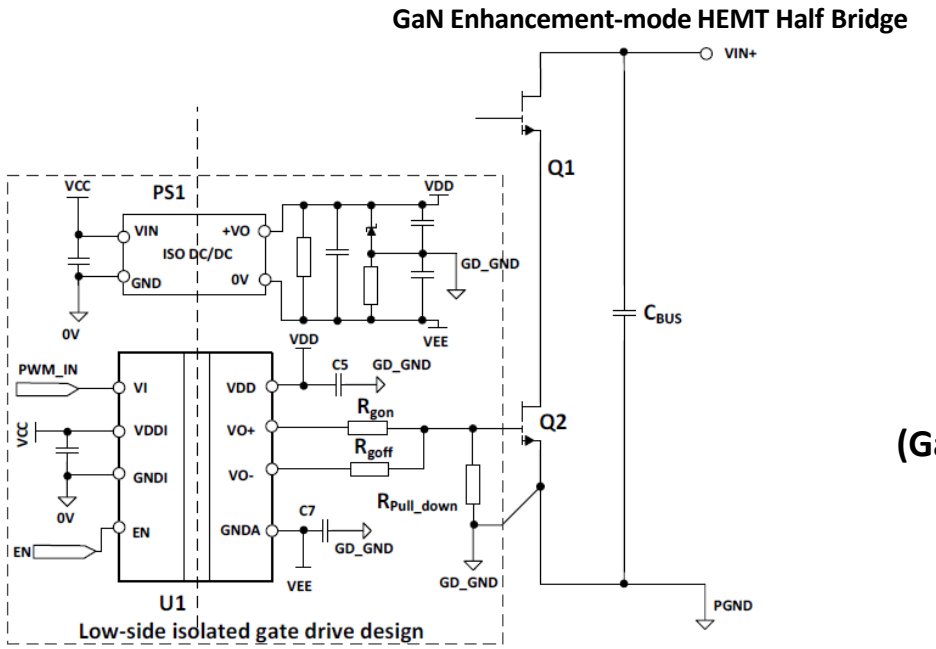
  - If there is a conflict for minimizing all the loops, refer to the priority listed on slides 7/8/9/10.
- **Step 3:** Connect the components optimally to achieve low parasitics with flux cancellation techniques

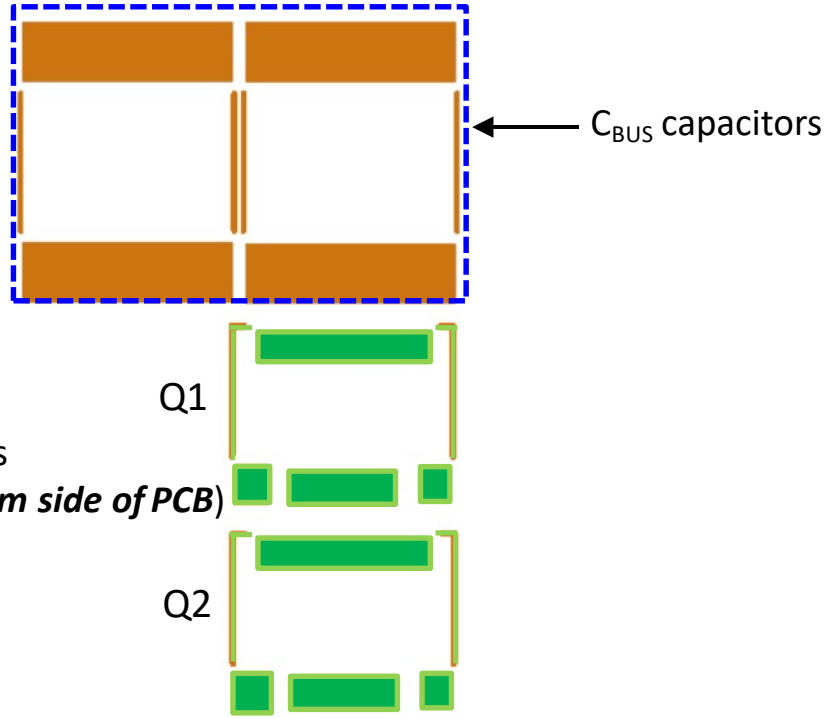
Step 2.1: Power commutation loops (Top-side cooling)

Example: Isolated gate driver circuit w/ single GaN HEMT

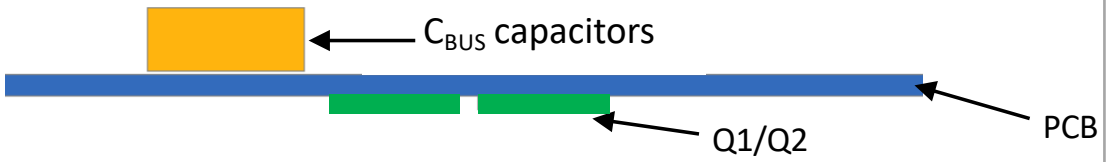
- Place components as close together as possible



Component Placement



Top-side cooled devices
(GaN HEMT *Q1/Q2 are on the bottom side of PCB*)



Side view

Priority	Critical Loops	Components	Critical Loops Design Rule
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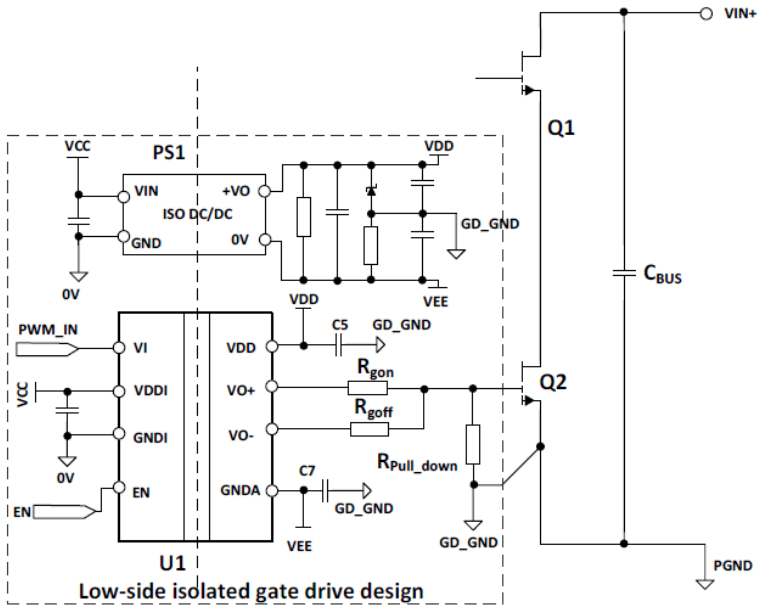
Step 2.2: Gate Driver Circuit Loop (Top-side cooling)

Example: Isolated gate driver circuit w/ single GaN HEMT

- Locate drivers close to the gate
- Use/create kelvin source for driver return

GaN Enhancement-mode HEMT Half Bridge



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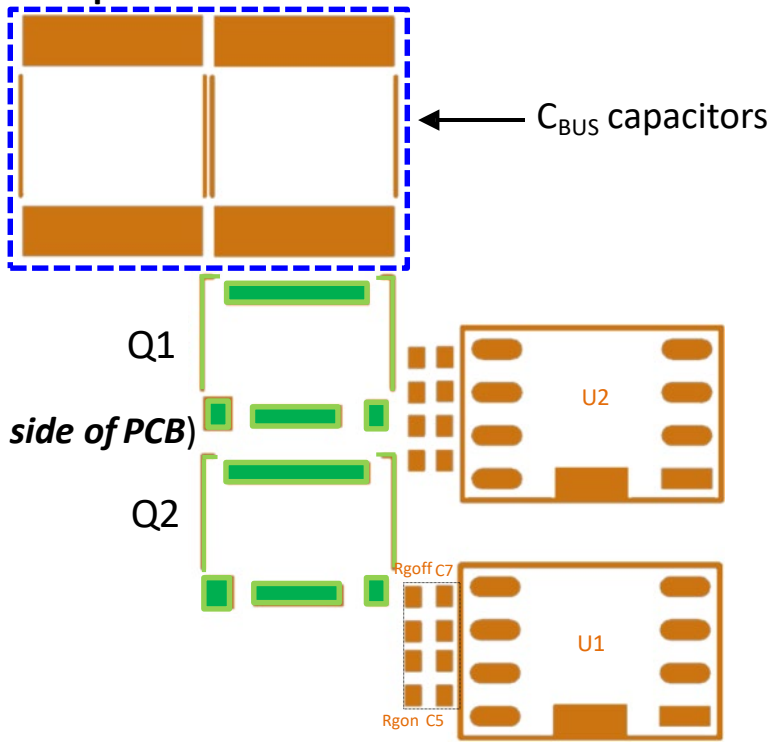

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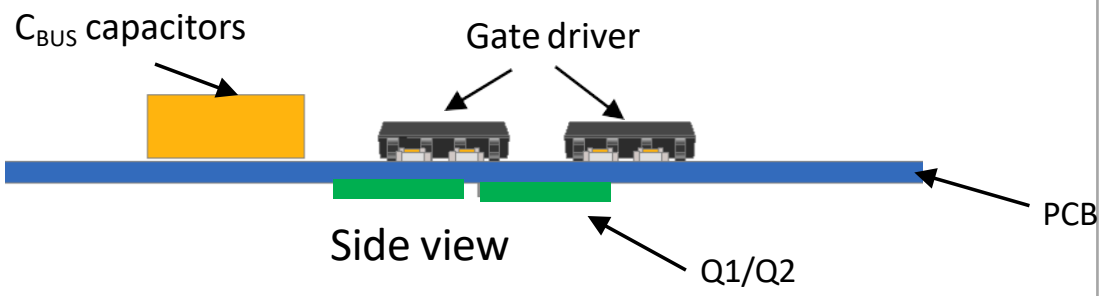

Step 2.1: Power commutation loops (Bottom-side cooling)

Example: Isolated gate driver circuit w/ single GaN HEMT

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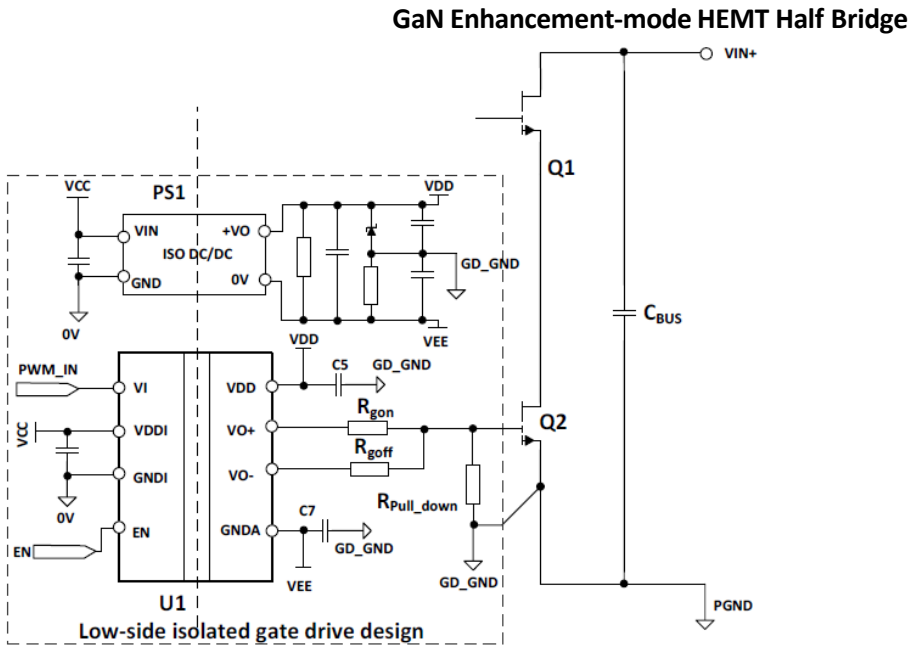

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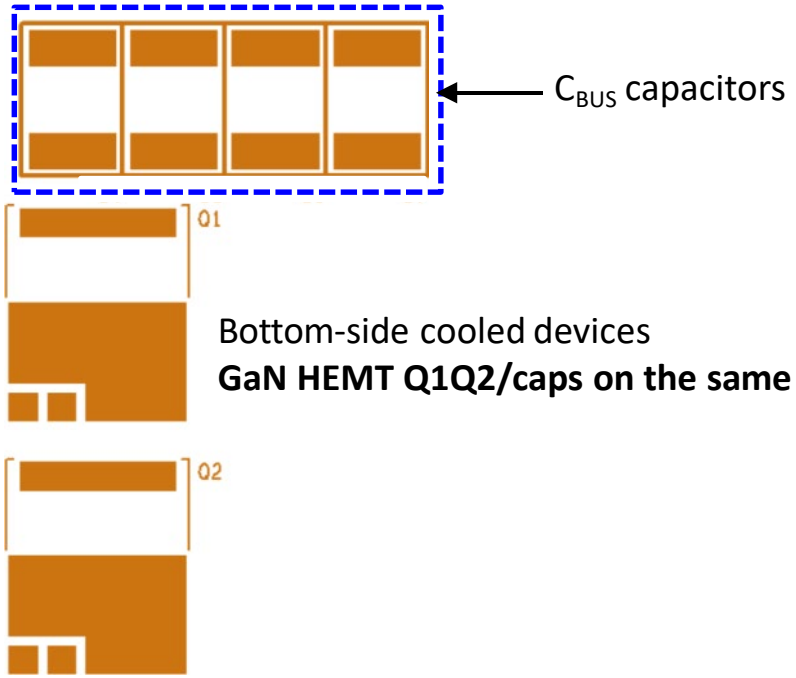

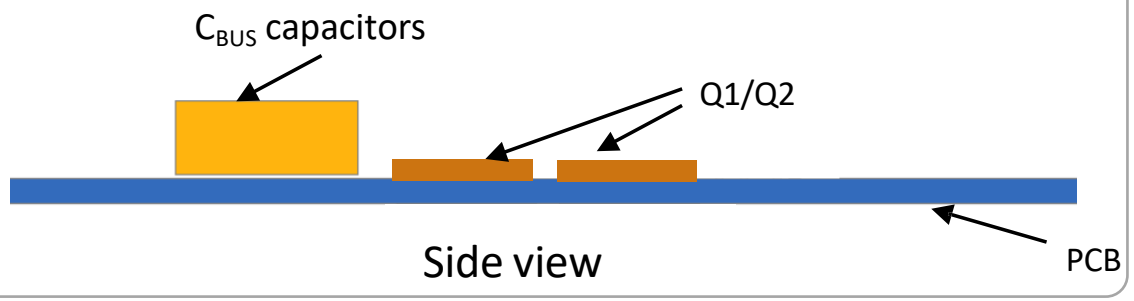

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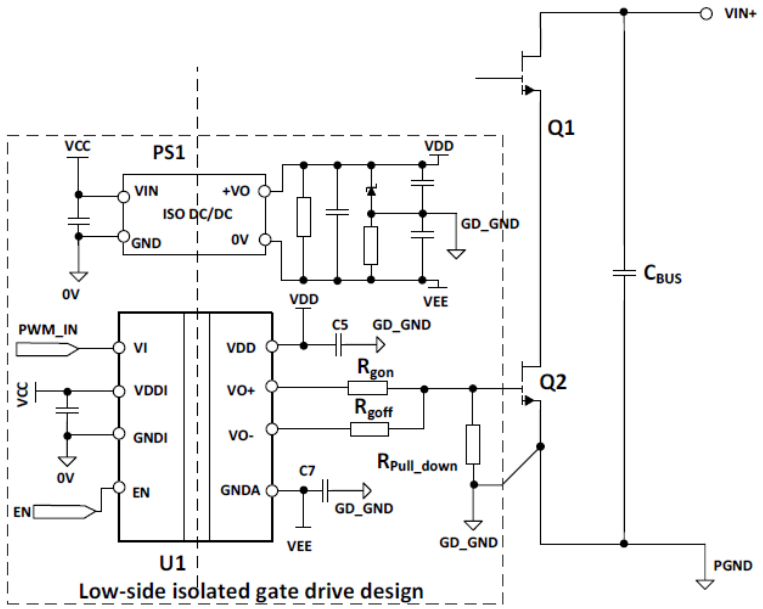

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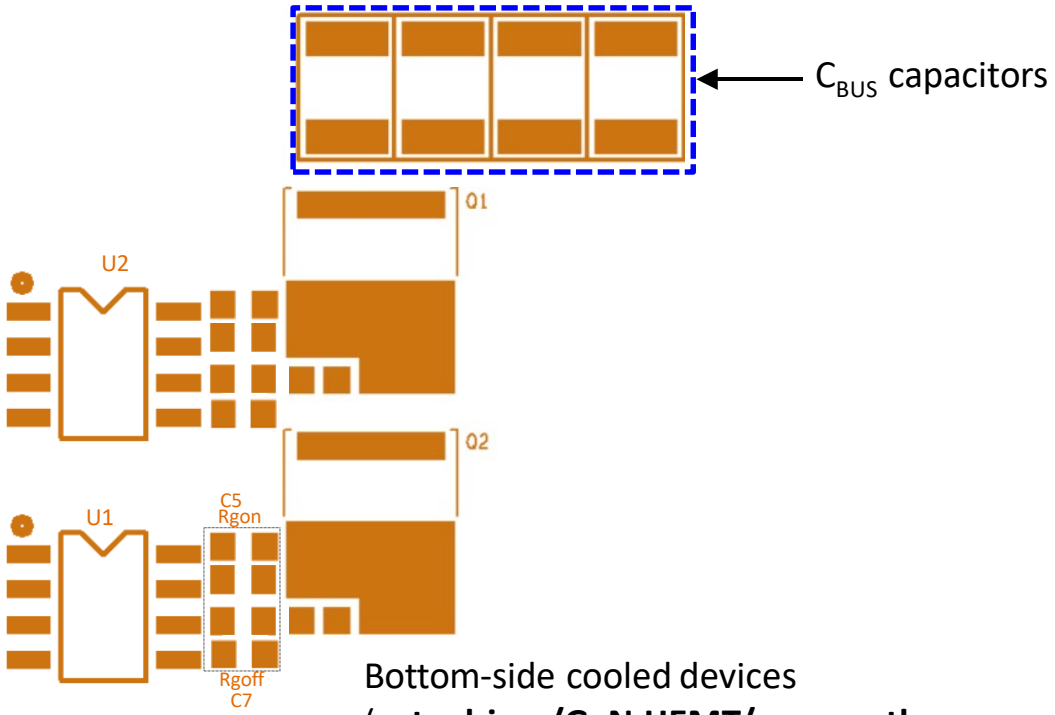
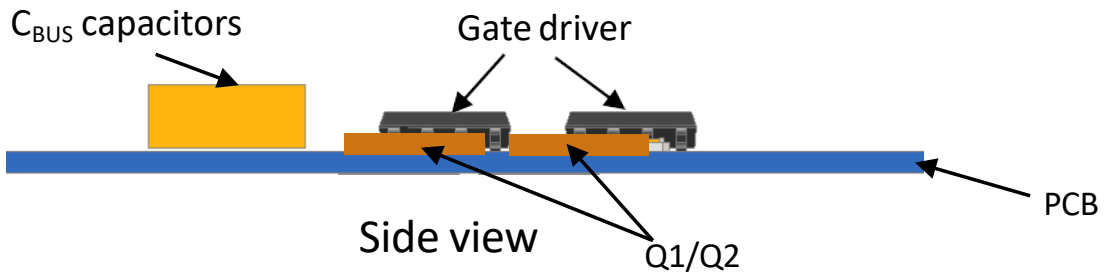


Bottom-side cooled devices
(gate driver/GaN HEMT/caps on the same side of PCB)



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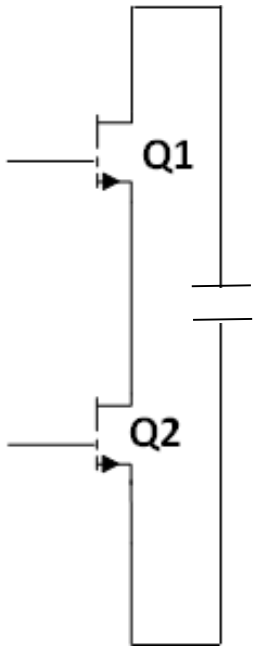
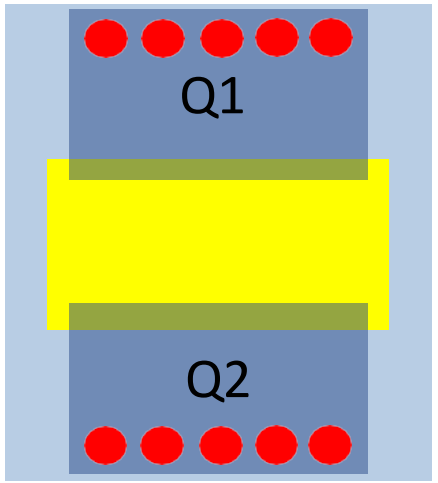
Step 3.1: Introduction - Magnetic Flux Cancellation for Lower Inductance

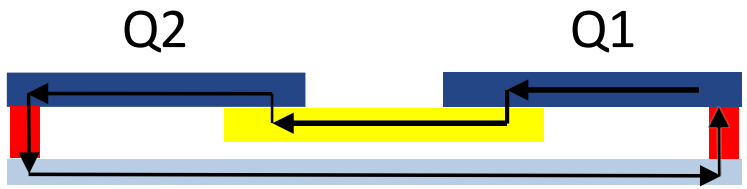
- When two adjacent conductors are located close with opposite current direction, magnetic flux generated by two current flows will cancel each other.
- This magnetic flux canceling effect can lower the parasitic inductance.
- Arrange the layout so that high-frequency current flows in opposite direction on two adjacent PCB layers.





Top View

Components
Top layer of PCB
Bottom layer of PCB
Via

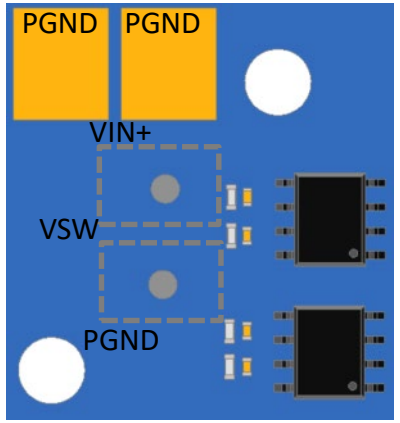


Side View

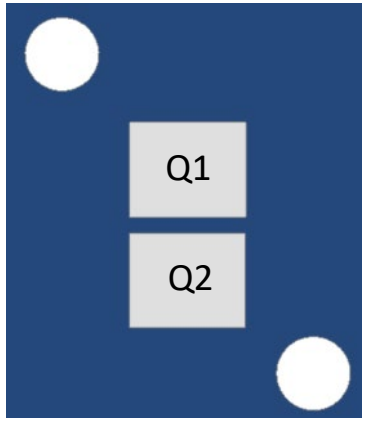
Step 3.2: Connect the components with Flux-cancelling traces

- Connect the components with Flux-cancelling traces, see below example of top-side cooled devices and bottom-side cooled devices.

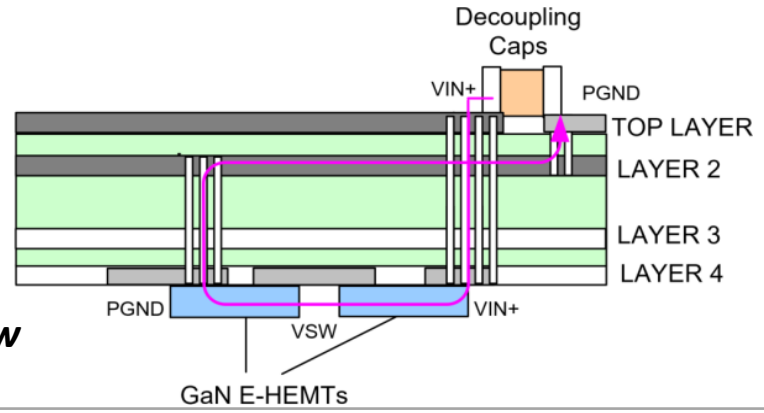
Example: Top-side cooled devices (*GaN HEMT is on the bottom side of PCB*)



Top view

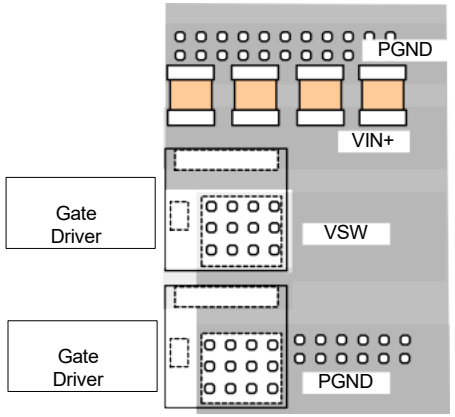


Bottom view

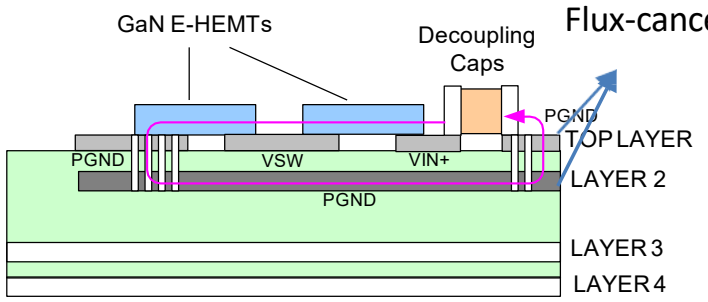


Side view

Example: Bottom-side cooled devices (gate driver/GaN HEMT/caps on the same side of PCB)



Top view



Side view

Use layer 2 as ground return (4-layer PCB)

Experimental Example: 400V/240A DPT Hard-switching Test

DUT: 4 x GS66516T in parallel.

Freewheeling: 4 x GS66516T in parallel

Test conditions

V_{BUS} = 400 V

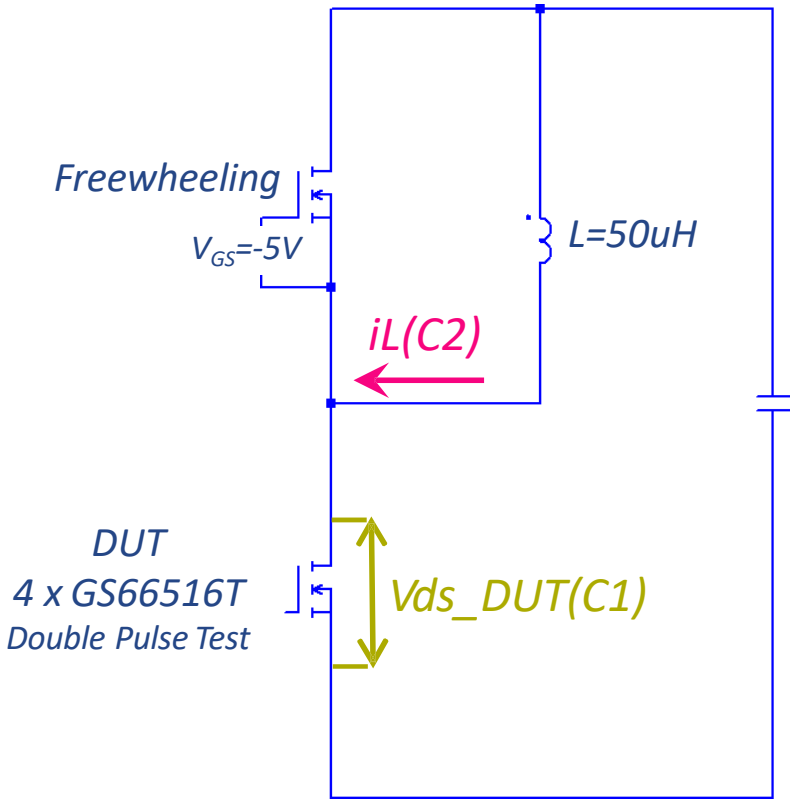
I_{DS_ON} = 231 A

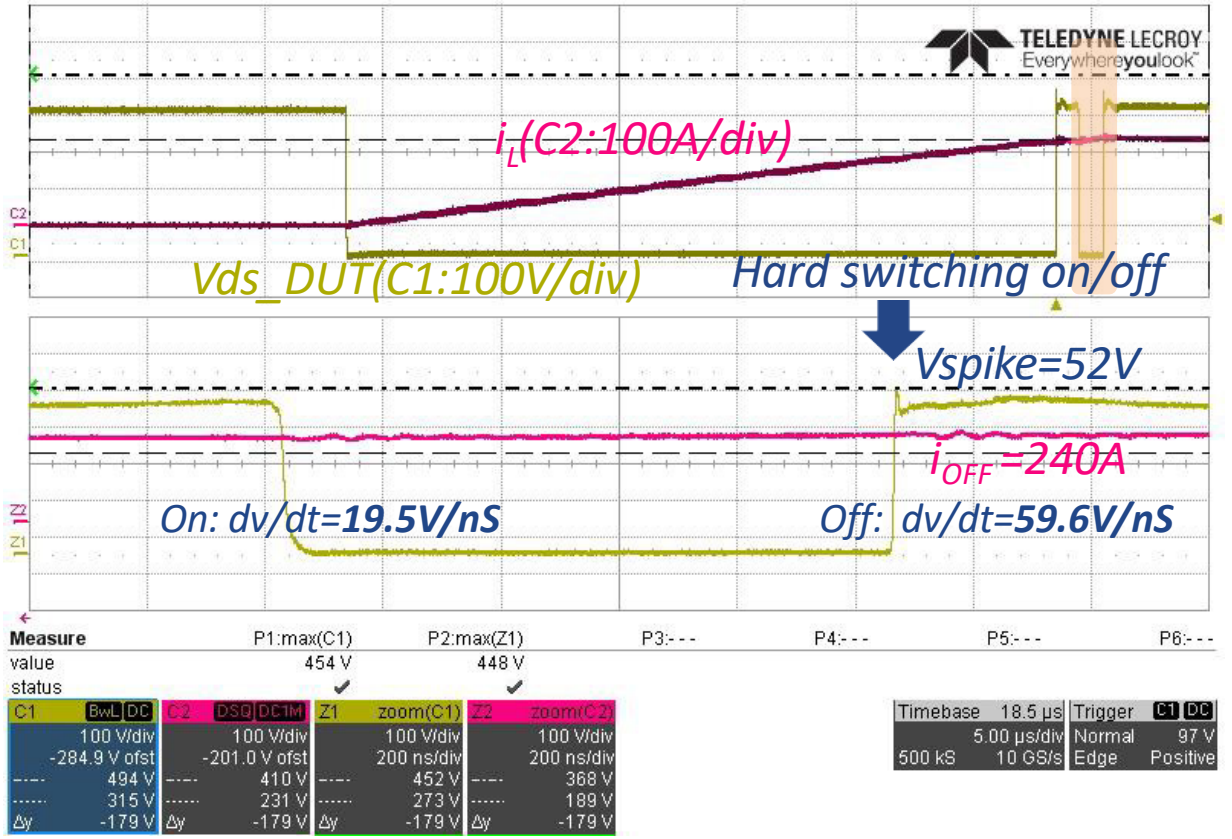
I_{DS_OFF} = 240 A

V_{GS} = +6.8 V/-5 V

R_{G_ON} = 4.55 Ω

R_{G_OFF} = 1.25 Ω





Measurement Setup: Lecroy WaveSurfer 10M Oscilloscope, HVD3106 Differential Probe(C1), CWT-3LFB mini Rogowski Coil(C2)

- Using good engineering practice for PCB layout in designs where GaN Systems' E-HEMTs are paralleled, current balancing and clean switching can be achieved. Hard switched is possible to full rated current.
- This example demonstrates ~200V V_{DS} margin on a 400V/240A hard-switching test

Summary

- Due to faster switching speed of GaN E-HEMTs, good engineering practice for PCB layout techniques are required to minimize parasitic inductance and fully utilize these advanced devices.

- Optimizing the PCB layout is important to achieve the maximum performance capability of GaN based designs. With optimum board layout combined with low GaN*PX*® package inductance, GaN Systems' E-HEMTs exhibit peak switching performance.

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