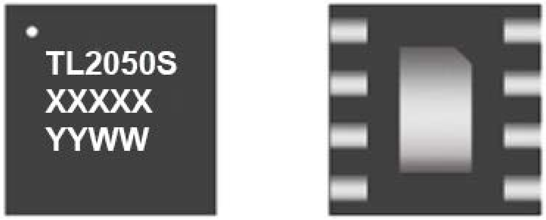
TDLNA2050SEP: 2.0 – 5.0 GHz GaAs Ultra Low Noise Amplifier

1.0 Features

- Small signal gain @ 3600MHz: 17.5 dB
- NF @ 3600 MHz: 1.5 dB
- OP1dB @ 3600 MHz: 12.0 dBm
- OIP3dB @ 3600 MHz: 33.0 dBm
- 5 V Typical operating voltage
- Operating frequency: 2.0 to 5.0 GHz



Top Side

Bottom Side

Figure 1.1 Device Image
(8 Pin 2×2×0.75 mm QFN Package)

RoHS/REACH/Halogen Free Compliance

2.0 Applications

- 4G/5G Infrastructure Radios
- Small Cells and Cellular Repeaters
- Phased Array Radar
- SDARS

3.0 Description

The TDLNA2050SEP is a high frequency version of TDLNA0430SEP which is a broadband, ultra-low Noise Amplifier (LNA). With a simple input and output match, this LNA can be tuned for different frequency bands targeting LTE (small cells and infrastructure), radar and any other applications requiring low noise, high gain, and linearity.

The TDLNA2050SEP is packaged in a compact, low-cost Dual Flat No Lead (DFN) 2 x 2 x 0.75 mm, 8-pin, plastic package.

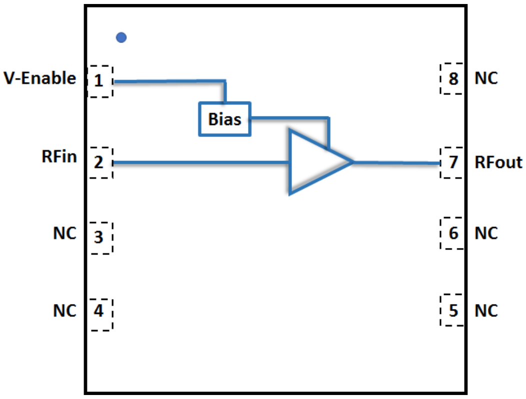


Figure 3.1 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 4.1 Ordering Information

Number	Package Type	Orderable Part Number
TDLNA2050S	8 Pin 2×2×0.75 mm DFN	TDLNA2050SEP
Tuned Evaluation Board, 3300 - 3800 MHz		TDLNA2050SEP-EVB-A
Tuned Evaluation Board, 3700 - 4200 MHz		TDLNA2050SEP-EVB-B
Tuned Evaluation Board, 4400 - 5000 MHz		TDLNA2050SEP-EVB-C
Tuned Evaluation Board, 2900 - 3300 MHz		TDLNA2050SEP-EVB-D

5.0 Pin Description

Table 5.1 Pin Definition

Pin Number	Pin Name	Description
3-6, 8	NC	No internal connection, can be connected to ground
1	V_{enable}	V_{enable} along with series resistor, sets the Idq. V_{enable} <0.2V disables the device
2	RF_{IN}	RF Input. DC blocking cap required
7	RF_{OUT}/V_{dd}	RF Output. Vdd supplied through an external choke inductor
Package Base	Paddle/Slug	DC and RF Ground. Also provides thermal relief. Multiple vias are recommended

Note: [1] The backside ground slug of the device must be grounded directly to the ground plane through multiple vias to ensure proper operation. Adequate heatsinking required.

6.0 Absolute Maximum Rating

Table 6.1 Absolute Maximum Rating @T_A = +25 °C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Supply voltage, V_{enable}	V_{dd}	+6	V
Drain current	I_{DQ}	70	mA
RF input power CW	RF_{IN}	23	dBm
Storage Temperature Range	T_{st}	-55 to +150	°C
Operating Temperature Range	T_{op}	-40 to +105	°C
Maximum Junction Temperature	T_J	170	°C
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	15.0	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

7.0 Recommended DC Operating Conditions

Table 7.1 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Drain Voltage	V_{DD}		+5.0		V
Venable Voltage	V_{enable}		+5.0		V
Drain Bias Current	$I_{DQ,}$ Set by external resistor	45	60		mA
Venable Bias Current	I_{bias}		3.0		mA
Operating Temperature Range		-55	+25	+125	°C

8.0 Switching Time

Table 8.1 Switching time.

Parameter	Test Condition	Typical	Unit
Switching Rise Time /1	10/90% of the RF value	300	nsec
Switching Fall Time /1	10/90% of the RF value	350	nsec

9.0 RF Electrical Specifications

Table 9.1 EVB A 3300-3800MHz

Venable = 5 V, Idd = 60 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band	13		22	dB
Noise Figure /1	Across Band		1.5		dB
EVB Noise Figure /1	Across Band		0.45 - 0.55		dB
Input Return Loss	Across Band	-14			dB
Output Return Loss	Across Band		-10		dB
OP1dB	Across Band	-12			dBm
OIP3 /1	Across Band ,0dBm per tone, Tone Spacing 1 MHz		33		dBm

All parametric data displayed in Tables 7.1 to 9.1 designated with /1 footnote are not tested in Production.

Table 9.2 EVB B 3700-4200MHz

Venable = 5 V, Idd = 60 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		15.5-16.5		dB
Noise Figure	Across Band		0.5-0.6		dB
EVB Noise Figure	Across Band		0.6-0.7		dB
Input Return Loss	Across Band		-8 to -12		dB
Output Return Loss	Across Band		- 8 to -12		dB
OP1dB	Across Band		19-20.5		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1 MHz		33-34		dBm

All parametric data displayed in Tables 9.2 to 9.4 are not tested in Production.

Table 9.3 EVB C 4400-5000 MHz

Venable = 5 V, Idd = 60 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band		16		dB
Noise Figure	Across Band		0.55-0.65		dB
EVB Noise Figure	Across Band		0.7-0.8		dB
Input Return Loss	Across Band		10.4-12.4		dB
Output Return Loss	Across Band		7.5-9		dB
OP1dB	Across Band		18-20		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1 MHz		33-36		dBm

Table 9.4 EVB D 2900-3300 MHz

Venable = 5 V, Idd = 65 mA, Vdd = 5 V, @T_A = +25 °C Unless Otherwise Specified

Parameter	Test Condition	Minimum	Typical	Maximum	Unit
Gain	Across Band	13	18.5-17.9		dB
Noise Figure	Across Band	0	0.35-0.45		dB
EVB Noise Figure	Across Band		0.4-0.5		dB
Input Return Loss	Across Band	14	-19 to -13		dB
Output Return Loss	Across Band	2	8.3-6		dB
OP1dB	Across Band	12	19.3-19.4		dBm
OIP3	Across Band, 0dBm per tone, Tone Spacing 1 MHz	20	33.8-35.5		dBm

10.0 Evaluation Board Details

10.1 EVB A 3.3-3.8 GHz

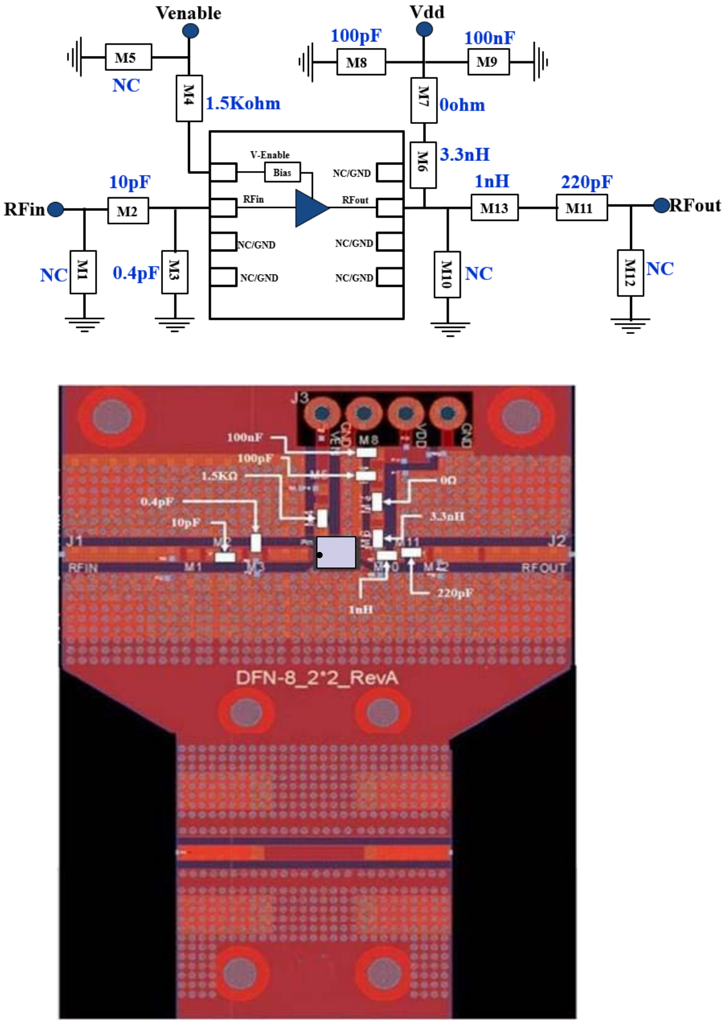


Figure 10.1 Schematic and EVB layout of the 3300-3800 MHz EVB-A

Table 10.1 BOM of the 3300-3800 MHz EVB A

Component ID	Value	Manufacturer	Recommended Part Number
M2	10 pF	Murata	GJM1555C1H100JB01
M3	0.4 pF	Murata	GJM1555C1HR40BB01
M6	3.3 nH	Coil craft	0402HP-3N3XGE
M4	1.5 kΩ	Panasonic	ERJ-2RKF1501X
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M7	0 Ω	Panasonic	ERJ-2GE0R00X
M11	220 pF	Kemet	C0402C221K5GACAUTO
M13	1 nH	coil craft	0402HP-1N0XJE
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.2 EVB B 3.7-4.2 GHz

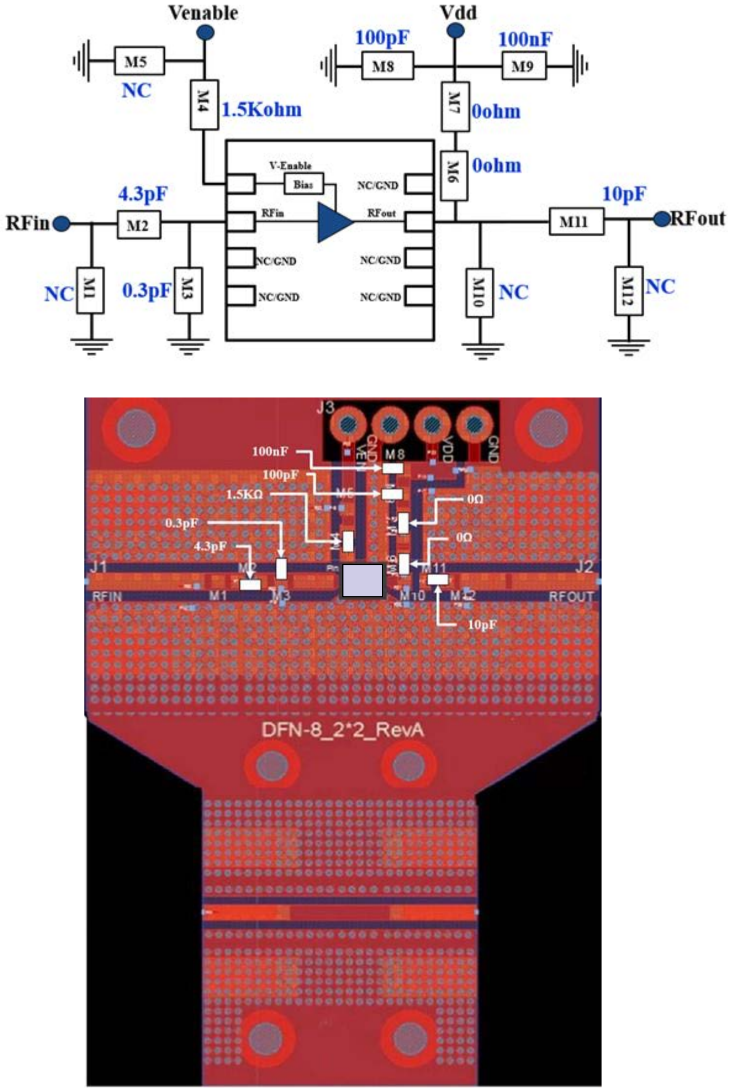


Figure 10.2 Schematic and EVB layout of the 3700-4200 MHz EVB-B

Table 10.2 BOM of the 3700-4200 MHz EVB B

Component ID	Value	Manufacturer	Recommended Part Number
M2	4.3 pF	Murata	GJM1555C1H4R3BB01
M3	0.3 pF	Murata	GJM1555C1HR30BB01
M4	1.5 kΩ	Panasonic	ERJ-2RKF1501X
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M6, M7	0 Ω	Panasonic	ERJ-2GE0R00X
M11	10 pF	AVX	04025A100JAT4A
Q1	GaAs LNA	Teledyne e2v HiRel	TDLNA2050SEP
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.3 EVB C 4.4-5.0 GHz

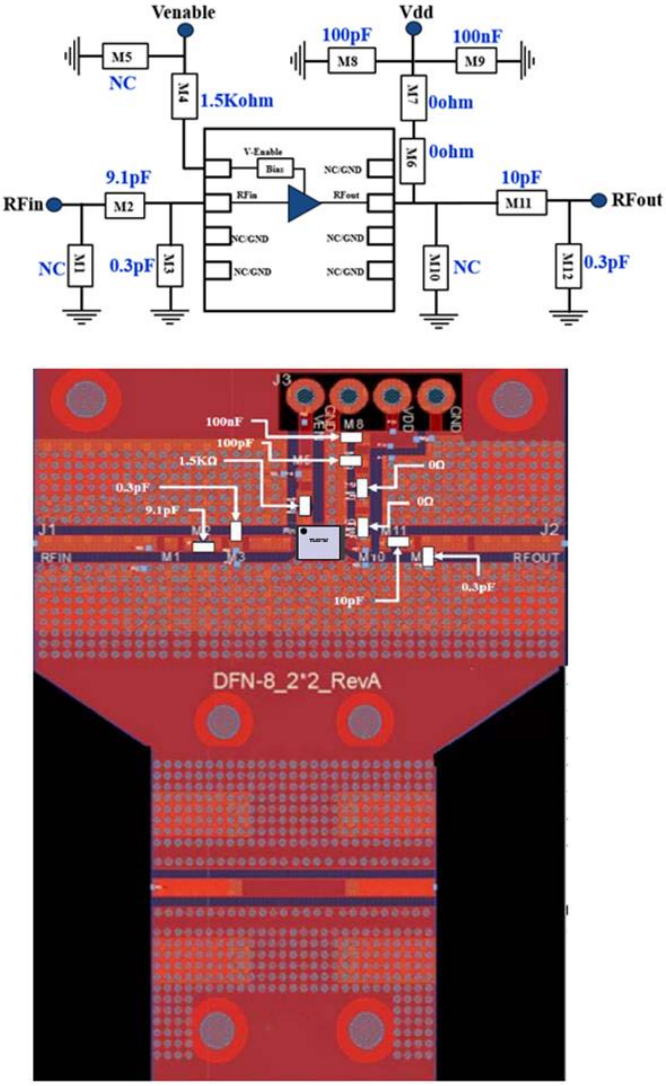


Figure 10.3 Schematic and EVB layout of the 4400-5000 MHz EVB-C

Table 10.3 BOM of the 4400-5000 MHz EVB C

Component ID	Value	Manufacturer	Recommended Part Number
M2	9.1 pF	Murata	GJM1555C1H9R1BB01
M4	1.5 kΩ	Panasonic	ERJ-2RKF1501X
M3	0.3 pF	Murata	GJM1555C1HR30BB01
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M6,M7	0 Ω	Panasonic	ERJ-2GE0R00X
M11	10 pF	AVX	04025A100JAT4A
M12	0.3 pF	Murata	GJM1555C1HR30BB01
Q1	GaAs LNA	Teledyne e2v HiRel	TDLNA2050SEP
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

10.4 EVB D 2.9-3.3 GHz

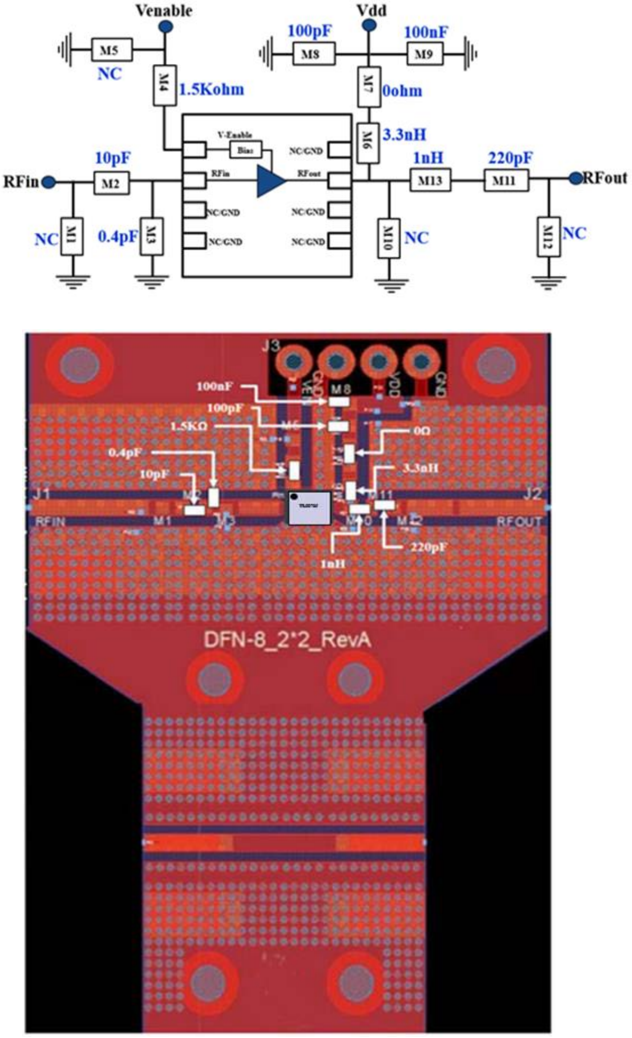


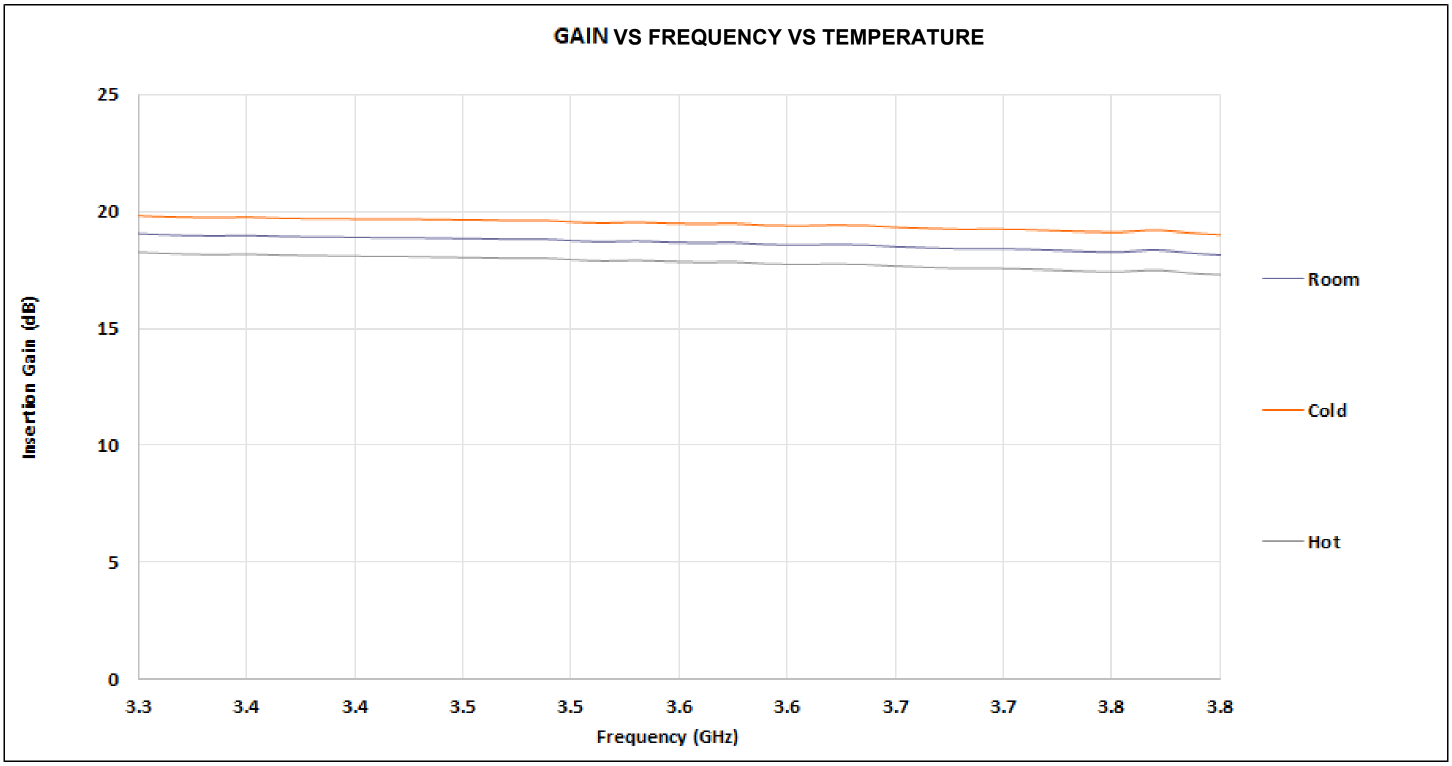
Figure 10.4 Schematic and EVB layout of the 2900-3300 MHz EVB-D

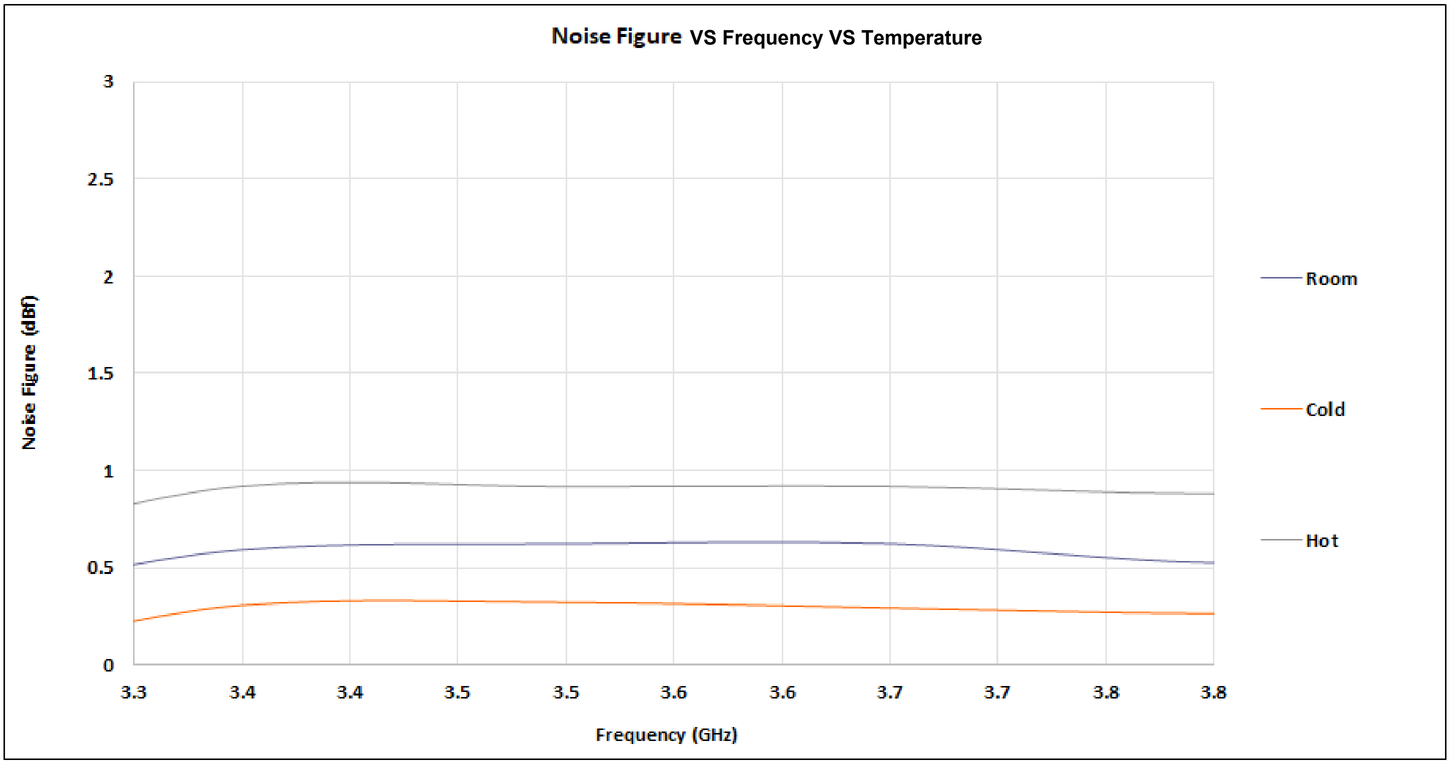
Table 10.4 BOM of the 2900-3300 MHz EVB D

Component ID	Value	Manufacturer	Recommended Part Number
M2	10 pF	Murata	GJM1555C1H100JB01
M3	0.4 pF	Murata	GJM1555C1HR40BB01
M6	3.3 nH	Coil craft / Wurth Electronics	0402HP-3N3XGE / 744916033
M4	1.5 kΩ	Panasonic	ERJ-2RKF1501X
M8	100 pF	AVX	04025A101JAT4A
M9	100 nF	TDK	C1005X7R1H104K050BE
M7	0 Ω	Panasonic	ERJ-2GE0R00X
M11	220 pF	Kemet	C0402C221K5GACAUTO
M13	1 nH	Coil craft / Wurth Electronics	0402HP-1N0XJE /744916010
Q1	GaAs LNA	Teledyne e2v HiRel	TDLNA2050SEP
PCB	Rogers RO4350B, 20 mils, 1 oz copper		

11.0 Typical Characteristics

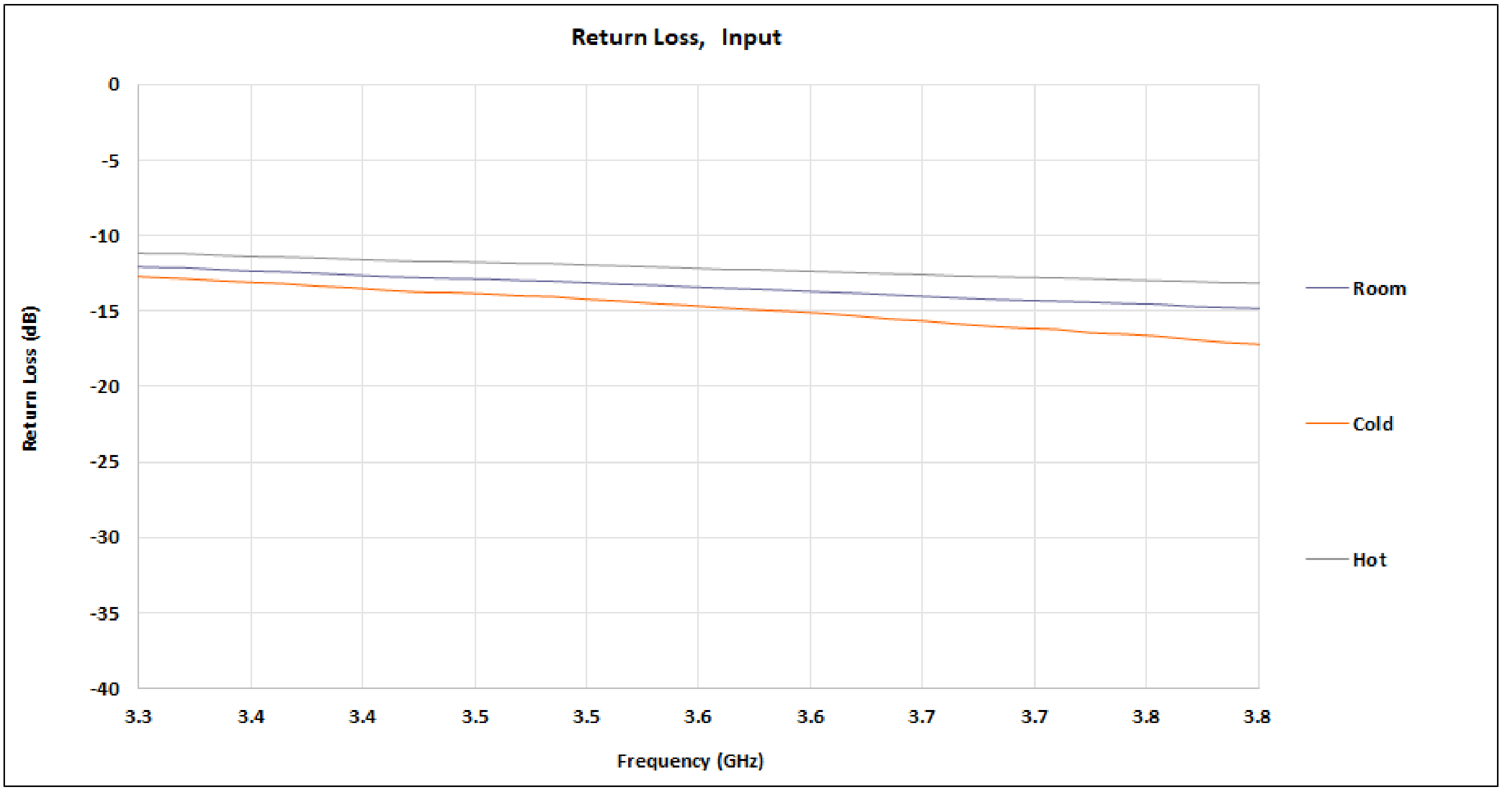
Test Conditions: Vdd = 5 V,, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC

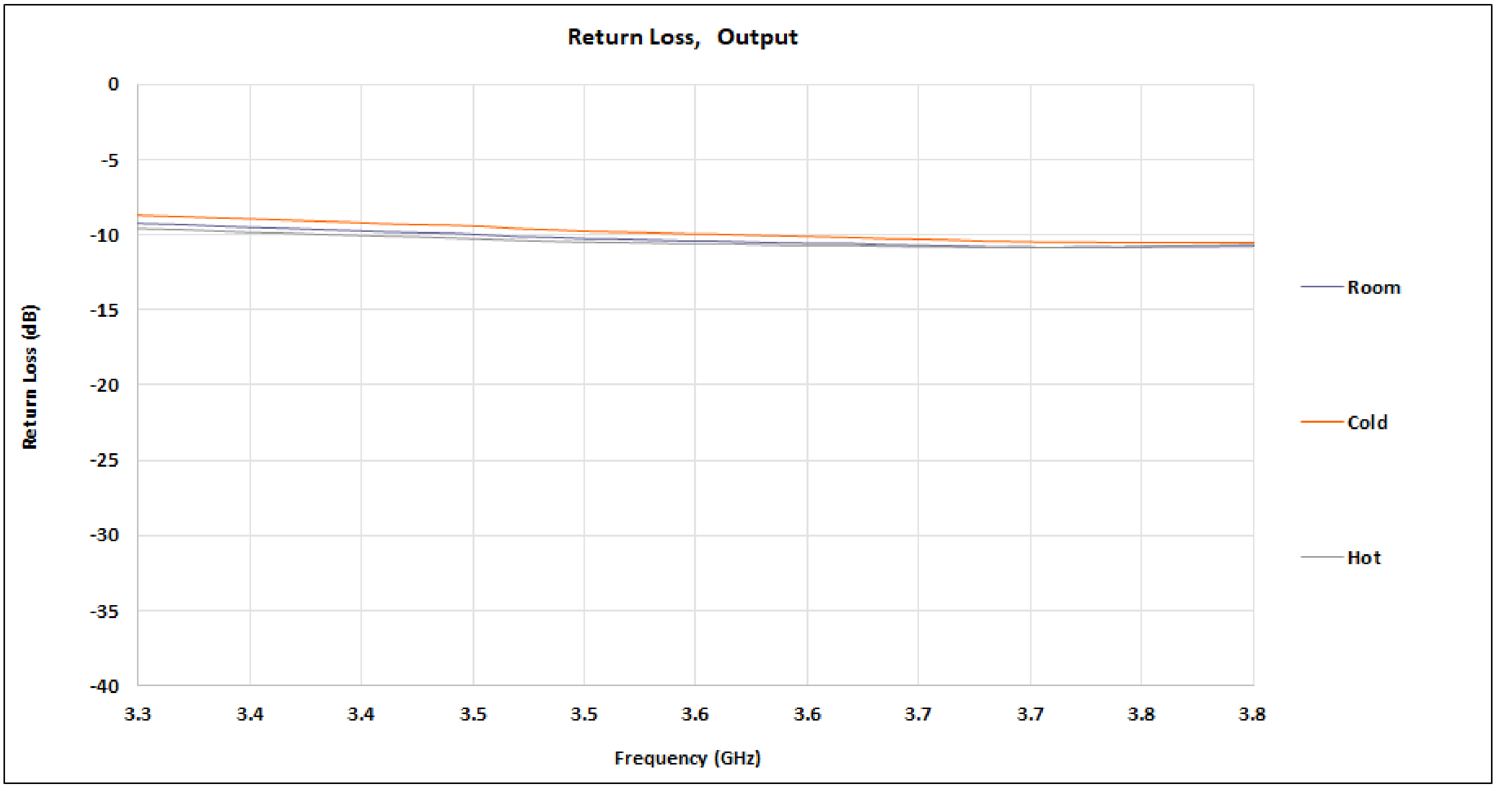




11.0 Typical Characteristics (continued)

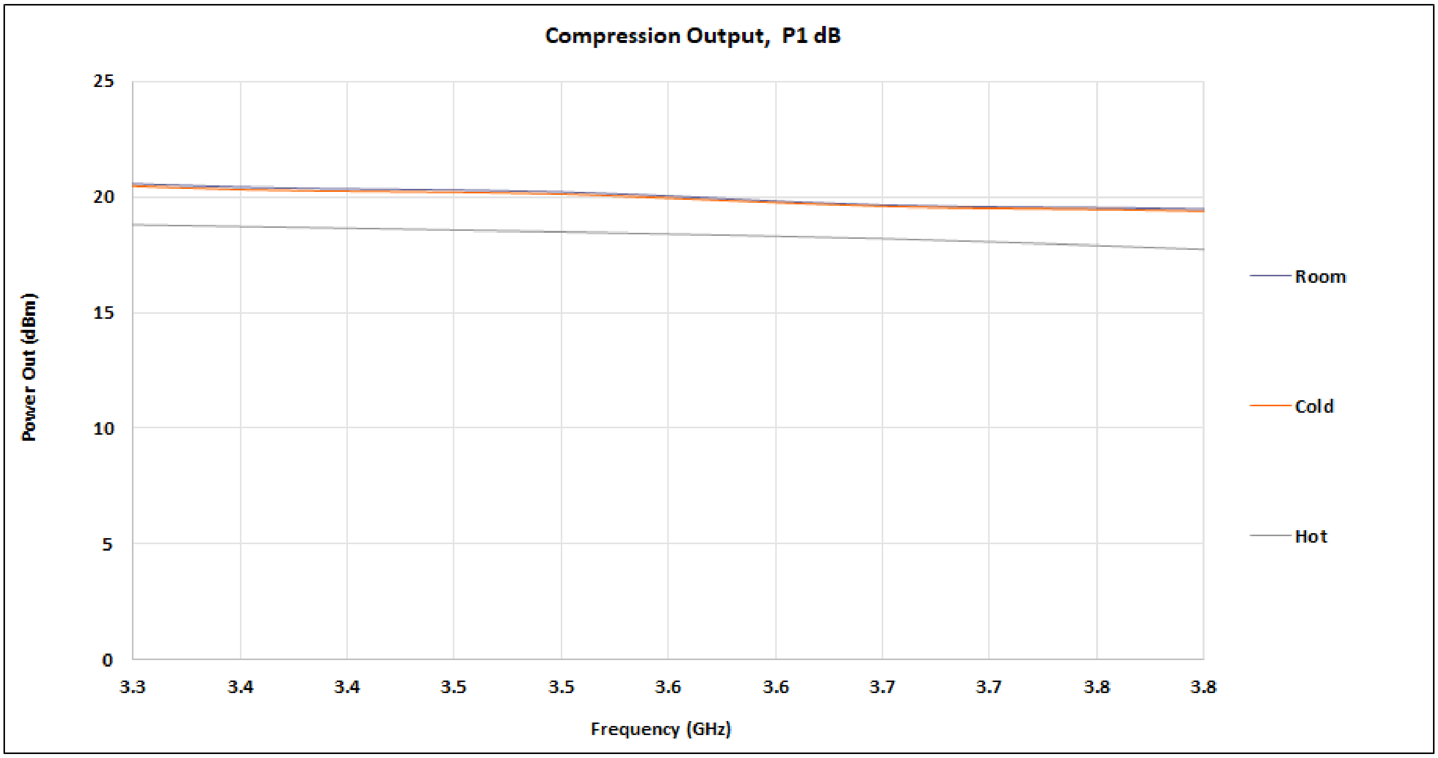
Test Conditions: Vdd = 5 V,, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC

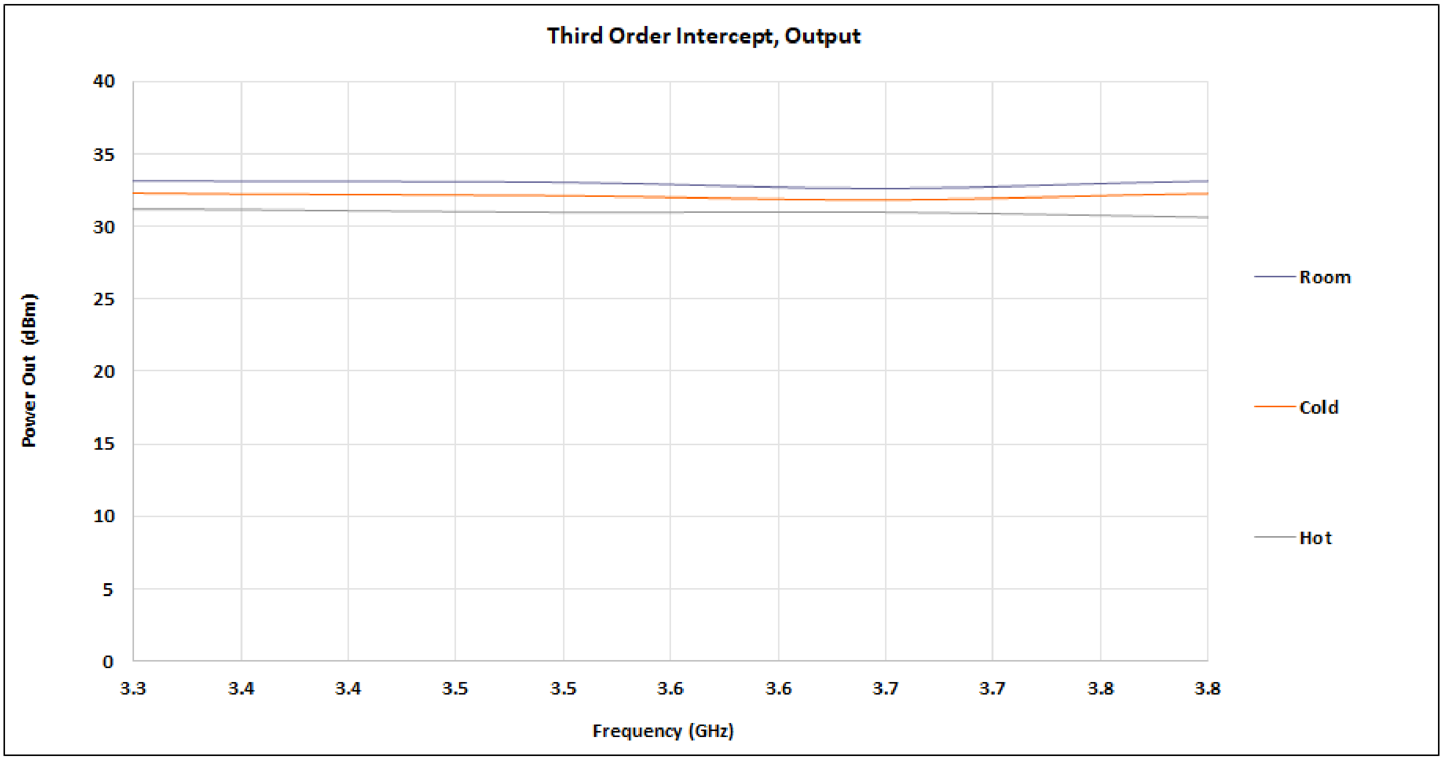




11.0 Typical Characteristics (continued)

Test Conditions: Vdd = 5 V,, Cold = -55 ºC, Room = 25 ºC, Hot = 125 ºC

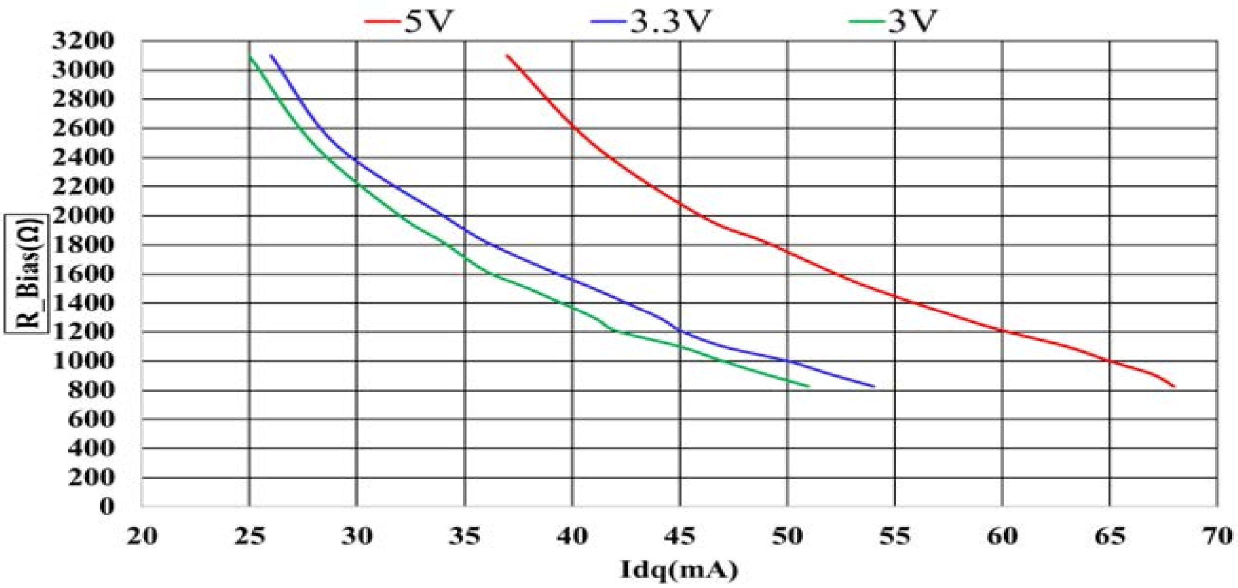




11.0 Typical Characteristics (continued)

Test Conditions: As noted @ Room = 25 ºC

TDLNA2050SEP



Rbias on Venable vs Idq

12.0 Test Procedures

Biasing Sequence

To properly bias the TDLNA2050SEP-EVB-A, follow these steps: Connect the supply Ground the Ground test point.

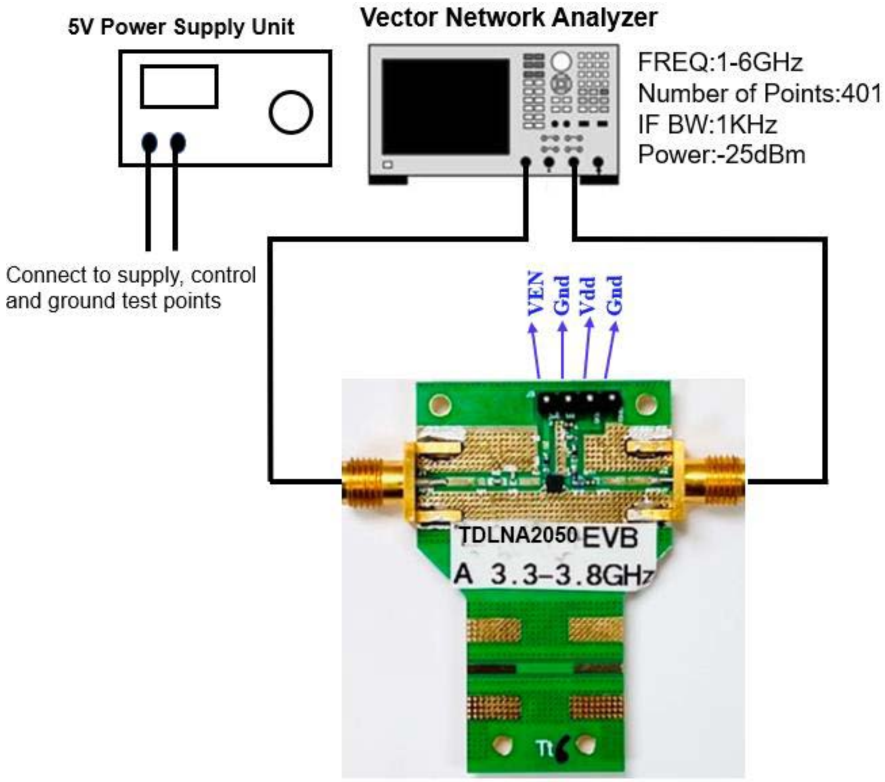
- Apply bias to the Venable = 5 V test points.
- Apply bias to the Vdd = 5 V test point.
- Apply an RF input signal.

The TDLNA2050SEP-EVB-A is shipped fully assembled and tested. Figure 12.1 illustrates a basic test setup diagram for evaluating s-parameters, which includes gain, input output return loss and reverse isolation using a network analyzer. Follow these steps to complete the test setup and verify the operation of the TDLNA2050SEP-EVB-A:

1. Connect the Ground test point to the ground terminal of the power supply.
2. Connect the Venable and Vdd test points to the voltage output terminal of a 5 V supply that sources a current of approximately 60 mA.
3. Connect a calibrated network analyzer to the RF-in, and RF-out SMA connectors. Sweep the frequency from 1 GHz to 6 GHz and set the power to -25 dBm.

The TDLNA2050SEP-EVB-A is expected to have a gain of 17.5 dB at 3.6 GHz. Refer to Figure 11.1.2 for the expected results.
Additional test equipment is required for a comprehensive evaluation of the device's functions and performance.
For noise figure evaluation, use either a noise figure analyzer or a spectrum analyzer with a noise option. It is recommended to use a low excess noise ratio (ENR) noise source.
For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is recommended.
For power compression and power handling evaluations, use a two-channel power meter and a signal generator. Ensure that the input power amplifier has sufficient power capacity. Test accessories such as couplers and attenuators must also have adequate power handling capabilities.

Please note that measurements conducted at the SMA connectors of the TDLNA2050SEP-EVB-A include the losses of the SMA connectors and the PCB. The through line should be measured to calibrate the effects of the TDLNA2050SEP-EVB-A. The through line consists of an RF input line and an RF output line that are connected to the device and have equal lengths.



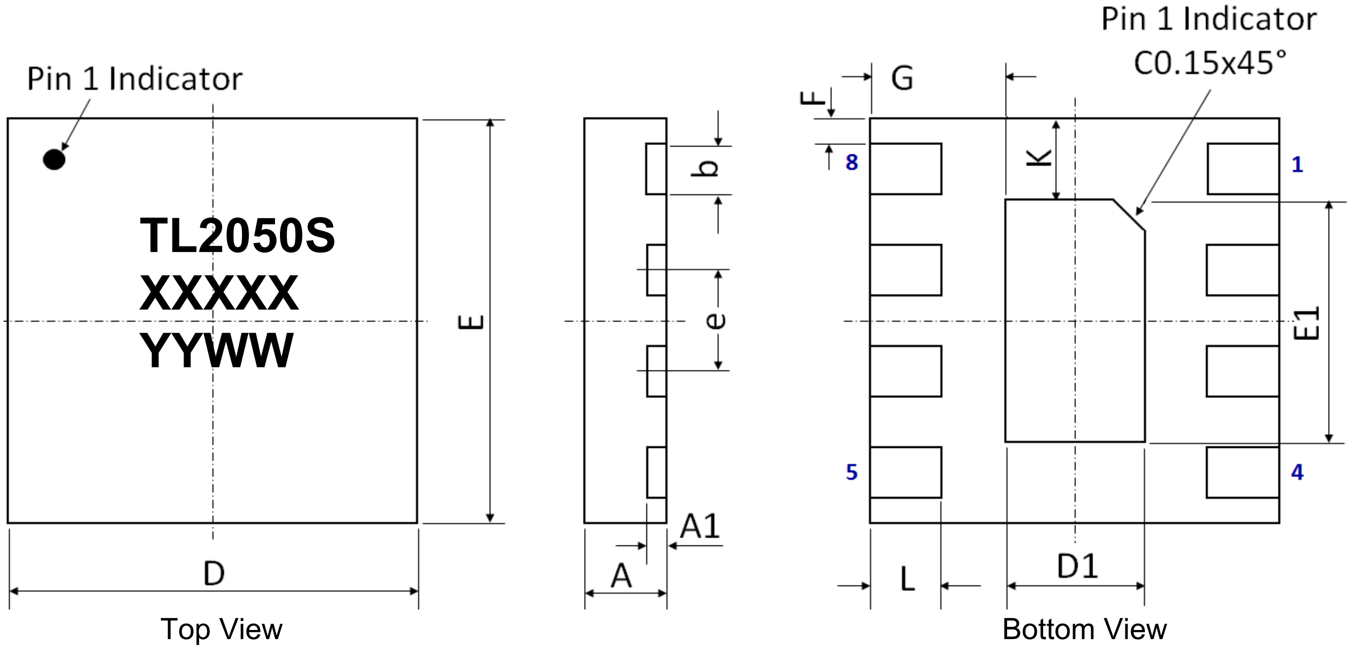
Test set up:

For LNA on mode apply

- Connect ground
- Apply VEN[Venable]=5V
- Apply Vdd =5V
- Apply RF

Figure 12.1 TEST Set Up Diagram

13.0 Device Package Information



XXXXX=Lot Mfg Code
YYWW=Date Code

Figure 13.1 Device Package Drawing
(All dimensions are in mm)
Not to scale.

Table 13.1 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	2.00 BSC	±0.05
A1	0.203	±0.02	E1	1.20	±0.05
b	0.25	±0.02	F	0.125	±0.02
D	2.00 BSC	±0.05	G	0.66	±0.03
D1	0.68	±0.03	L	0.35	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5 µm ~ 20 µm (Typical 10 µm ~ 12 µm)

14.0 PCB Land Design

Guidelines:
[1] 2-layer PCB is recommended
[2] Via diameter is recommended to be 0.3mm to prevent solder wicking inside the vias
[3] Thermal vias shall only be placed on the center pad and should be filled/plugged with solder or copper
[4] The maximum via number for the center pad is 1(X)×2(Y)=2

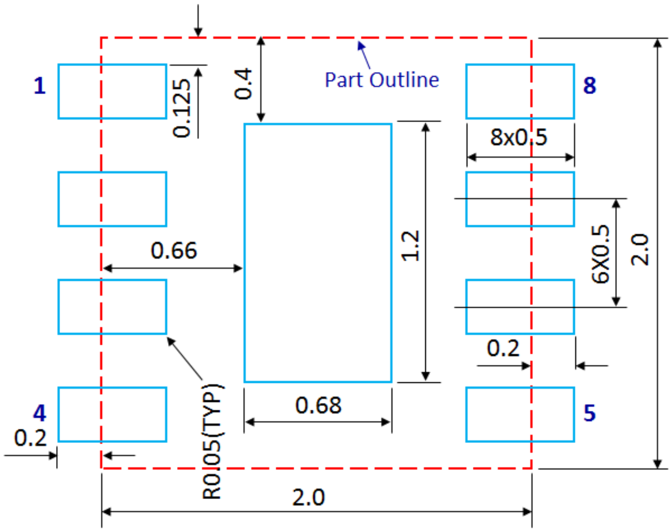


Figure 14.1 PCB Land Pattern
(Dimensions are in mm)

Non-Solder Mask Defined
(Preferred)

Solder Mask Defined

Figure 14.2 Solder Mask Pattern
(Dimensions are in mm)

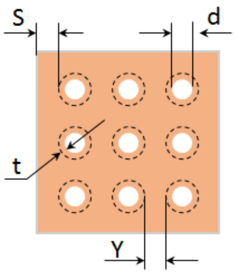


Figure 14.3 Thermal Via Pattern
(Recommended Values: S≥0.15 mm; Y≥0.20 mm; d=0.3 mm; Plating Thickness t = 25 μm or 50 μm)

15.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 μm.

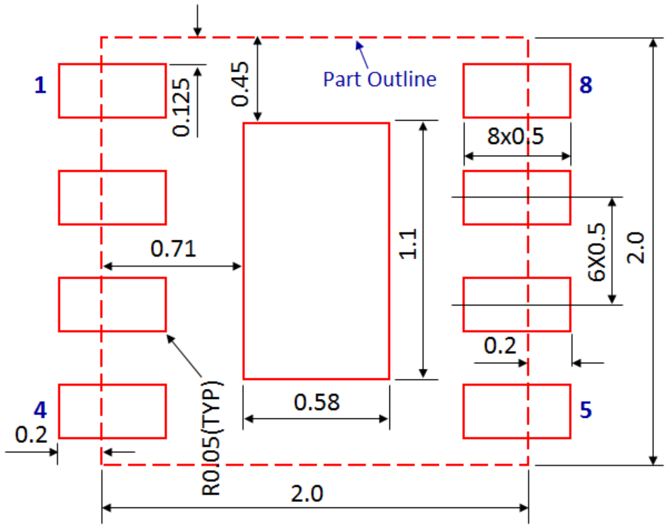


Figure 15.1 Stencil Openings
(Dimensions are in mm)

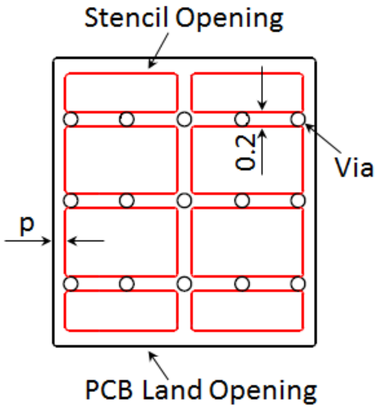


Figure 15.2 Stencil Openings Shall Not Cover Via Areas If Possible
(Dimensions are in mm)

Revision Information

Document	Description	Change/Revision Details / Date
TDLNA2050SEP_Prod_Spec	Initial Release of the Product Specification data sheet	Rev 0.1 / 12_27_2023

Document Category Definitions:

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, Email us at: **hirel@teledyne.com** **website: www.tdehirel.com**

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