TELEDYNE e2V
HIREL ELECTRONICS
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Product Specification

TDGD27x Data Sheet

Isolated Gate Drivers

November 2022

Single/Dual 4-Amp Isolated Gate Driver with High Transient (dV/dt) Immunity

The TDGD27x isolators are ideal for driving power switches used in a wide variety of power supply, inverter, and motor control applications. The TDGD27x isolated gate drivers utilize a proprietary silicon isolation technology, supporting up to 2.5 kV_{RMS} withstand voltage and fast 60 ns propagation times. This technology enables industry leading, common-mode transient immunity (CMTI), tight timing specifications, reduced variation with temperature and age, better part-to-part matching, and extremely high reliability. It also offers unique features such as separate pull-up/down outputs, driver shutdown on UVLO (Undervoltage Lockout) fault, and precise dead-time programmability. The TDGD27x series offers longer service life and dramatically higher reliability compared to opto-coupled gate drivers.

Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. TTL-level compatible inputs with >400 mV hysteresis is available in individual control input (TDGD271) or PWM input (TDGD274) configurations. High integration, low propagation delay, small installed size, flexibility, and cost effectiveness make the TDGD27x family ideal for a wide range of isolated MOSFET/IGBT and SiC or GaN HEMT gate drive applications.

Ideally suited for driving Teledyne HiRel's TDG family of GaN HEMTs.

HiRel Applications

- dc/dc Converter
- Battery Management Systems
- Power Supplies
- Motor Control Systems

KEY FEATURES

- Single, dual, or high-side/low-side drivers
- Single PWM or dual digital inputs
- High dV/dt immunity:
  - 200 kV/µs CMTI
  - 400 kV/µs Latch-up
- Separate pull-up/down outputs for slew rate control
- Wide supply range:
  - Input supply: 2.5–5.5 V
  - Driver supply: 4.2–30 V
- Very low jitter of 200 ps p-p
- 60 ns propagation delay (max)
- Dedicated enable pin
- High performance isolation technology:
  - Industry leading noise immunity
  - High speed, low latency and skew
  - Best reliability available
- Compact packages:
  - 8-pin SOIC
  - 16-pin SOIC
- Wide temperature range:
  - –55 to 125 °C
- One Diffusion Lot
- Teledyne 100% screening
- Obsolescence Support

1. Ordering Guide

Table 1.1. TDGD27x Ordering Guide ***(SEE NOTES)***

Ordering Part Number	Inputs	Driver Configuration[2]	Output UVLO (V)	Integrated Deglitcher	Dead-Time Adjustable Range (ns)	Low Jitter	Package	Isolation Rating
2.5 kV_{RMS} Isolation Options								
TDGD271DEP	VI	Single	3	N	N/A	Y	SOIC-8 NB	2.5 kV_{RMS}
TDGD274DEP	PWM	HS/LS, Dual	3	N	10-200	Y	SOIC-16 NB	2.5 kV_{RMS}

Note:

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. For device availability and package options, please contact the factory.

2. System Overview

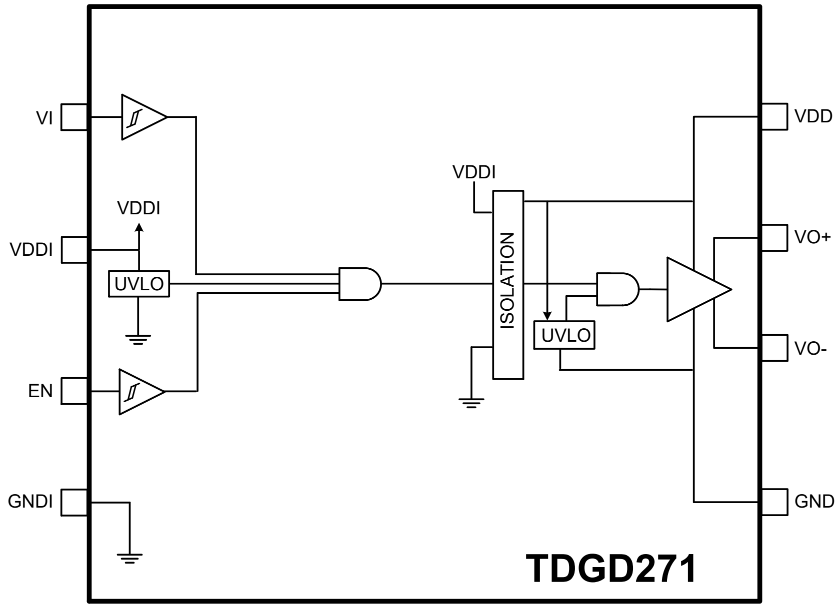


Figure 2.1. TDGD271 Block Diagram

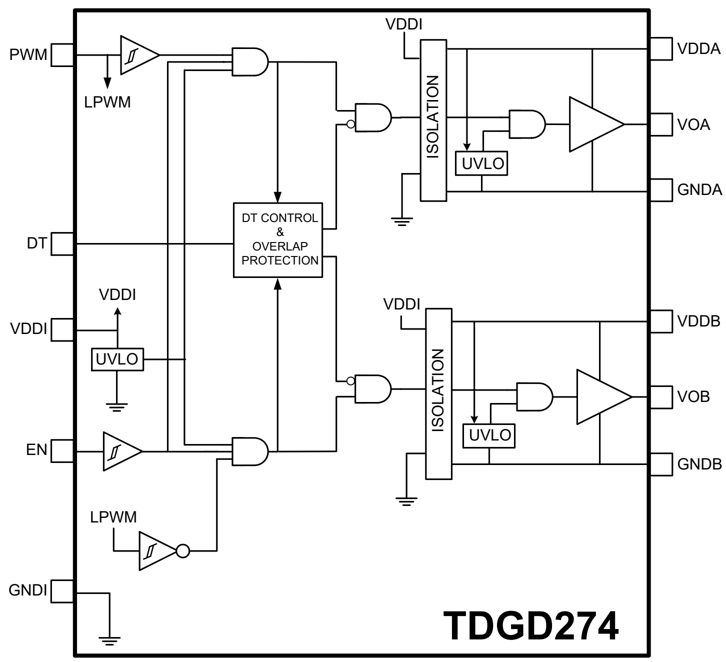


Figure 2.2. TDGD274 Block Diagram

The operation of an TDGD27x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single TDGD27x channel is shown in the figure below.

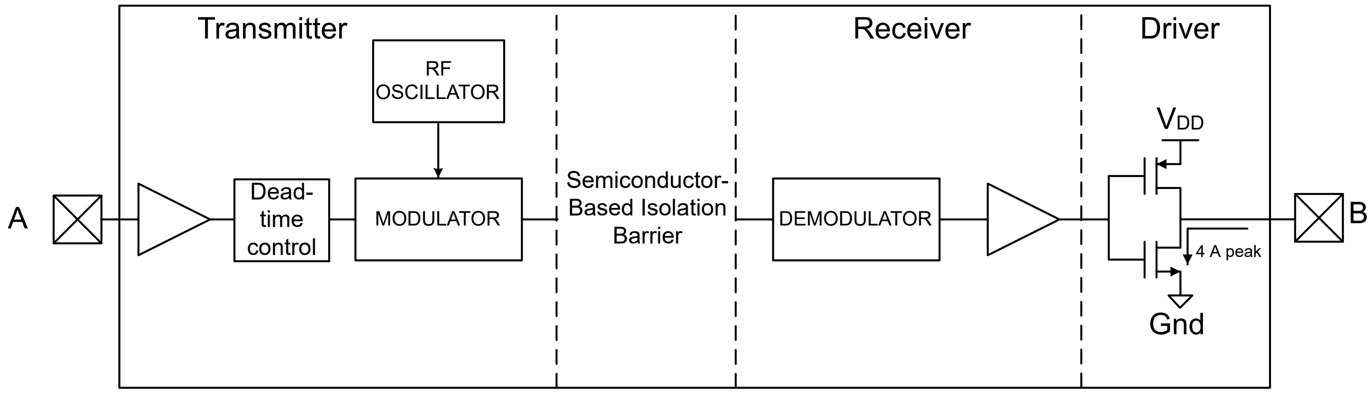


Figure 2.3. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 2.4 Modulation Scheme for more details.

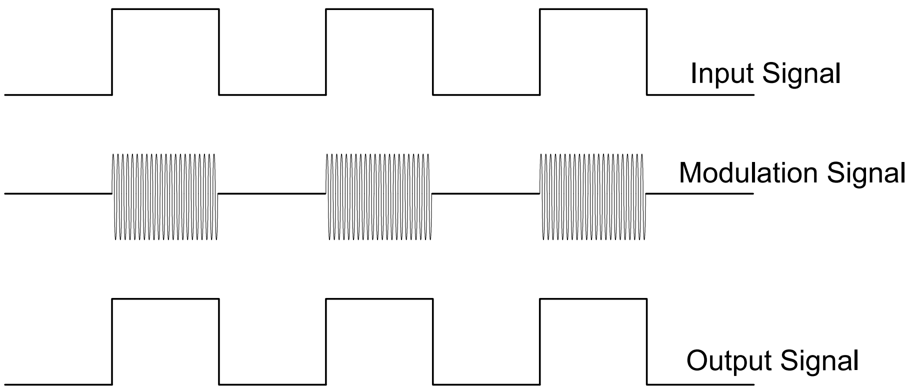


Figure 2.4. Modulation Scheme

2.1 Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to Table 4.1 Electrical Characteristics on page 15 for actual specification limits.

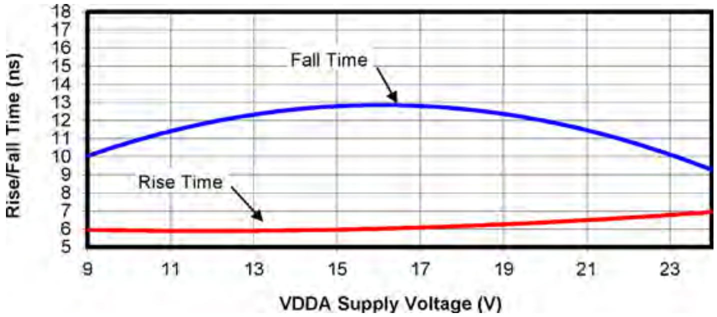


Figure 2.5. Rise/Fall Time vs. Supply Voltage

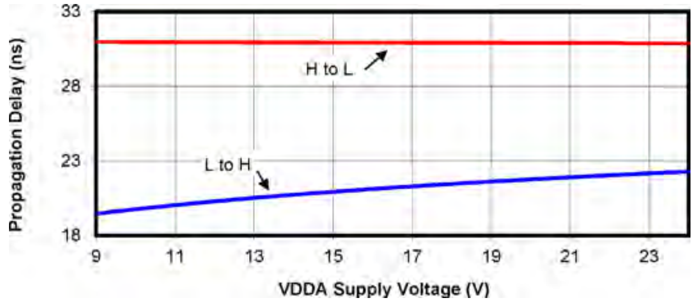


Figure 2.6. Propagation Delay vs. Supply Voltage

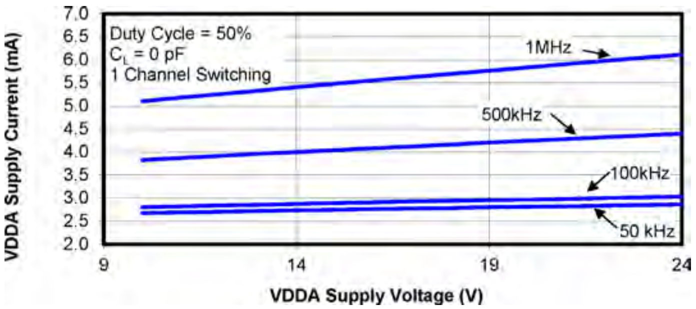


Figure 2.7. Supply Current vs. Supply Voltage

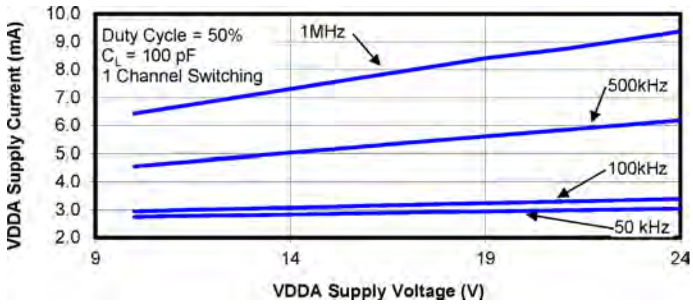


Figure 2.8. Supply Current vs. Supply Voltage

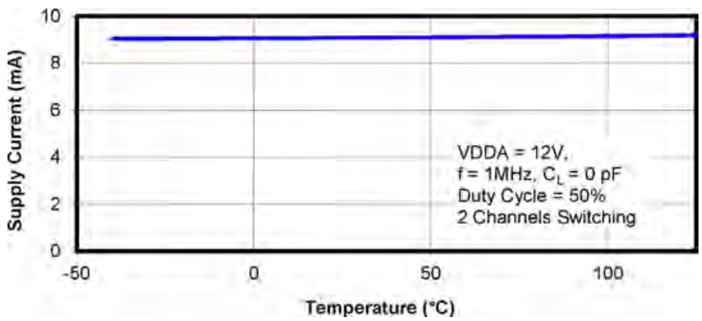


Figure 2.9. Supply Current vs. Temperature

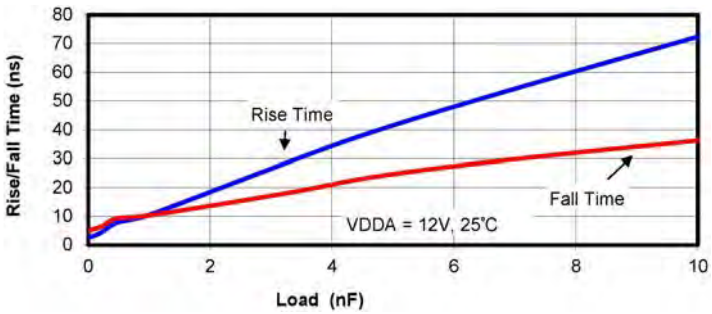


Figure 2.10. Rise/Fall Time vs. Load

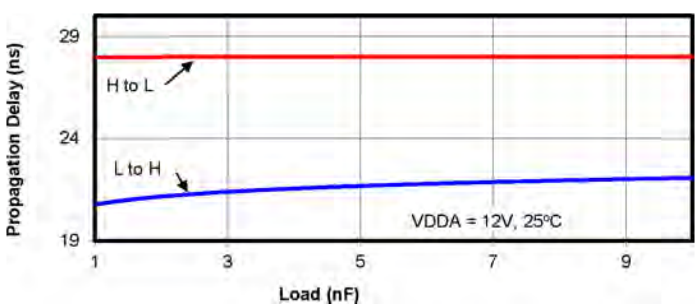


Figure 2.11. Propagation Delay vs. Load

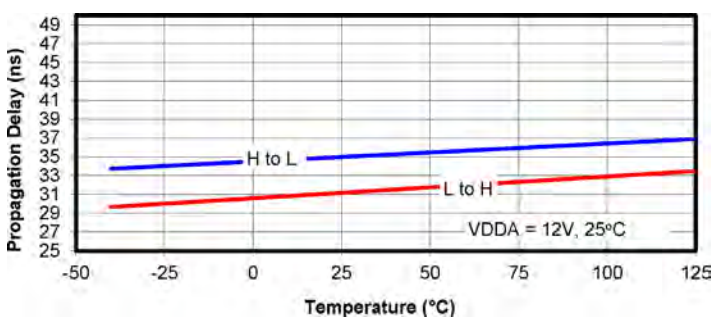


Figure 2.12. Propagation Delay vs. Temperature

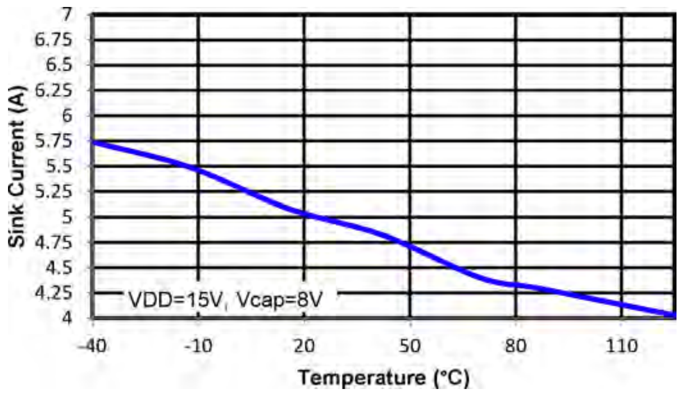


Figure 2.13. Output Sink Current vs. Temperature

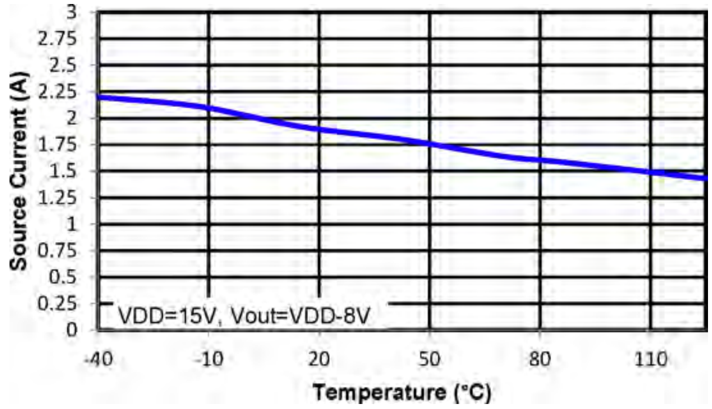


Figure 2.14. Output Source Current vs. Temperature

2.2 Family Overview and Logic Operation During Startup

The TDGD27x family of isolated drivers consists of single, high-side/low-side, and dual driver configurations.

2.2.1 Products

The table below shows the configuration and functional overview for each product in this family.

Table 2.1. TDGD27x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
TDGD271	Single Driver	—	—	VI	4.0
TDGD274	PWM	Y	Y	PWM	4.0

2.2.2 Device Behavior

The following table consists of truth tables for the TDGD27x families. (Continued next page.)

Table 2.2. TDGD27x Family Truth Table[1]

TDGD271 (Single Driver) Truth Table					
Inputs	VDDI State	Enable	Output		Notes
VI			VO+	VO–	
L	Powered	H	Hi–Z	L	
H	Powered	H	H	Hi–Z	
X[2]	Unpowered	X	Hi–Z	L	
X	Powered	L	Hi–Z	L	
TDGD274 (PWM Input High-Side/Low-Side) Truth Table					
PWM Input	**VDDI State**	**Enable**	**Output**		**Notes**
			VOA	**VOB**	
H	Powered	H	H	L	
L	Powered	H	L	H	
X[2]	Unpowered	X	L	L	Output returns to input state within 7 μs of VDDI power restoration.
X	Powered	L	L	L	Device is disabled.

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 2.6.2 Undervoltage Lockout for more information.
2. An input can power the input die through an internal diode, if its source has adequate current.

2.3 Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the TDGD27x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

2.4 Power Dissipation Considerations

Proper system design must assure that the TDGD27x operates within safe thermal limits across the entire load range. The TDGD27x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. The equation below shows total TDGD27x power dissipation.

$$P_D = (\text{VDDI})(\text{IDDI}) + 2(\text{IDDx})(\text{VDDx}) + (f)(Q_G)(\text{VDDx})\left[\frac{R_P}{R_P + R_G}\right] + (f)(Q_G)(\text{VDDx})\left[\frac{R_N}{R_N + R_G}\right] + 2\,f\,C_{INT}\text{VDDx}^2$$

where:

P_D is the total TDGD27x device power dissipation (W)

IDDI is the input-side maximum bias current (10 mA)

IDDx is the driver die maximum bias current (4 mA)

C_{INT} is the internal parasitic capacitance (370 pF)

VDDI is the input-side VDD supply voltage (2.5 to 5.5 V)

VDDx is the driver-side supply voltage (4.2 to 30 V)

f is the switching frequency (Hz)

Q_G is the gate charge of the external FET

R_G is the external gate resistor

R_P is the $R_{DS(ON)}$ of the driver pull-up switch (2.7 Ω)

R_N is the $R_{DS(ON)}$ of the driver pull-down switch (1 Ω)

Equation 1

For example, the total power dissipation for an application can be found using Equation 1 and the following application-specific values:

VDDI = 5.0 V

VDDx = 12 V

f = 350 kHz

R_G = 22 Ω

Q_G = 25 nC

With these application-specific values, Equation 1 yields P_D = 199 mW .

The driver junction temperature is calculated using Equation 2, shown below.

$$T_J = P_D \times \theta_{JA} + T_A$$

where:

P_D is the total TDGD27x device power dissipation (W), as determined by

Equation 1. θ_{JA} is the thermal resistance from junction to air (°C/W)

T_A is the ambient temperature (°C)

Equation 2

Continuing the example above, the driver junction temperature can be determined using the result of Equation 1 and Equation 2 with the following application-specific values:

θ_{JA} = 66 ˚C/W

T_A = 20 ˚C

With these application-specific values, Equation 2 yields T_J = 33.1 ˚C.

The maximum power dissipation allowable for the TDGD27x, for any given application, is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 3 below.

$$P_{D(MAX)} \leq \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where:

$P_{D(MAX)}$ is the maximum TDGD27x power dissipation (W)

$T_{J(MAX)}$ is the maximum TDGD27x junction temperature (150

°C) T_A is the ambient temperature (°C)

θ_{JA} is the TDGD27x junction-to-air thermal resistance (°C/W)

Equation 3

Continuing our example from the previous page and using the results of Equation 1 and Equation 2 as inputs to Equation 3, along with the example values of T_A and θ_{JA} previously given, yields a maximum allowable power dissipation of 1.97 W.

Maximum allowable gate charge as a function of switching frequency is found by substituting the maximum allowable power dissipation limit and the appropriate data sheet values from Table 4.1 Electrical Characteristics on page 15 into Equation 1 and simplifying. For our example, the result is Equation 4, which assumes VDDI = 5 V and VDDA = VDDB = 12 V, and can be easily charted to visualize design constraints as is demonstrated by Figure 2.15 below.

$$Q_{G(MAX)} = \frac{0.995}{f} - 1.06 \times 10^{-7}$$

Equation 4

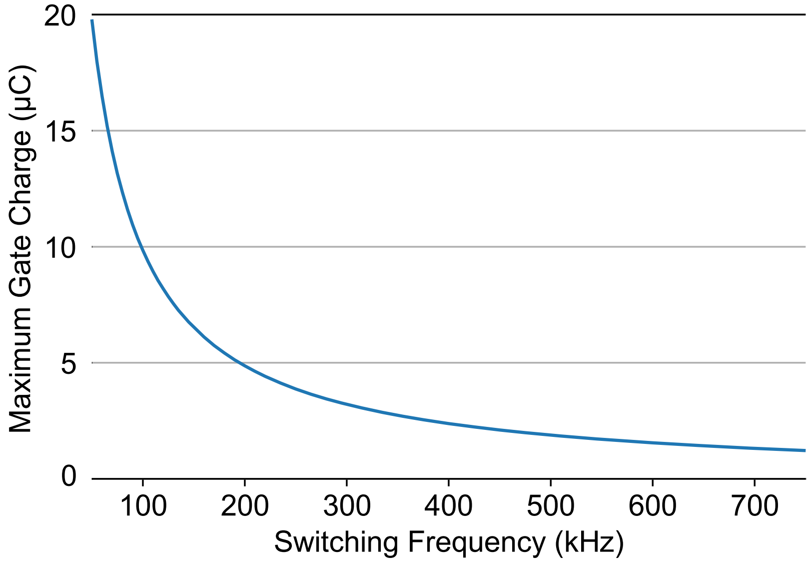


Figure 2.15. Maximum Gate Charge vs. Switching Frequency

2.5 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the TDGD27x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the TDGD27x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

2.6 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in the Figure 2.16 on page 11, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively.

It's important to note that the driver outputs (VO) will default to a low output state when the input side power supply (VDDI) is not present, but the output side power supply (VDDx) is present.

2.6.1 Device Startup

Driver outputs (VO) are held low during power-up until the device power supplies are above the UVLO threshold for time period t_{START}.

Following this, the outputs follow the state of device inputs (VI).

2.6.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when the device power supplies are below their specified operating circuits range. The input (control) side, and each driver on the output side, have their own undervoltage lockout monitors.

The TDGD27x input side enters UVLO when VDDI < $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver output (VO) remains low when the input side of the TDGD27x is in UVLO and VDDx is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

The UVLO circuit unconditionally drives VO low when VDDx is below the lockout threshold. Upon power up, the TDGD27x is maintained in UVLO until VDDx rises above $VDDx_{UV+}$. During power down, the TDGD27x enters UVLO when VDDx falls below $VDDx_{UV-}$. Please refer to spec tables for UVLO values.

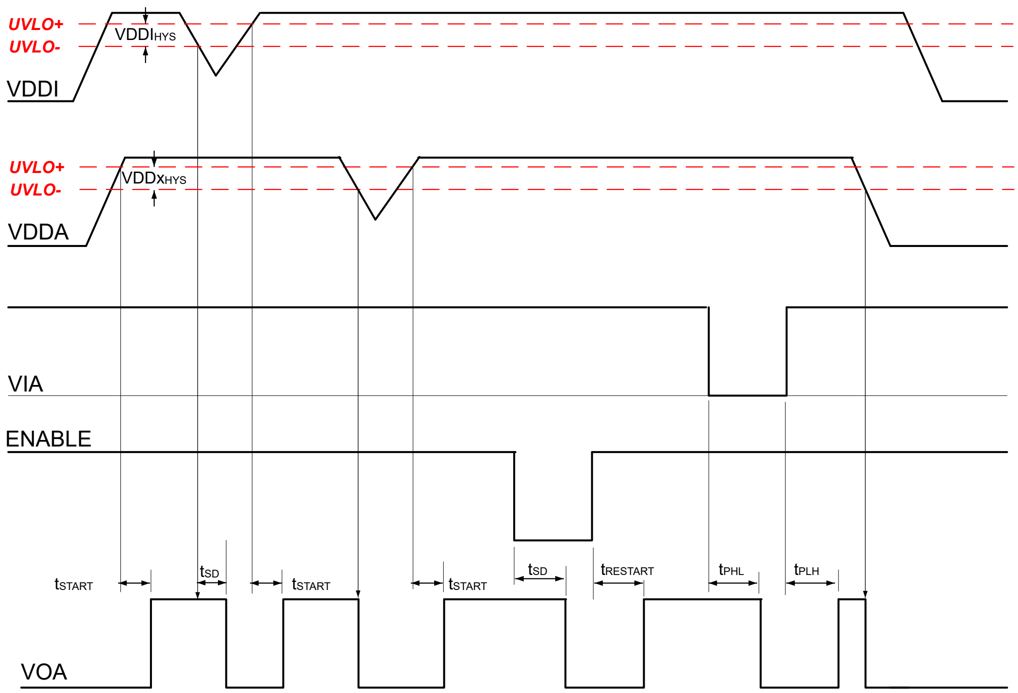


Figure 2.16. Device Behavior during Normal Operation and Shutdown

2.6.3 Control Inputs

PWM input is a high-true, TTL level-compatible logic input. For PWM input versions (TDGD274), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.6.4 Enable Input

When brought low, the ENABLE input unconditionally drives VOA and VOB low. Device operation terminates within t_{SD} after ENABLE = V_{IL} and resumes within $t_{RESTART}$ after ENABLE = V_{IH}. The ENABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

2.7 Overlap Protection and Programmable Dead Time

Overlap protection prevents the two driver outputs from both going high at the same time. Programmable dead time control sets the amount of time between one output going low and the other output going high.

Drivers controlled with a single input (TDGD274x) have inherit overlap protection by virtue of one driver being active high and the other being active low with respect to the PWM input.

All high-side/low-side drivers with a single PWM input (TDGD274x) include programmable dead time, which adds a user- programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per the equation below. Note that the dead time pin should be connected to GNDI through a resistor between the values of 6 kΩ and 100 kΩ. A filter capacitor of 100 pF in parallel with RDT is recommended. See Figure 2.17.

$$DT = 2.02 \times RDT + 7.77 \text{ (for 10-200 ns range)}$$

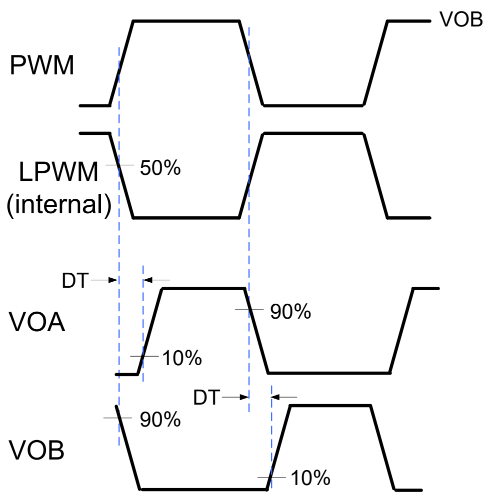
$$DT = 6.06 \times RDT + 3.84 \text{ (for 20-700 ns range)}$$

where:

DT is the dead time (ns)

RDT is the dead time programming resistor (kΩ)

Equation 4



Typical Dead Time Operation

Figure 2.17. Dead-Time Waveforms for TDGD8274x Drivers

2.8 Deglitch Feature

A deglitch feature is provided on some options, as defined in the 1. Ordering Guide. The internal deglitch circuit provides an internal time delay of 15 ns typical, during which any noise is ignored and will not pass through the IC. For these product options, the propagation delay will be extended by 15 ns, as specified in the spec table.

3. Applications

The following examples illustrate typical circuit configurations using the TDGD274.

3.1 High-Side/Low-Side Driver

In the figure below shows the TDGD274 controlled by a single PWM signal.

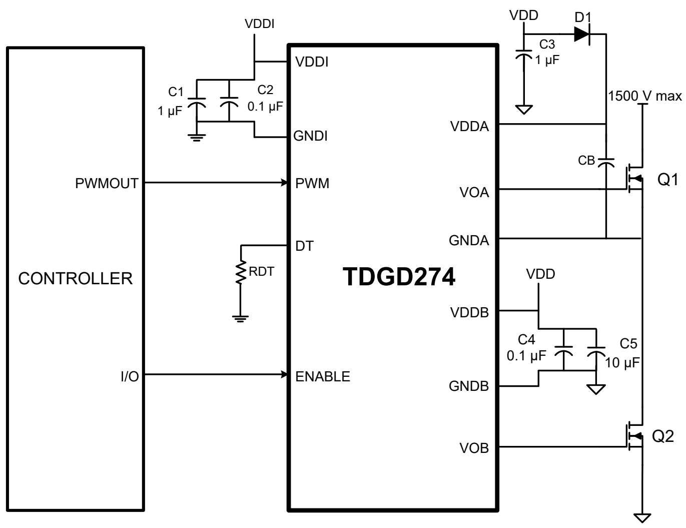


Figure 3.1. TDGD274 in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the TDGD274 requires VDDI in the range of 2.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 4.2 and 30 V with respect to their respective grounds. The boot-strap start up time will depend on the CB capacitor chosen. VDD is usually the same as VDDB. Also, note that the bypass capacitors on the TDGD274 should be located as close to the chip as possible. Moreover, it is recommended that bypass capacitors be used (as shown in the figures above for input and driver side) to reduce high frequency noise and maximize performance. The outputs VOA and VOB can be used interchangeably as high side or low side drivers.

4. Electrical Specifications

Table 4.1. Electrical Characteristics

VDDI = 2.5 to 5.5 V; VDDx - GNDx = 4.2 to 30 V; T_A = -40 to +125 ˚C

Typical specifications at VDDI = 5 V; VDDx - GNDx = 15 V; T_A = 25 ˚C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDI	VDDI – GNDI	2.5	—	5.5	V
Driver Supply Voltage	VDDx[1]	VDDx – GNDx	4.2	—	30	V
Input Supply Quiescent Current	IDD_Q		—	7.9	10.0	mA
Input Supply Active Current	IDDI	f = 500 kHz	—	8.0	10.0	mA
Output Supply Quiescent Current	$IDDx_Q$[2]		—	2.5	4.0	mA
Output Supply Active Current	IDDx[2]	f = 500 kHz (no load)	—	10.0	11.0	mA
Gate Driver						
High Output Transistor RDS (ON)	R_{OH}		—	2.7	—	Ω
Low Output Transistor RDS (ON)	R_{OL}		—	1.0	—	Ω
High Level Peak Output Current	I_{OH}	VDDx = 15 V, See Figure 4.2 on page 17 for TDGD27x, VDDx = 4.2 V, t_{PW_IOH} < 250 ns	—	1.8	—	A
Low Level Peak Output Current	I_{OL}	VDDx = 15 V, See Figure 4.1 on page 17 for TDGD27x, VDDx = 4.2 V, t_{PW_IOL} < 250 ns	—	4.0	—	A
UVLO						
VDDI UVLO Threshold +	$VDDI_{UV+}$		1.85	2.2	2.45	V
VDDI UVLO Threshold –	$VDDI_{UV-}$		1.75	2.1	2.35	V
VDDI Hysteresis	$VDDI_{HYS}$		—	100	—	mV
UVLO Threshold + (Driver Side)						
3 V Threshold	$VDDx_{UV+}$[1]		2.7	3.5	4.0	V
5 V Threshold			4.9	5.5	6.3	V
8 V Threshold			7.2	8.3	9.5	V
12 V Threshold			11	12.2	13.5	V
UVLO Threshold - (Driver Side)						

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
3 V Threshold	$VDDx_{UV-}$[1]		2.5	3.0	3.8	V
5 V Threshold			4.6	5.2	5.9	V
8 V Threshold			6.7	7.8	8.9	V
12 V Threshold			9.6	10.8	12.1	V
UVLO Lockout Hysteresis						
3 V Threshold	$VDDx_{HYS}$		—	500	—	mV
5 V Threshold			—	300	—	mV
8 V Threshold			—	500	—	mV
12 V Threshold			—	1400	—	mV
Digital						
Logic High Input Threshold	V_{IH}		—	—	2.0	V
Logic Low Input Threshold	V_{IL}		0.8	—	—	V
Input Hysteresis	V_{HYST}		350	400	—	mV
Logic High Output Voltage	V_{OH}	$I_O = -1$ mA	VDDx – 0.04	—	—	V
Logic Low Output Voltage	V_{OL}	$I_O = 1$ mA	—	—	0.04	V
AC Switching Parameters						
Propagation Delay TDGD271 with low jitter	t_{PLH}, t_{PHL}	$C_L = 200$ pF	20	30	60	ns
Propagation Delay TDGD271 with deglitch	t_{PLH}, t_{PHL}	$C_L = 200$ pF	30	45	75	ns
Propagation Delay TDGD274 with low jitter	t_{PHL}	$C_L = 200$ pF	20	30	60	ns
Propagation Delay TDGD274 with deglitch	t_{PHL}	$C_L = 200$ pF	30	45	75	ns
Propagation Delay TDGD274 with low jitter	t_{PLH}	$C_L = 200$ pF	30	45	75	ns
Propagation Delay TDGD274 with deglitch	t_{PLH}	$C_L = 200$ pF	65	85	105	ns
Pulse Width Distortion TDGD271 all options	PWD	$\|t_{PLH} - t_{PHL}\|$	—	3.6	8	ns
Pulse Width Distortion TDGD274 with low jitter	PWD	$\|t_{PLH} - t_{PHL}\|$	0	14	19	ns
Pulse Width Distortion TDGD274 with deglitch option	PWD	$\|t_{PLH} - t_{PHL}\|$	—	38	47	ns
Peak to Peak Jitter TDGD27x with low jitter	$t_{JIT(PK)}$		100	200	550	ps

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmed dead time (DT) for products with 10–200 ns DT range	DT	RDT = 6 kΩ	10	20	30	ns
		RDT = 15 kΩ	26	38	50	
		RDT = 100 kΩ	150	210	260	
Programmed dead time (DT) for products with 20–700 ns DT range	DT	RDT = 6 kΩ	23	40	57	ns
		RDT = 15 kΩ	60	95	130	
		RDT = 100 kΩ	450	610	770	
Rise time	t_R	CL = 200 pF	4	10.5	16	ns
Fall time	t_F	CL = 200 pF	5.5	13.3	18	ns
Shutdown Time from Enable False	t_{SD}		—	—	60	ns
Restart Time from Enable True	$t_{RESTART}$		—	—	60	ns
Device Startup Time	t_{START}		—	16	30	μs
Common Mode Transient Immunity TDGD27x with deglitch option	CMTI	See Figure 4.3 on page 18. VCM = 1500 V	200	350	400	kV/μs
Common Mode Transient Immunity TDGD27x with low jitter option	CMTI	See Figure 4.3 on page 18. VCM = 1500 V	150	300	400	kV/μs

Notes:

1. The symbols VDD, VDDA and VDDB all refer to the driver supply voltage, but reflect the different pin names used for the supply on different product options. Specifications that apply to the driver supply voltage are also referred to as VDDx in this data sheet.
2. The symbols IDD, IDDA and IDDB all refer to the driver supply current, but reflect the different pin names used for the supply on different product options. Specifications that apply to the driver supply current are also referred to as IDDx in this data sheet.

4.1 Test Circuits

The figures below depict sink current, source current, and common-mode transient immunity test circuits.

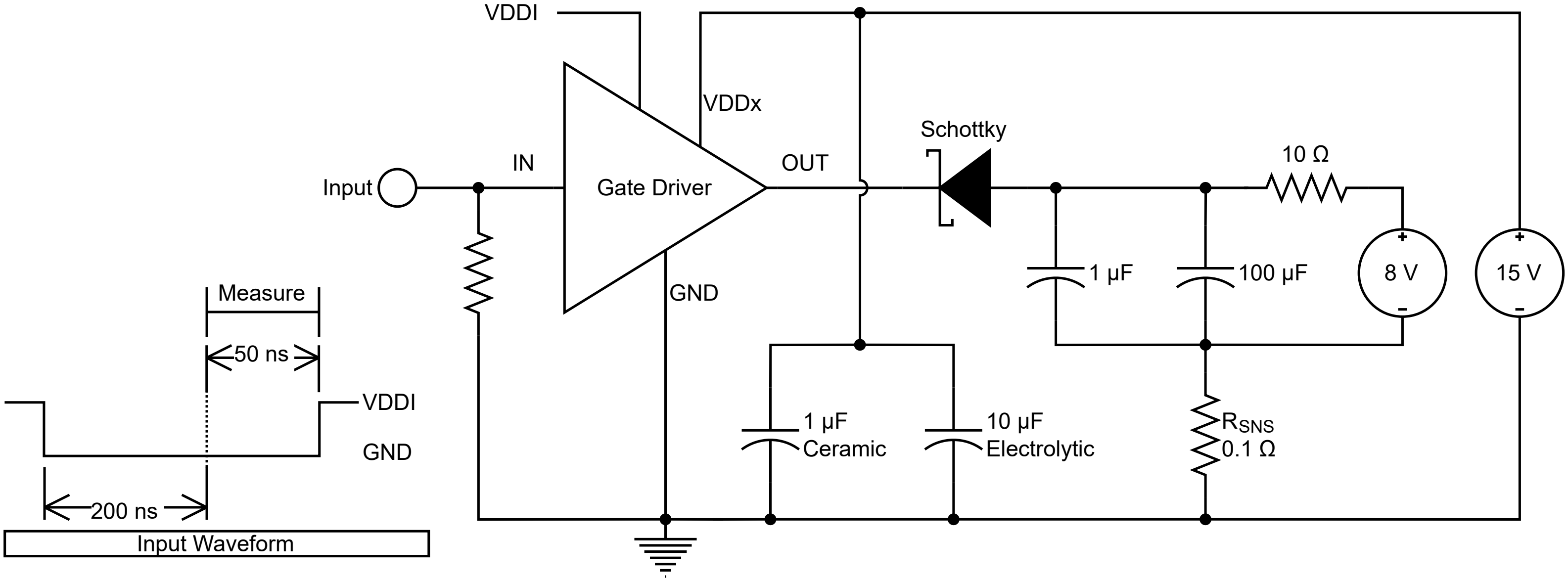


Figure 4.1. IOL Sink Current Test Circuit

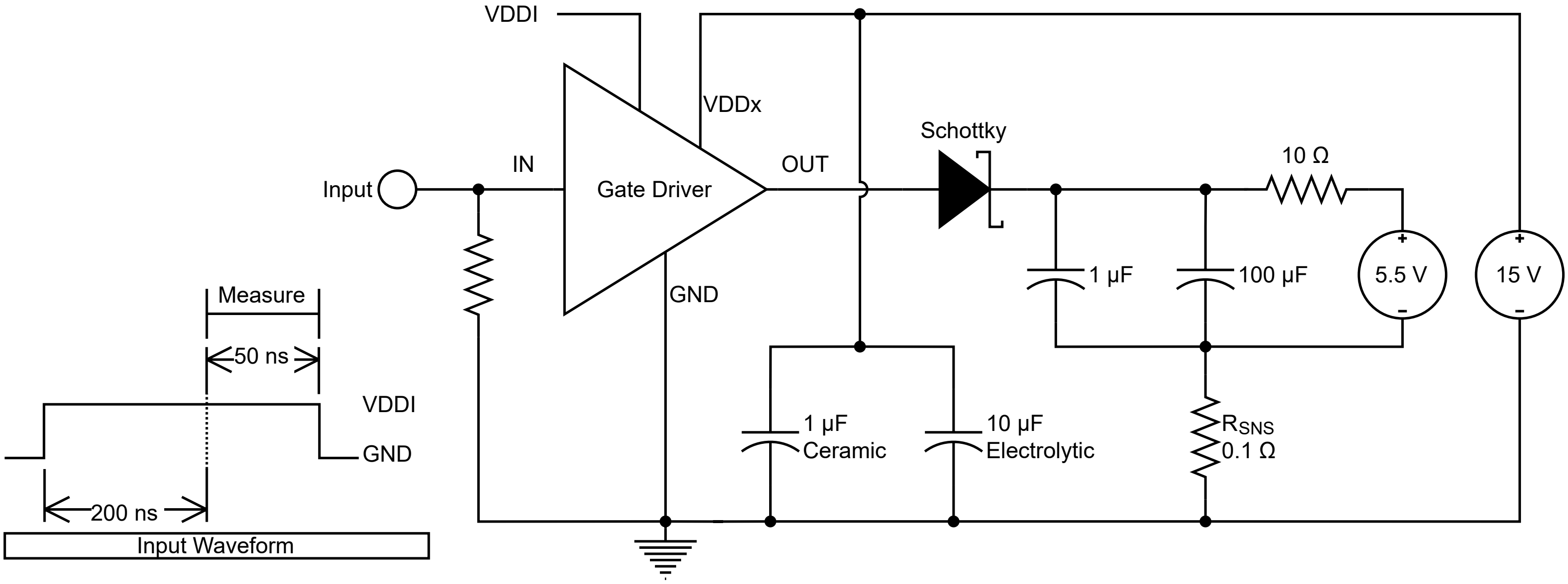


Figure 4.2. IOH Source Current Test Circuit

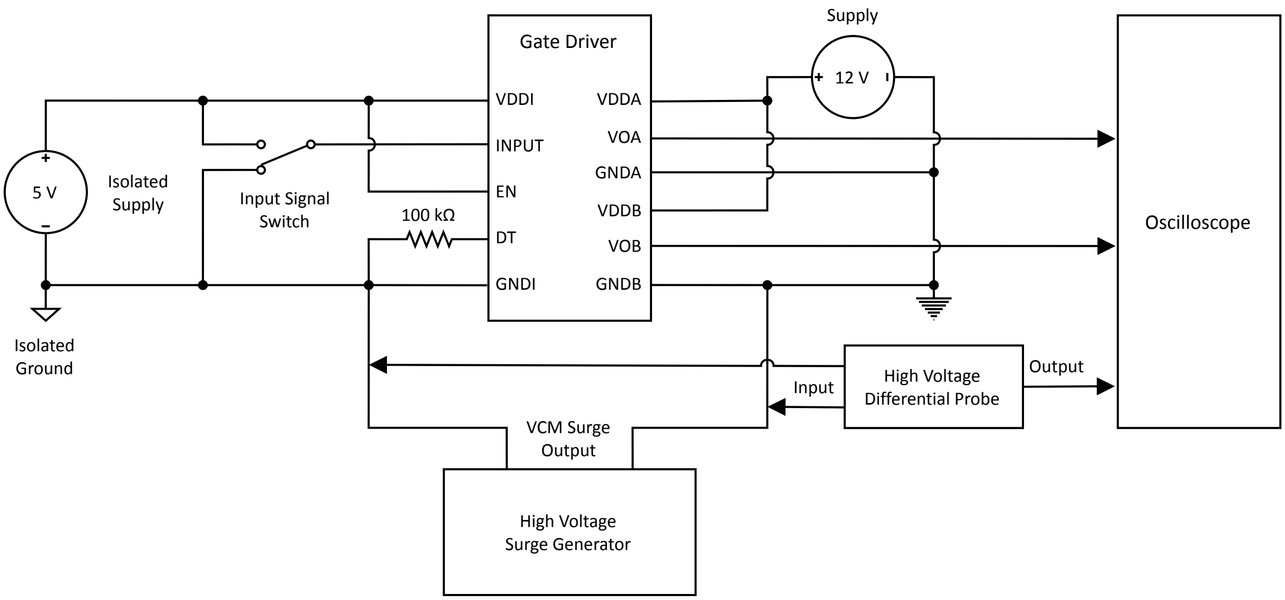


Figure 4.3. Common Mode Transient Immunity Test Circuit

4.2 Regulatory Information (Pending)

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol		Value		Unit
Nominal External Air Gap (Clearance)	CLR		4.7	4.7	mm
Nominal External Tracking (Creepage)	CPG		3.9	3.9	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.008	0.008	mm
Tracking Resistance	PTI or CTI	IEC60112	600	600	Ω
Erosion Depth	ED		0.019	0.019	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	0.5	0.5	pF
Input Capacitance[2]	C_I		3.0	3.0	pF

Notes:
1. To determine resistance and capacitance, the TDGD27x is converted into a 2-terminal device. All pins on side 1 are shorted to create terminal 1, and all pins on side 2 are shorted to create terminal 2. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification	
		SOIC-8	NB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-III	I-III
	Rated Mains Voltages < 400 V_{RMS}	I-II	I-II
	Rated Mains Voltages < 600 V_{RMS}	I-II	I-II

Table 4.5. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	SOIC-8	NB SOIC-16	Unit
Safety Temperature	T_S		150	150	°C
Safety Input Current	I_S	θ_{JA} = 115 °C/W (SOIC-8), 66 °C/W (NB SOIC-16), VDDI = 5.5 V, VDDx = 30 V, T_J = 150 °C, T_A = 25 °C	36	63	mA
Device Power Dissipation	P_D		1.1	1.2	W

Note:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in the two figures below.

Table 4.6. Thermal Characteristics

Parameter	Symbol	SOIC-8	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	115	66	°C/W

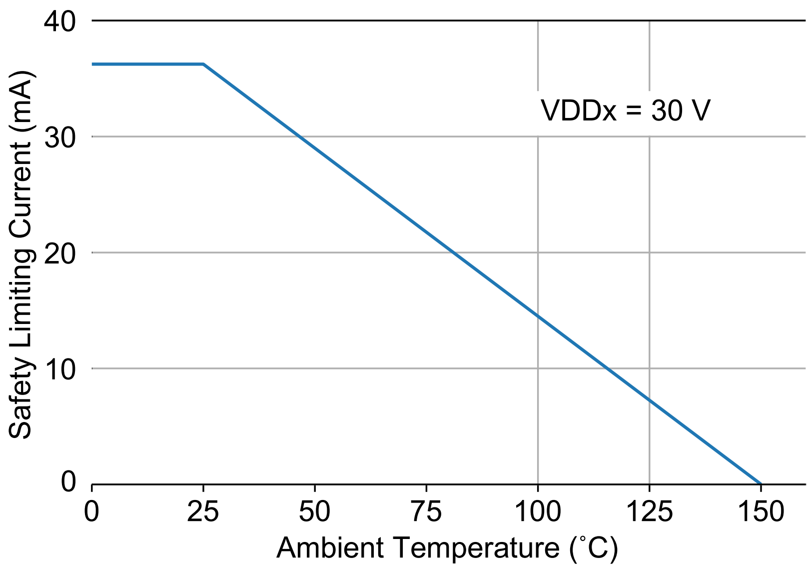


Figure 4.4. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values per VDE

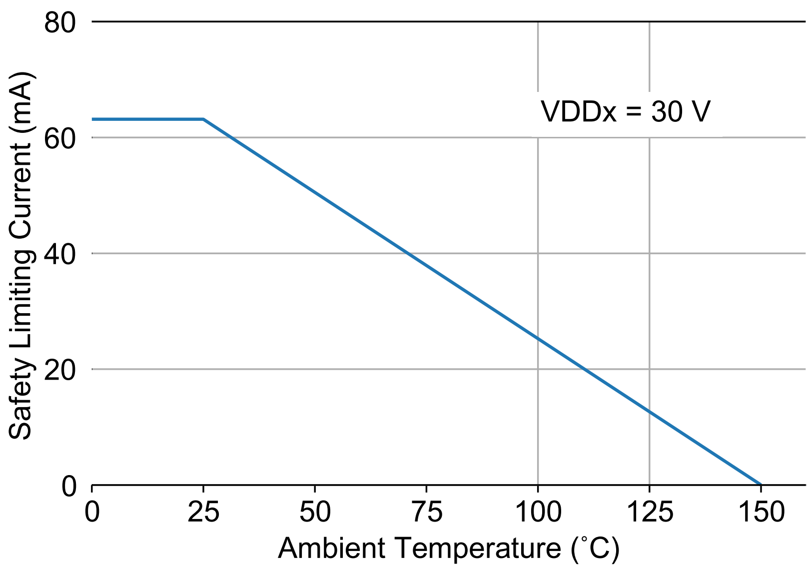


Figure 4.5. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values per VDE

Table 4.7. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+150	°C
Input-side supply voltage	VDDI	–0.6	6.0	V
Driver-side supply voltage	VDD, VDDA, VDDB	–0.6	36	V
Voltage on any input pin with respect to ground	VI, EN, DT	–0.5	VDD + 0.5	V
Voltage on any input pin with respect to ground[2]	VO+, VO-, VOA, VOB	–0.5	VDD + 0.5	V
	VO+, VO-, VOA, VOB Transient for 200 ns	–1.2		
Peak Output Current (t_{PW} = 10 μs, duty cycle = 0.2%)	I_{OPK}	—	4.0	A
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		—	3.5	kV
CDM		—	2000	V
Maximum Isolation Voltage (Input to Output) (1 sec) NB SOIC-16 and SOIC-8		—	3000	V_{RMS}
Maximum Isolation Voltage (Output to Output) (1 sec) NB SOIC-16		—	1500	V_{RMS}
Latch-up Immunity		—	400	kV/μs

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.
2. Transient voltage pulse repeatable at 200 kHz.

5. Pin Descriptions

5.1 TDGD271 Pin Descriptions

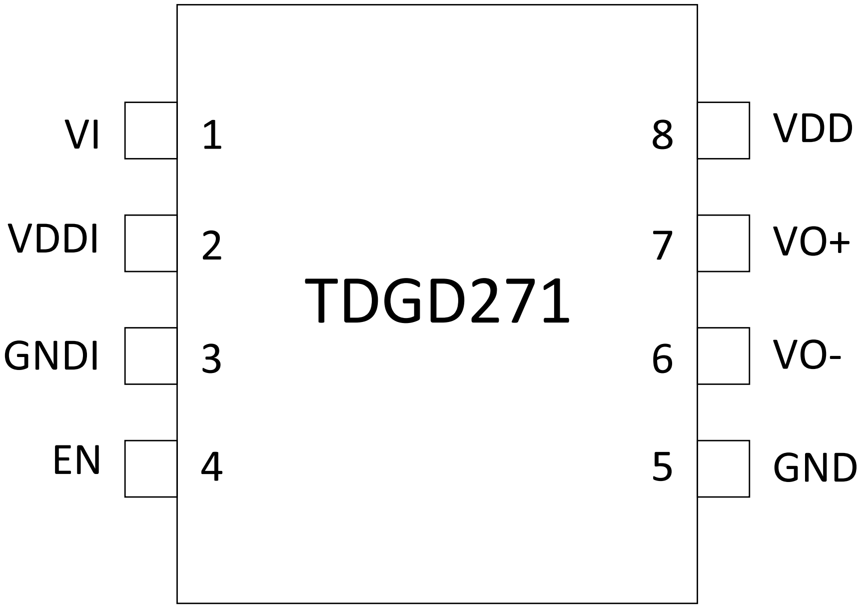


Figure 5.1. Pin Assignments

Table 4.8. TDGD271 Pin Descriptions

Pin	Name	Description
1	VI	Digital driver control signal
2	VDDI	Input side power supply
3	GNDI	Input side ground
4	EN	Enable
5	GND	Driver side ground
6	VO–	Gate drive pull low
7	VO+	Gate drive pull high
8	VDD	Driver side power supply

5.2 TDGD274 Pin Descriptions

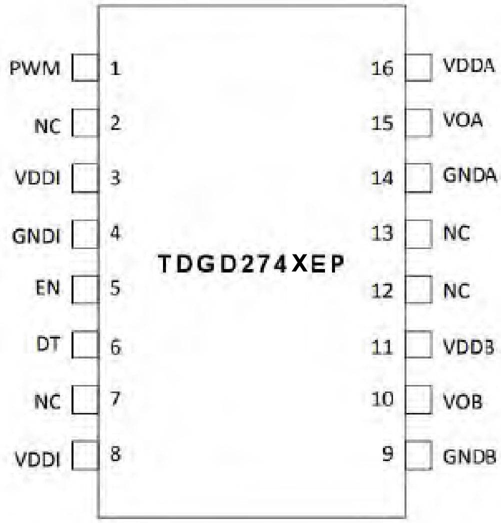


Figure 5.2. TDGD274 Pin Assignments

Table 4.9. TDGD274 Pin Descriptions

NB SOIC-16 Pin #	Name	Description
1	PWM	Pulse width modulated driver control signal
2, 7, 12, 13	NC	No Connect
3, 8	VDDI	Input side power supply
4	GNDI	Input side ground
5	EN	Enable
6	DT	Dead-time control
9	GNDB	Driver side power supply for “B” driver
10	VOB	Gate drive output for “B” driver
11	VDDB	Driver side power supply for “B” driver
14	GNDA	Driver side power supply for “A” driver
15	VOA	Gate drive output for “A” driver
16	VDDA	Driver side power supply for “A” driver

6. Package Outlines

6.1 Package Outline: 16-Pin Narrow-Body SOIC

The figure below illustrates the package details for the TDGD274 in a 16-pin narrow-body SOIC (SO-16). The table below lists the values for the dimensions shown in the illustration.

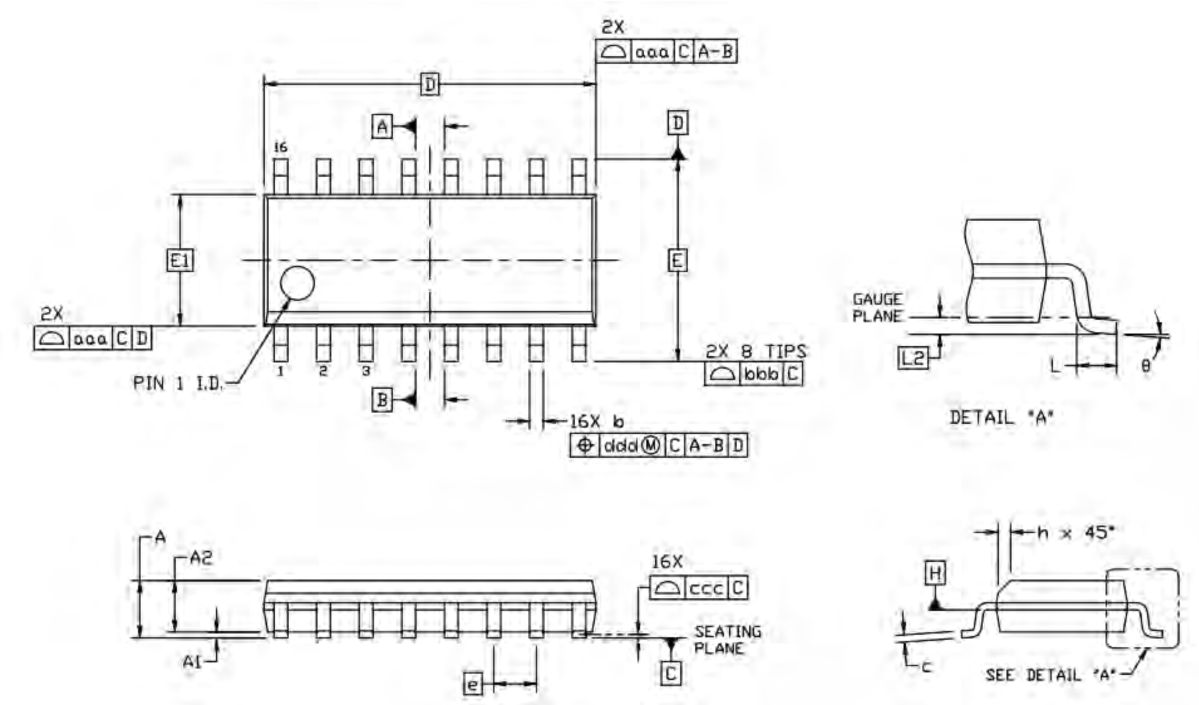


Figure 6.1. 16-pin Small Outline Integrated Circuit (SOIC)

Package **Table 5.0. Package Diagram Dimensions**

Dimension	Min	Max	Dimension	Min	Max
A	—	1.75	L	0.40	1.27
A1	0.10	0.25	L2	0.25 BSC	
A2	1.25	—	h	0.25	0.50
b	0.31	0.51	θ	0°	8°
c	0.17	0.25	aaa	0.10	
D	9.90 BSC		bbb	0.20	
E	6.00 BSC		ccc	0.10	
E1	3.90 BSC		ddd	0.25	
e	1.27 BSC				

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the TDGD271 in an 8-pin narrow-body SOIC package. The table below lists the values for the dimensions shown in the illustration.

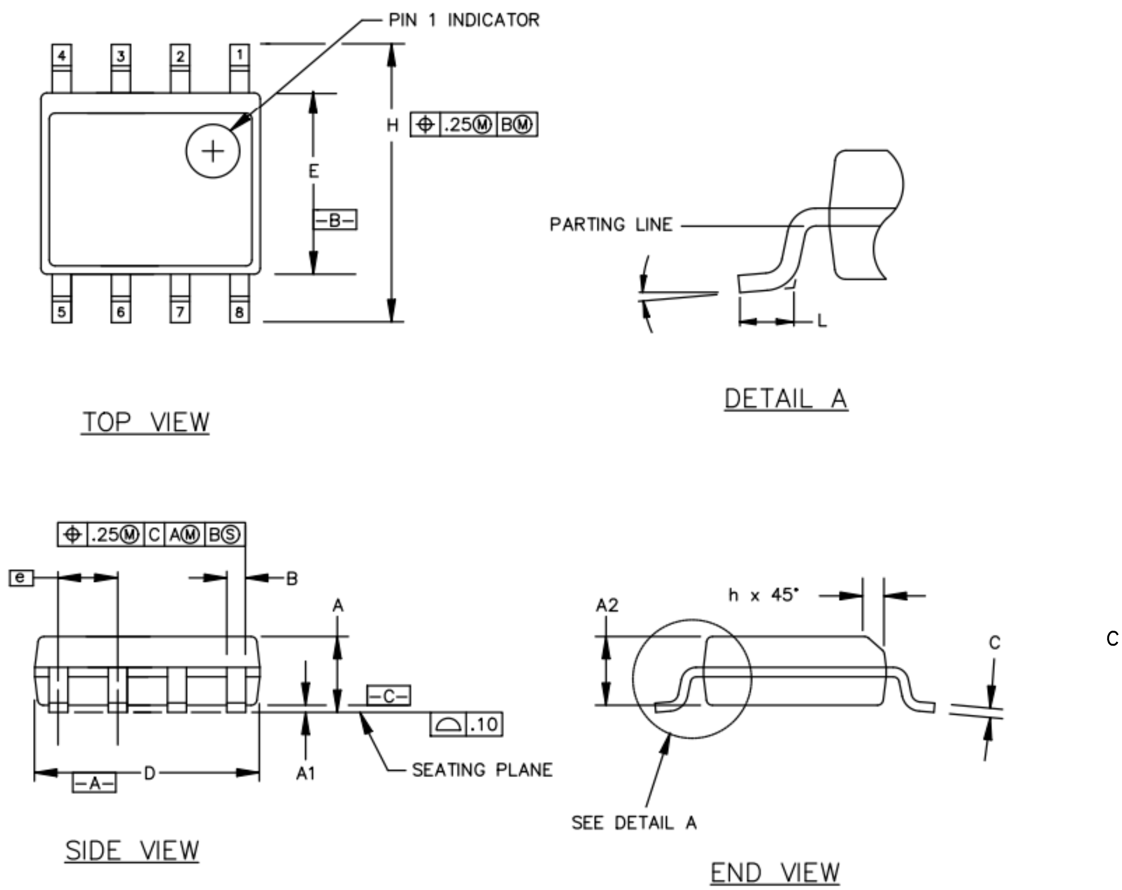


Figure 6.2. 8-Pin Narrow Body SOIC Package

Table 5.1. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

7. Land Patterns

7.1 Land Pattern: 16-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the TDGD274 in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

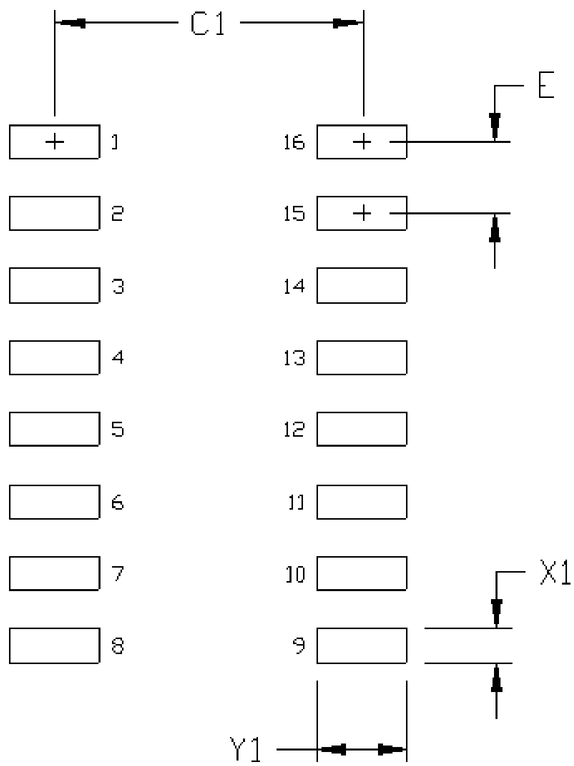


Figure 7.1. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 5.3. 16-Pin Narrow Body SOIC Land Pattern

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

7.2 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the TDGD271 in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

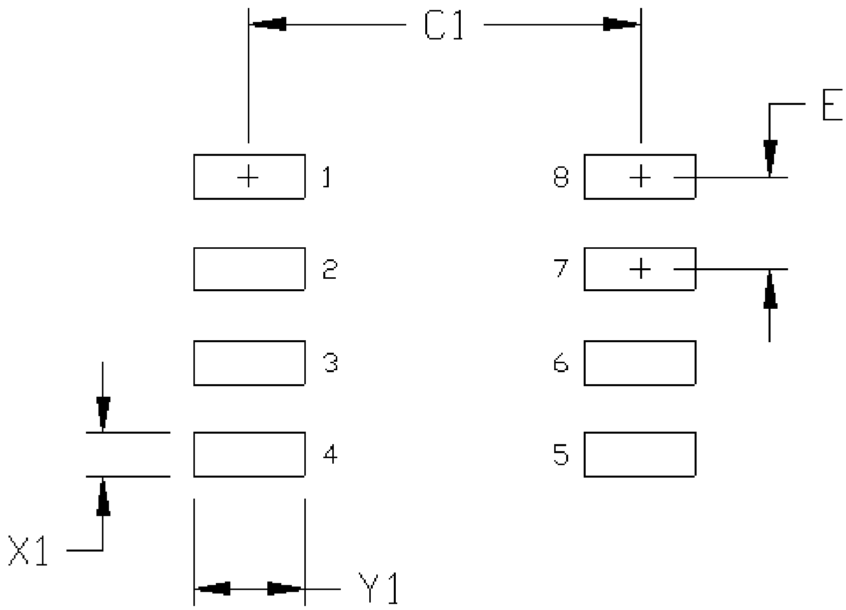


Figure 7.2. 8-Pin Narrow Body SOIC Land Pattern

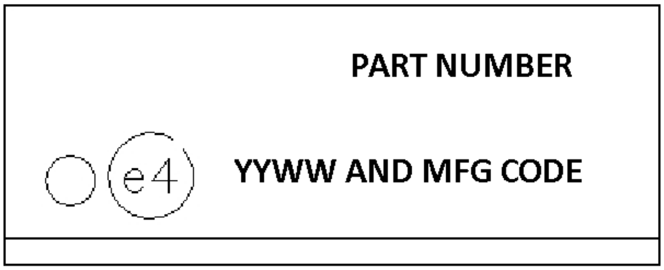
Table 5.4. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Markings

8.1 TDGD274 Top Marking (16-Pin Narrow Body SOIC)



Part Number:
TDGD274DEP

Date Code:
YYWW

8.2 TDGD271 Top Marking (8-Pin Narrow Body SOIC)