

## Features

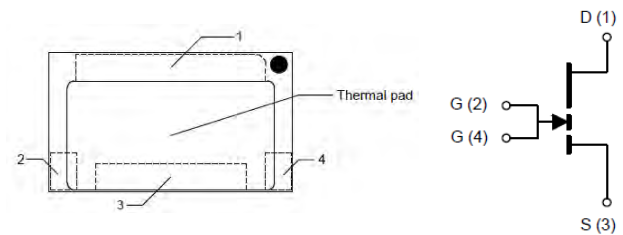
- 100 V enhancement mode power transistor
- Top-side cooled configuration
- $R_{DS(on)} = 7 \text{ m}\Omega$
- $I_{DS(max)} = 90 \text{ A}$
- Ultra-low FOM die
- Low inductance GaNPX® package
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 10 MHz)
- Reverse current capability
- Zero reverse recovery loss
- Small  $7.6 \times 4.6 \text{ mm}^2$  PCB footprint
- Source Sense (SS) pin for optimized gate drive
- Single diffusion lot available
- RoHS compliant
- Enhanced wafer level reliability
- HiRel qualification flow
- Obsolescence support

## Applications

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Motor Drives
- Single $\Phi$  and 3 $\Phi$  inverter legs
- Solar and Wind Power
- Fast Battery Charging
- dc-dc Converters
- On Board Battery Chargers
- E-Switch



## Package Outline    Circuit Symbol



*The top-side thermal pad is internally connected to Source (S pin 3) and substrate*

## Description

The TDG100E90TEP is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** and **GaNPX®** packaging. **Island Technology®** cell layout realizes high-current die and high yield. **GaNPX®** packaging enables low inductance & low thermal resistance in a small package. The TDG100E90TEP is a top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

**Absolute Maximum Ratings (T<sub>case</sub> = 25 °C except as noted)**

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T <sub>J</sub>	-55 to +150	°C
Storage Temperature Range	T <sub>S</sub>	-55 to +150	°C
Drain-to-Source Voltage	V <sub>DS</sub>	100	V
Drain-to-Source Voltage - transient (Note 1)	V <sub>DS(transient)</sub>	120	V
Gate-to-Source Voltage	V <sub>GS</sub>	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)	V <sub>GS(transient)</sub>	-20 to +10	V
Continuous Drain Current (T <sub>case</sub> = 25 °C)	I <sub>DS</sub>	90	A
Continuous Drain Current (T <sub>case</sub> = 100 °C)	I <sub>DS</sub>	65	A
Pulse Drain Current (Pulse width 50 μs, V <sub>GS</sub> = 6 V) (Note 2)	I <sub>DS Pulse</sub>	140	A

(1) For ≤ 1 μs

(2) Defined by product design and characterization. Value is not tested to full current in production.

**Thermal Characteristics (Typical values unless otherwise noted)**

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – Top side	R <sub>θJC</sub>	0.55	°C /W
Maximum Soldering Temperature (MSL3 rated)	T <sub>SOLD</sub>	260	°C

**Ordering Information**

Ordering Code	Package Type/Part Marking	Packing Method	Qty	Reel Diameter	Reel Width	Origin	ECCN
TDG100E90TEP	GaNPX® bottom cooled / TDG90TE	Mini-Reel	250	7" (180 mm)	16mm	US	EAR99
TDG100E90TEPF	GaNPX® bottom cooled / TDG90TF	Mini-Reel	250	7" (180 mm)	16mm	EU	EU

**Electrical Characteristics (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)**

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	100			V	$V_{GS} = 0\text{ V}$ $I_{DSS} = 50\text{ }\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(on)}$	6	7	9.5	m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ $I_{DS} = 27\text{ A}$
Drain-to-Source On Resistance	$R_{DS(on)}$	12.1	17.5	20	m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ $I_{DS} = 27\text{ A}$
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	$V_{DS} = V_{GS}$ , $I_{DS} = 7\text{ mA}$
Gate-to-Source Current	$I_{GS}$		200		$\mu\text{A}$	$V_{GS} = 6\text{ V}$ , $V_{DS} = 0\text{ V}$
Gate Plateau Voltage	$V_{plat}$		3.5		V	$V_{DS} = 50\text{ V}$ $I_{DS} = 90\text{ A}$
Drain-to-Source Leakage Current	$I_{DSS}$		0.5	50	$\mu\text{A}$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 25\text{ }^\circ\text{C}$
Drain-to-Source Leakage Current	$I_{DSS}$		100	265	$\mu\text{A}$	$V_{DS} = 100\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$
Internal Gate Resistance	$R_G$		0.6		$\Omega$	$f = 5\text{ MHz}$ open drain
Input Capacitance	$C_{ISS}$		600		pF	$V_{DS} = 50\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Output Capacitance	$C_{OSS}$		250		pF	
Reverse Transfer Capacitance	$C_{RSS}$		12		pF	
Effective Output Capacitance, Energy Related (Note 3)	$C_{O(ER)}$		302		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 0\text{ to }50\text{ V}$
Effective Output Capacitance, Time Related (Note 4)	$C_{O(TR)}$		385		pF	
Total Gate Charge	$Q_G$		8		nC	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 50\text{ V}$ $I_{DS} = 90\text{ A}$
Gate-to-Source Charge	$Q_{GS}$		3.5		nC	
Gate threshold charge	$Q_{G(th)}$		1.9		nC	
Gate switching charge	$Q_{G(sw)}$		3.3		nC	
Gate-to-Drain Charge	$Q_{GD}$		1.7		nC	
Output Charge	$Q_{OSS}$		20		nC	$V_{GS} = 0\text{ V}$ , $V_{DS} = 50\text{ V}$
Reverse Recovery Charge	$Q_{RR}$		0		nC	

(3)  $C_{O(ER)}$  is the fixed capacitance that would give the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$

(4)  $C_{O(TR)}$  is the fixed capacitance that would give the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$ .

**Electrical Characteristics cont'd (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)**

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Capacitance Stored Energy	$E_{OSS}$		0.4		$\mu\text{J}$	$V_{DS} = 50\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Switching Energy during turn-on	$E_{on}$		2.8		$\mu\text{J}$	$V_{DS} = 50\text{ V}$ , $I_{DS} = 20\text{ A}$ $V_{GS} = -3 - 6\text{ V}$ , $R_{G(on)} = 4.7\ \Omega$ , $R_{G(off)} = 1\ \Omega$
Switching Energy during turn-off	$E_{off}$		1.6		$\mu\text{J}$	$L = 28\ \mu\text{H}$ $L_p = 3.8\text{ nH}$ (Notes 5, 6)

(5)  $L_p$  is the switching circuit parasitic inductance.

(6) See Figure 16 for switching loss test circuit.

**Electrical Performance Graphs**

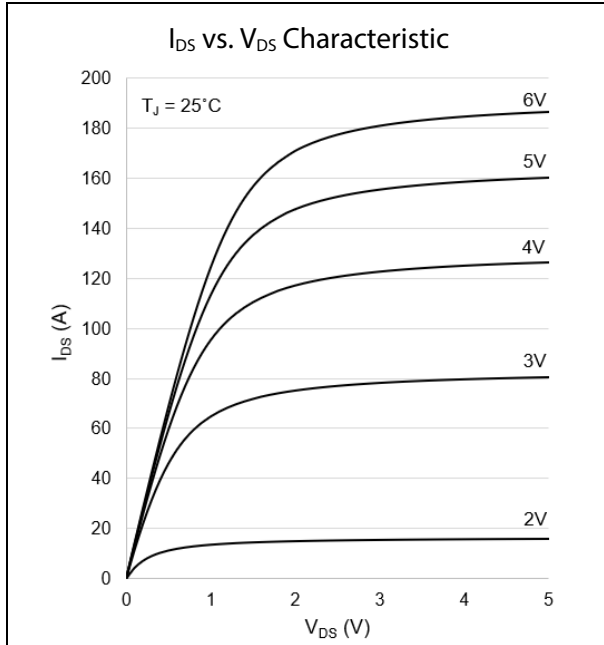


Figure 1: Typical  $I_{DS}$  vs.  $V_{DS}$  @  $T_J = 25^\circ\text{C}$

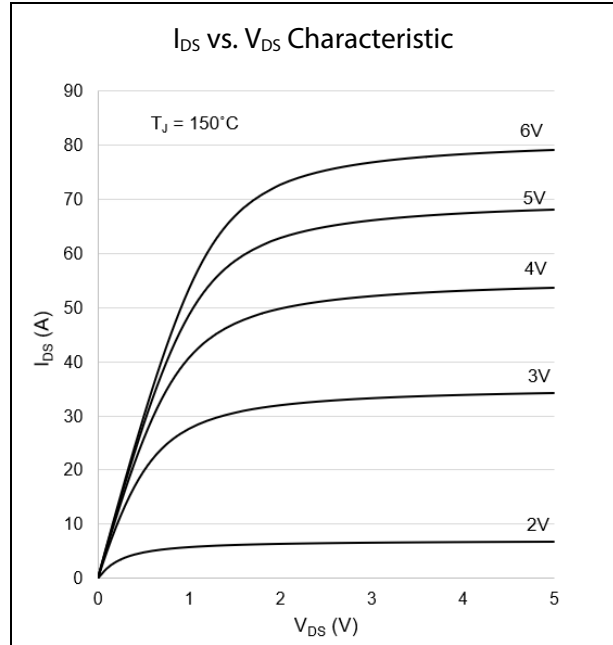


Figure 2: Typical  $I_{DS}$  vs.  $V_{DS}$  @  $T_J = 150^\circ\text{C}$

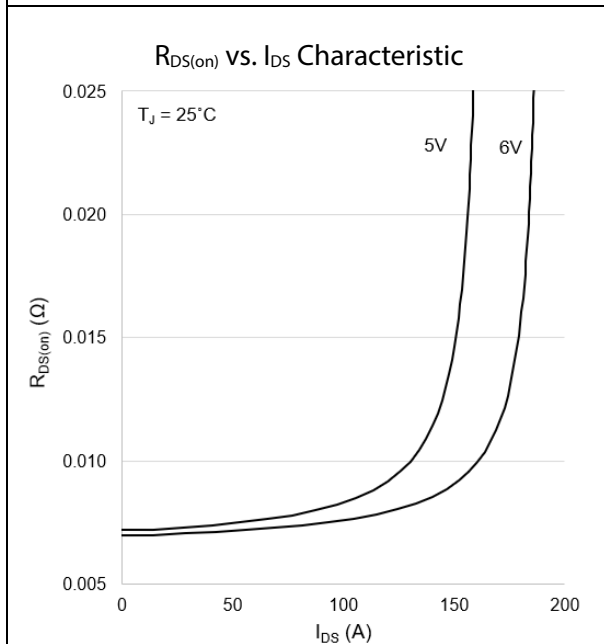


Figure 3:  $R_{DS(on)}$  vs.  $I_{DS}$  at  $T_J = 25^\circ\text{C}$

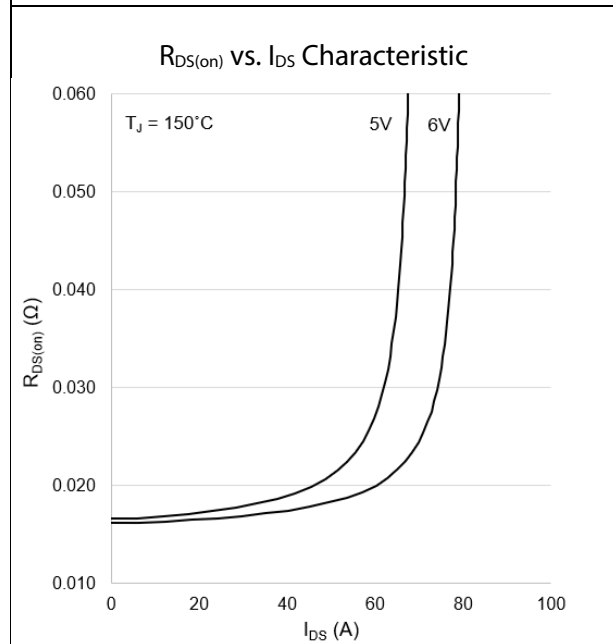
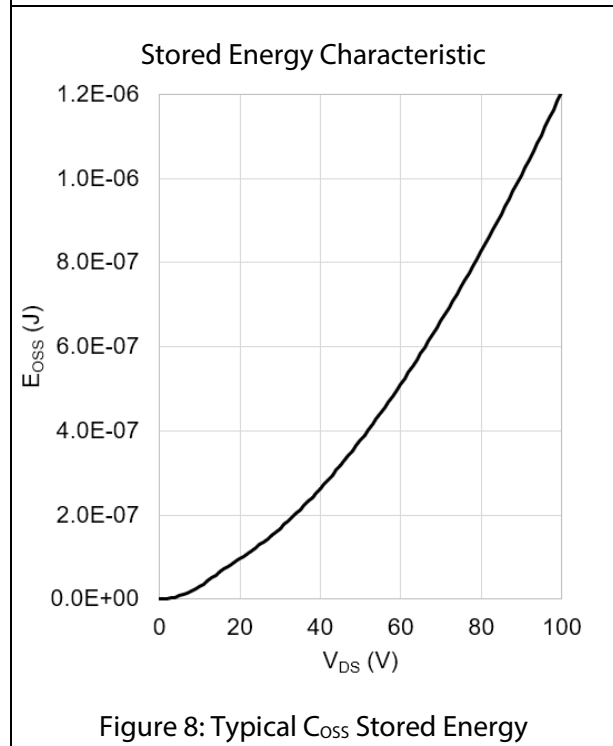
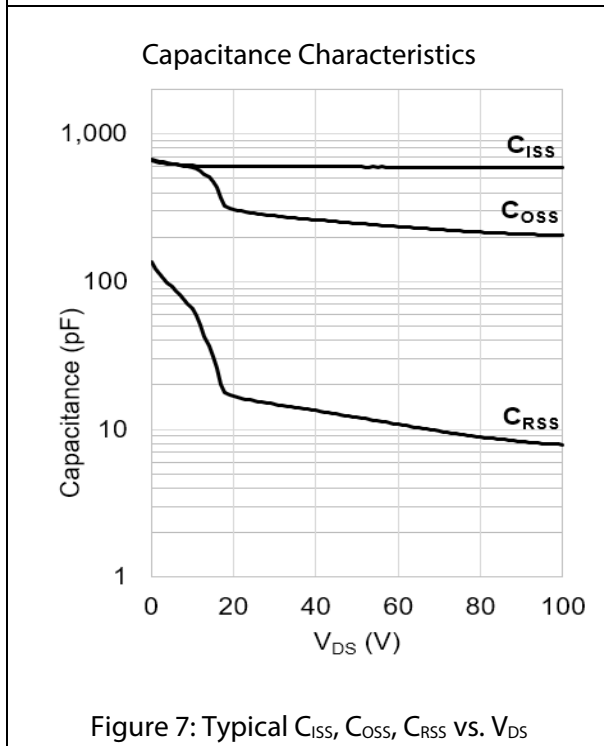
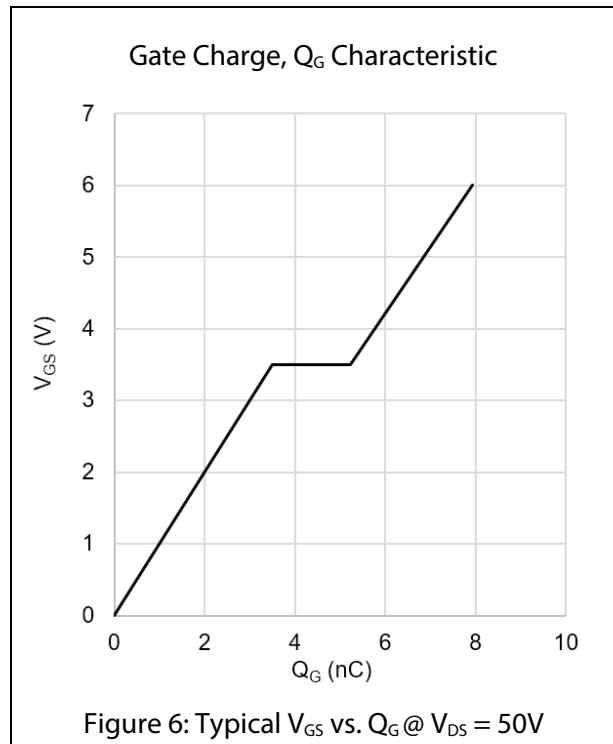
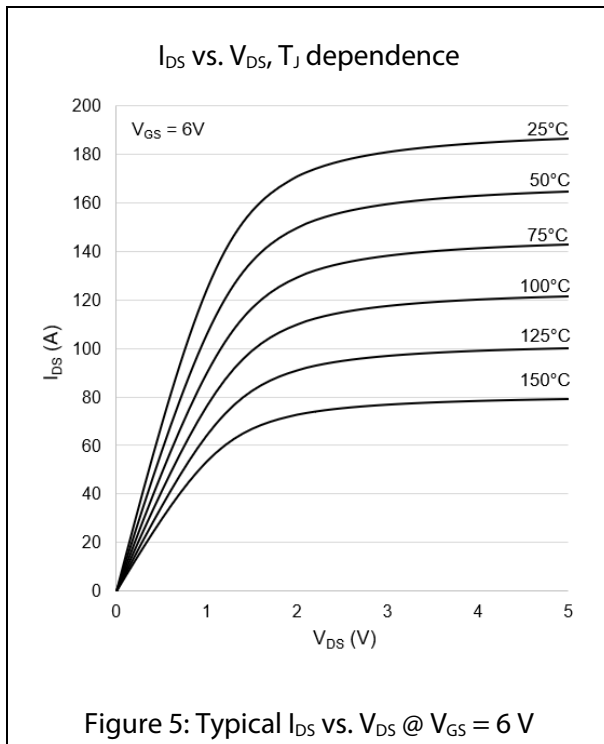


Figure 4:  $R_{DS(on)}$  vs.  $I_{DS}$  at  $T_J = 150^\circ\text{C}$

**Electrical Performance Graphs**



**Electrical Performance Graphs**

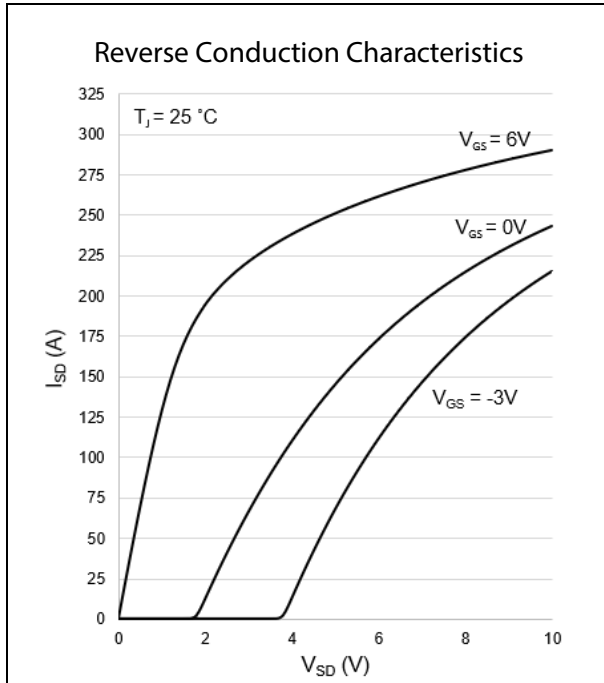


Figure 9: Typical  $I_{SD}$  vs.  $V_{SD}$  at  $T_J = 25^\circ\text{C}$

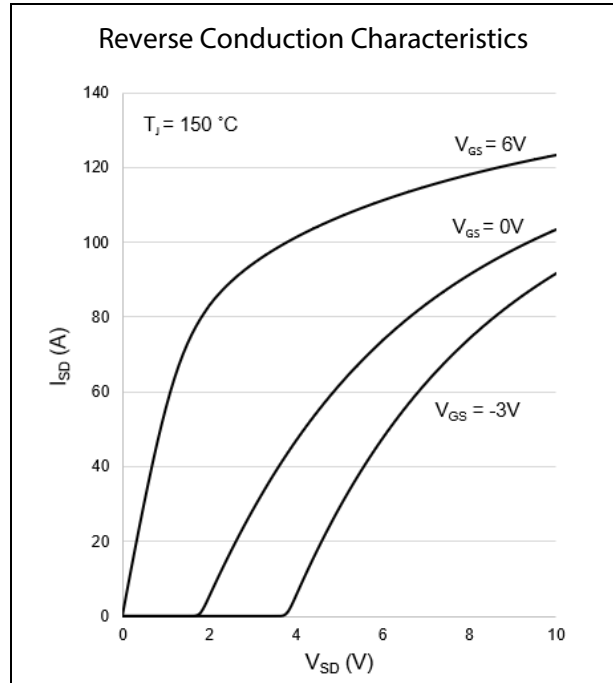


Figure 10: Typical  $I_{SD}$  vs.  $V_{SD}$  at  $T_J = 150^\circ\text{C}$

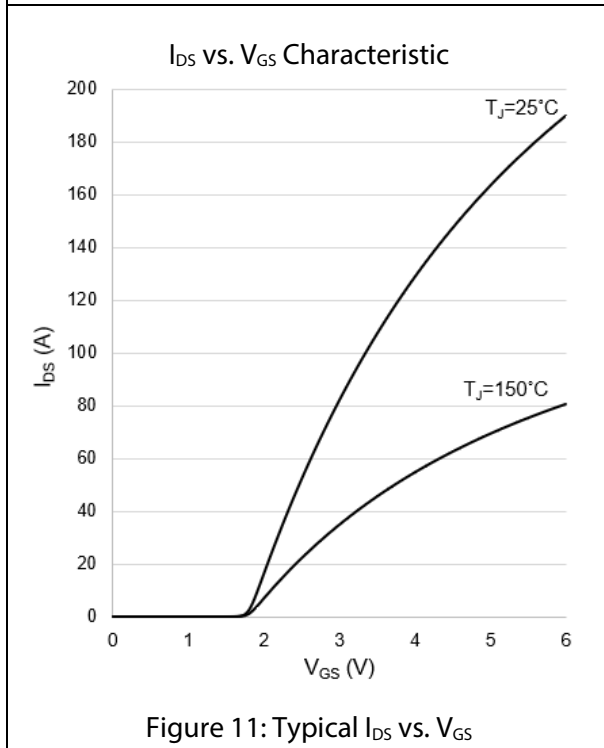


Figure 11: Typical  $I_{DS}$  vs.  $V_{GS}$

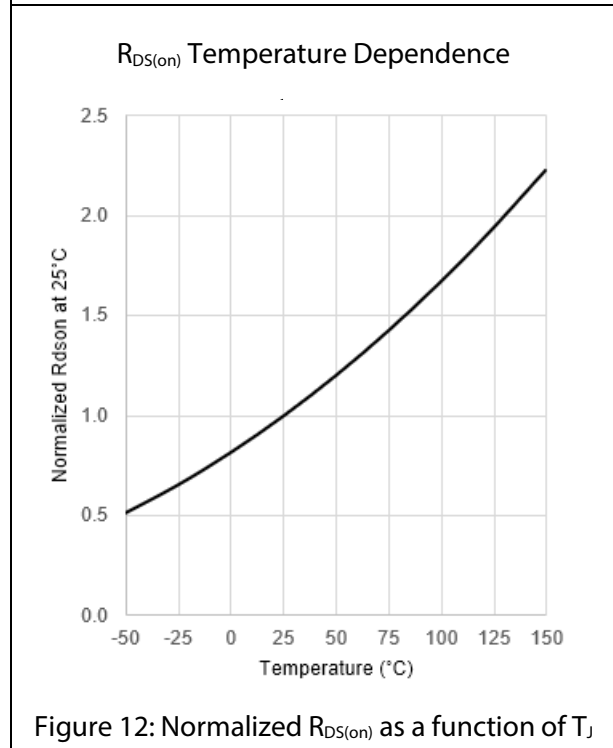
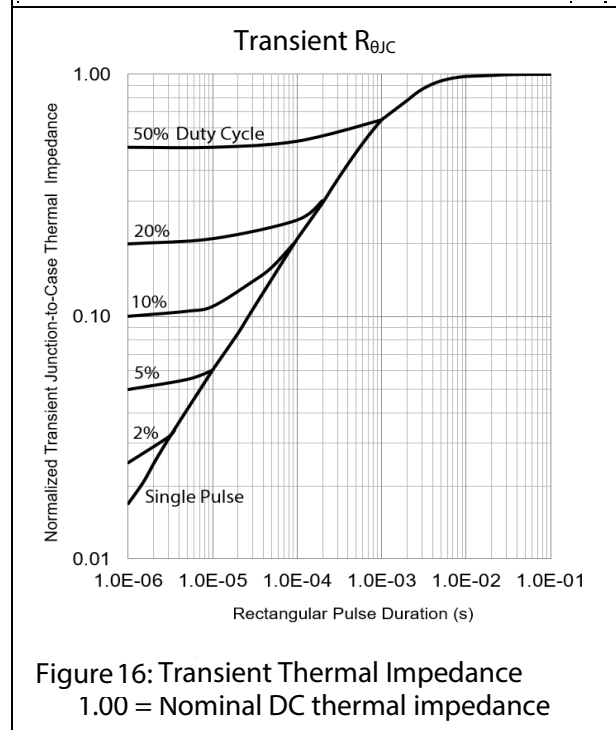
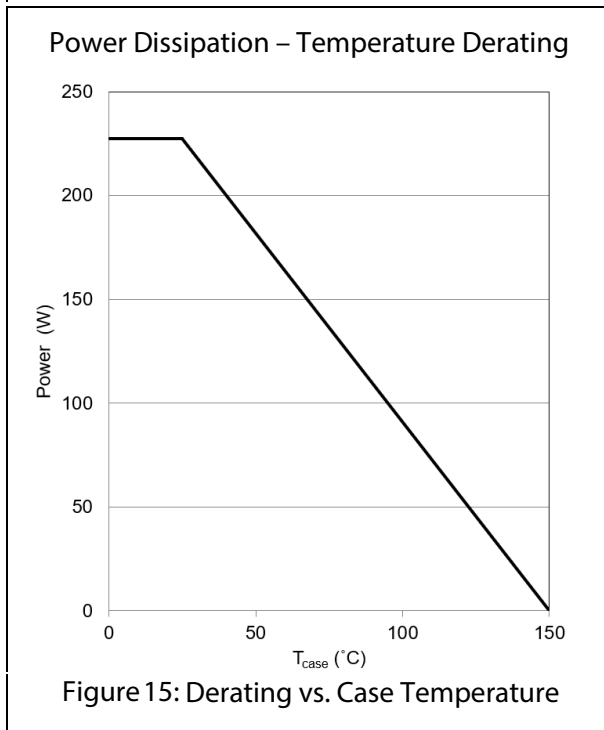
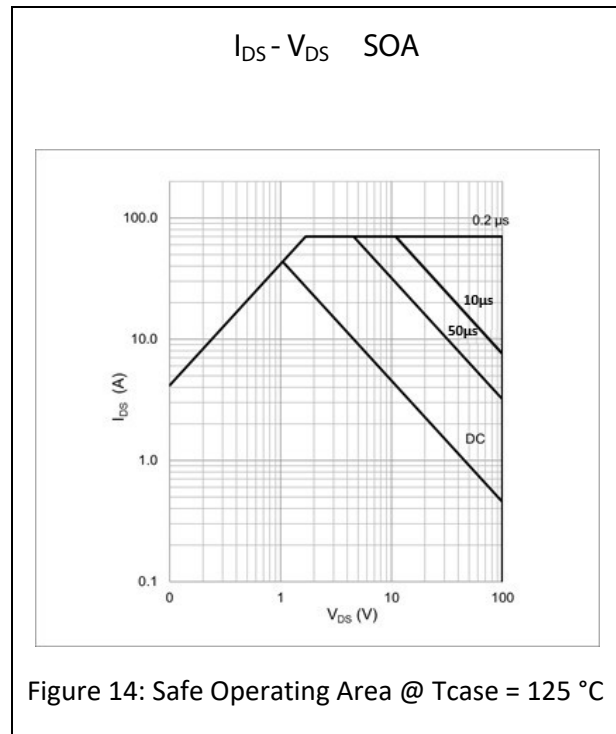
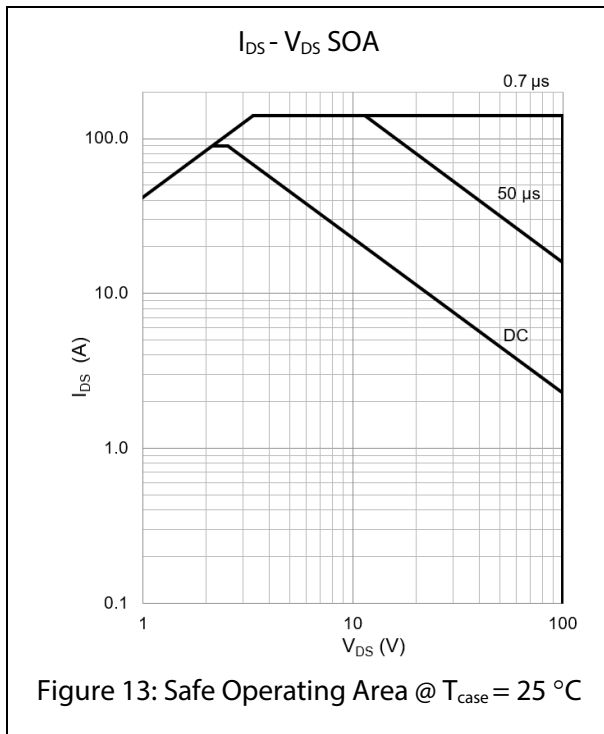


Figure 12: Normalized  $R_{DS(on)}$  as a function of  $T_J$

**Thermal Performance Graphs**





## Test Circuits

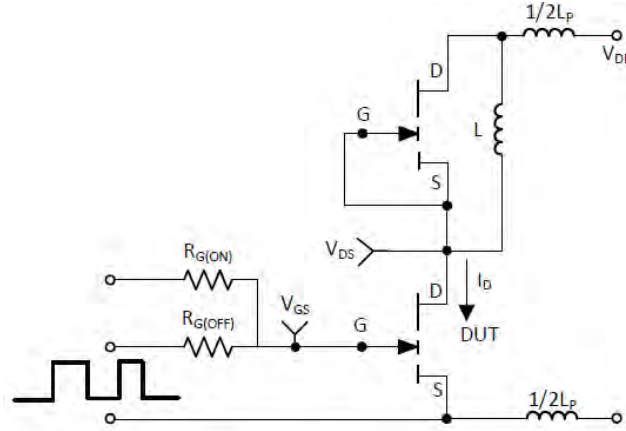


Figure 17: Switching Loss Test Circuit

## Application Information

### Gate Drive

The recommended gate drive voltage range,  $V_{GS}$ , is 0 V to + 6 V for optimal  $R_{DS(on)}$  performance. Also, the repetitive gate to source voltage, maximum rating,  $V_{GS(AC)}$ , is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and - 20 V for pulses up to 1  $\mu$ s. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically  $V_{GS} = -3$  V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at

[www.gansystems.com](http://www.gansystems.com)

Similar to a silicon MOSFET, the external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance,  $R_{G(OFF)}$  is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower  $Q_G$  when compared to equally sized  $R_{DS(on)}$  MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note (GN001) for more details.

### **Parallel Operation**

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the top-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2  $\Omega$ ) on each gate is strongly recommended to minimize the gate parasitic oscillation.

### **Source Sensing**

Although the device does not have a dedicated source sense pin, the GaNPX® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated “source sense” connection on the PCB to the Source pad in a kelvin configuration, the function can easily be implemented. It is recommended to implement a “source sense” connection to improve drive performance.

### **Thermal**

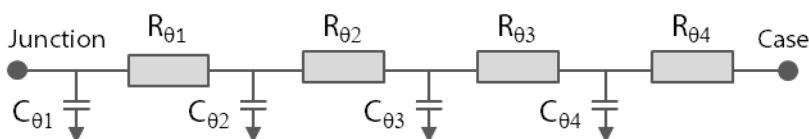
The substrate is internally connected to the thermal pad on the top-side and to the source pin on the bottom side of the package. The transistor is designed to be cooled using a heat sink on the top of the device.

The Drain and Source pads are not as thermally conductive as a thermal pad. However, adding more copper under these two pads will improve thermal performance by reducing the packaging temperature.

### **Thermal Modeling**

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This thermal model can be extended to the system level by adding extra  $R\theta$  and  $C\theta$  to simulate the Thermal Interface Material (TIM) or Heatsink.

RC Thermal Model:



RC breakdown of  $R_{\theta JC}$

$R_{\theta}$ ( $^{\circ}\text{C}/\text{W}$ )	$C_{\theta}$ ( $\text{W}\cdot\text{s}/^{\circ}\text{C}$ )
$R_{\theta 1} = 0.017$	$C_{\theta 1} = 7.0\text{E-}05$
$R_{\theta 2} = 0.253$	$C_{\theta 2} = 6.7\text{E-}04$
$R_{\theta 3} = 0.264$	$C_{\theta 3} = 5.9\text{E-}03$
$R_{\theta 4} = 0.016$	$C_{\theta 4} = 1.8\text{E-}03$

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaNPX® Using RC Thermal SPICE Models” available at [www.gansystems.com](http://www.gansystems.com).

### Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition ( $V_{GS} = +6\text{ V}$ ): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance,  $R_{DS(on)}$ , similar to forward conduction operation.

Off-state condition ( $V_{GS} \leq 0\text{ V}$ ): The reverse characteristics in the off-state are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, ( $V_{GD}$ ) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher  $V_F$  and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than  $V_{GS(th)} + V_{GS(off)}$  in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “ $V_F$ ” and hence increase the reverse conduction loss.

### Blocking Voltage

The blocking voltage rating,  $V_{(BL)DSS}$ , is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated  $V_{(BL)DSS}$ . As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 100 V and does not change

with negative gate voltage. GaN Systems tests devices in production with a 120 V drain-to-source voltage pulse to insure blocking voltage margin.

### **Packaging and Soldering**

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

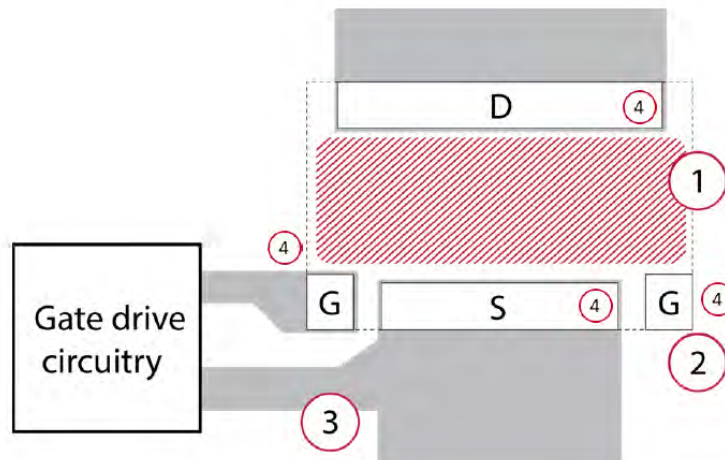
- Preheat/Soak: 60 - 120 seconds.  $T_{min} = 150\text{ °C}$ ,  $T_{max} = 200\text{ °C}$ .
- Reflow: Ramp up rate 3°C/s maximum. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/s maximum.

Using “No-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “No-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “No-Clean” paste residues.

Avoid placing printed circuit board traces with high differential voltage to the source or drain directly underneath the top-cooled TDG100E90TEP package on the PCB to avoid potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation

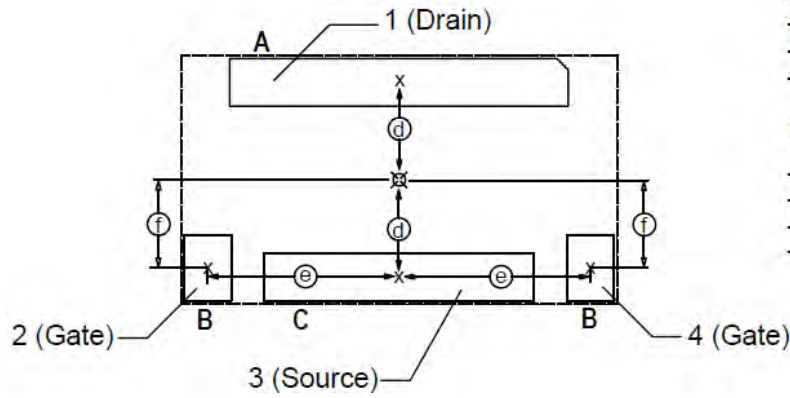
## Routing Guidelines

The following layout recommendations are highlighted. Additional detail is provided in Application Note GN001 at [www.gansystems.com](http://www.gansystems.com).



- ① Keep out area: Avoid placing traces or vias on the top layer of the PCB, directly underneath the package. This is to prevent potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.
- ② Symmetrical dual gates are provided for flexible layout and easy paralleling. Either gate drive can be used. If the second gate is not used, it should be left floating.
- ③ A separate Source Sense pin is not provided on our top-side products because of the ultra-low inductance of our GaNPX® packaging. The Source Sense pin functionality can be implemented simply by routing a Kelvin connection at the side of the Source pad. This can be done at either side of the source pad for layout optimization.
- ④ Do not route vias within the Gate pad as it may affect long term solder joint reliability. For other pads, it is recommended to implement filled vias for better solder joint reliability.

**Recommended PCB Footprint**





**Pad sizes**

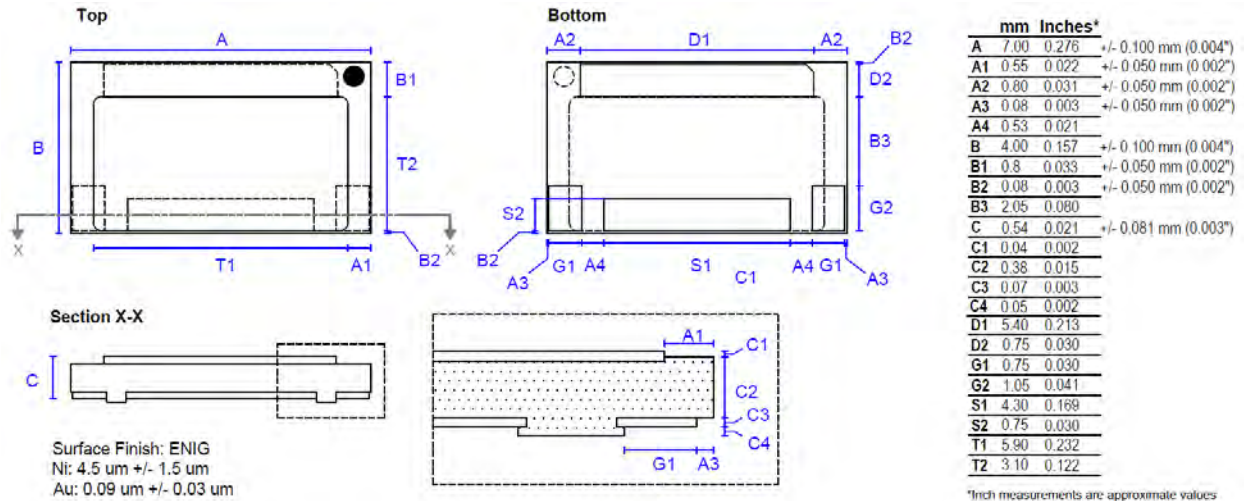
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
<b>A</b>	5.40	0.75	0.213	0.030
<b>B</b>	0.75	1.05	0.030	0.040
<b>C</b>	4.30	0.75	0.170	0.030

**Dimensions**

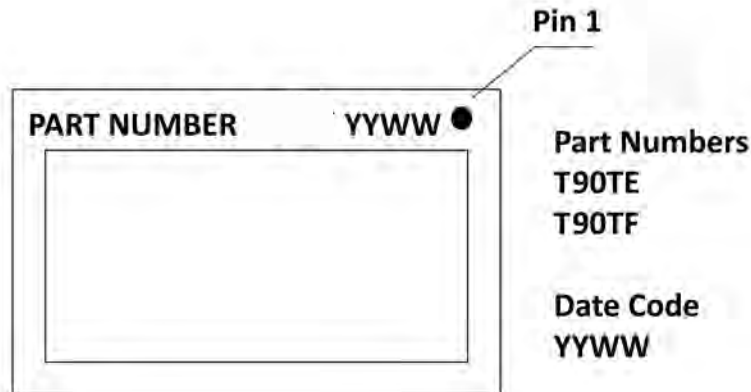
	mm	Inches
<b>d</b>	1.57	0.062
<b>e</b>	3.05	0.120
<b>f</b>	1.40	0.056

-  PCB pad openings
-  Package outline

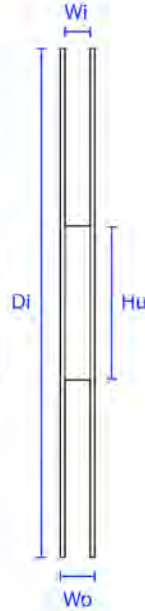
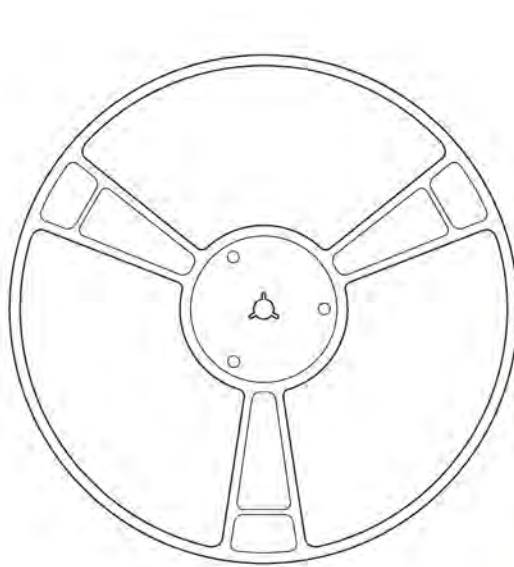
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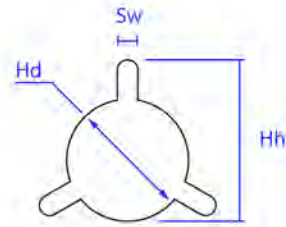
**Part Marking**



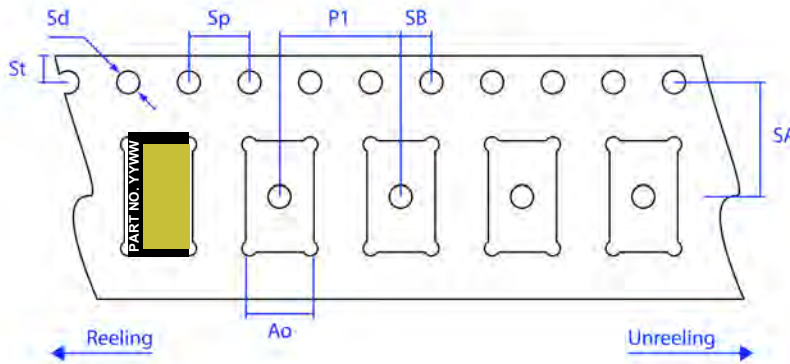
**Tape and Reel Information**



	Dimensions (mm)			
	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
<b>Di</b>	330.0	+/- 2.0	178.0	+1.0 / - 0.0
<b>Wo</b>	22.4	MAX	22.4	MAX
<b>Wi</b>	16.8	+1.6 / - 0.4	16.4	+2.0 / - 0.0
<b>Hu</b>	102.0	+/- 2.0	60.0	+1.0 / - 0.0
<b>Hh</b>	16.6	+0.5 / - 0.2	17.0	+/- 0.8
<b>Sw</b>	2.0	+/- 0.5	2.0	+/- 0.5
<b>Hd</b>	13.0	+0.5 / - 0.2	13.0	+/- 0.2



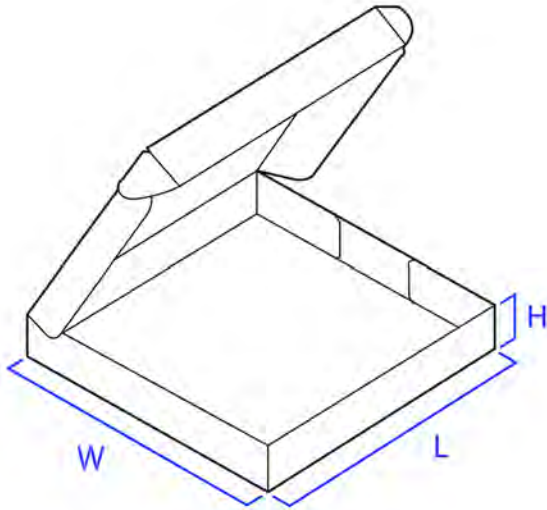
Note: Wo and Wi measured at hub



	Dimensions (mm)	
	Nominal	Tolerance
<b>P1</b>	8.00	+/- 0.1
<b>W</b>	16.00	+0.3 / - 0.1
<b>Ko</b>	0.80	+/- 0.1
<b>Ao</b>	4.50	+/- 0.1
<b>Bo</b>	7.30	+/- 0.1
<b>Sp</b>	4.00	+/- 0.02
<b>Sd</b>	1.50	+0.1 / - 0.0
<b>St</b>	1.75	+/- 0.1
<b>SA</b>	7.50	+/- 0.1
<b>SB</b>	2.00	+/- 0.1



**Tape and Reel Box Dimensions**



Outside dimensions (mm)		
	7" mini-reel	13" tape-reel
<b>W</b>	206.5	340
<b>L</b>	218.5	355
<b>H</b>	32	50

**Document Revision History:**

Document No.	Description	Date
TDG100E90TEP_09_30_2021 Rev 1	Initial Release	9/30/2021

**Document Categories**

**Advance Information**

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

**Preliminary Specification**

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

**Product Specification**

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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