**Features**

- 100 V enhancement mode GaN power switch
- Bottom-side cooled configuration
- RDS(on) = 7 mΩ
- IDS(max) = 90 A
- Ultra-low FOM Island Technology® die
- Low inductance GaNPX® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Reverse current capability
- Zero reverse recovery loss
- Small 7.6 x 4.6 mm² PCB footprint
- Source Sense (SS) pin for optimized gate drive
- Single diffusion lot available
- RoHS compliant
- Enhanced wafer level reliability
- HiRel qualification flow
- Class one / Level one Production Screening
- Lot Acceptance Test options available
- Obsolescence support

**Applications**

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Space Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- dc-dc Converters
- On Board Battery Chargers
- E-Switch

**Description**

The TDG100E90BSP is an enhancement mode GaN-on-silicon power transistor based on GaN Systems Technology. The properties of GaN ensure high current, high voltage breakdown combined with high switching frequency. GaN Systems implements patented Island Technology® cell layout for high-current performance.

GaNPX® packaging is designed for very low parasitic inductance in the smallest possible footprint. The TDG100E90BSP is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combined provide very high efficiency power switching. The high performance of the TDG650E30BSP makes it ideal for satellite applications.

These parts go through NASA Level 1 or ESA Class 1 screening flow and can be brought up to full Level 1 conformance with extra qualification testing, if desired. Each device is available with options for EAR99 or European sourcing.
**Absolute Maximum Ratings (T_{case} = 25 °C except as noted)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Junction Temperature</td>
<td>T_{J}</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>T_{S}</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>Drain-to-Source Voltage</td>
<td>V_{DS}</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Drain-to-Source Voltage - transient (note 1)</td>
<td>V_{DS(transient)}</td>
<td>120</td>
<td>V</td>
</tr>
<tr>
<td>Gate-to-Source Voltage</td>
<td>V_{GS}</td>
<td>-10 to +7</td>
<td>V</td>
</tr>
<tr>
<td>Gate-to-Source Voltage - transient (note 1)</td>
<td>V_{GS(transient)}</td>
<td>-20 to +10</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Drain Current (T_{case} = 25 °C)</td>
<td>I_{DS}</td>
<td>90</td>
<td>A</td>
</tr>
<tr>
<td>Continuous Drain Current (T_{case} = 100 °C)</td>
<td>I_{DS}</td>
<td>65</td>
<td>A</td>
</tr>
<tr>
<td>Pulse Drain Current (Pulse width 50 μs, V_{GS} = 6 V)</td>
<td>I_{DS Pulse}</td>
<td>140</td>
<td>A</td>
</tr>
</tbody>
</table>

(1) Pulse ≤1 μs

**Thermal Characteristics (Typical values unless otherwise noted)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance (junction-to-case)</td>
<td>R_{ΘJC}</td>
<td>0.55</td>
<td>°C /W</td>
</tr>
<tr>
<td>Thermal Resistance (junction-to-top)</td>
<td>R_{ΘJT}</td>
<td>7</td>
<td>°C /W</td>
</tr>
<tr>
<td>Thermal Resistance (junction-to-ambient) (note 3)</td>
<td>R_{ΘJA}</td>
<td>23</td>
<td>°C /W</td>
</tr>
<tr>
<td>Maximum Soldering Temperature (MSL3 rated)</td>
<td>T_{SOLD}</td>
<td>260</td>
<td>°C</td>
</tr>
</tbody>
</table>

(2) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm² each. The PCB is mounted in horizontal position without air stream cooling.
## Electrical Characteristics

Typical values at $T_J = 25 \, ^\circ C$, $V_{GS} = 6 \, V$. Unless otherwise noted, Min/Max values are specified over the full temperature range from $T_J = -55 \, ^\circ C$ to $T_J = 150 \, ^\circ C$ based on Teledyne Dynamic Burn-In$^5$ after 15k Cycles.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-to-Source Blocking Voltage</td>
<td>$BV_{DS}$</td>
<td>100</td>
<td>V</td>
<td>V</td>
<td>$V_{GS} = 0 , V$, $I_{DS} = 50 , \mu A$</td>
<td></td>
</tr>
<tr>
<td>Drain-to-Source On Resistance</td>
<td>$R_{DS(on)}$</td>
<td>6</td>
<td>7</td>
<td>9.5</td>
<td>mΩ</td>
<td>$V_{GS} = 6 , V$, $T_J = 25 , ^\circ C$, $I_{DS} = 27 , A$</td>
</tr>
<tr>
<td>Drain-to-Source On Resistance</td>
<td>$R_{DS(on)}$</td>
<td>12.1</td>
<td>17.5</td>
<td>20</td>
<td>mΩ</td>
<td>$V_{GS} = 6 , V$, $T_J = 150 , ^\circ C$, $I_{DS} = 27 , A$</td>
</tr>
<tr>
<td>Dynamic Drain-to-Source On Resistance Shift</td>
<td>$DR_{DS(on)}$</td>
<td>8.1</td>
<td>%</td>
<td></td>
<td></td>
<td>$V_{GS} = 6 , V$, $T_J = 25 , ^\circ C$, $I_{DS} = 27 , A$</td>
</tr>
<tr>
<td>Gate-to-Source Threshold</td>
<td>$V_{GS(th)}$</td>
<td>1.1</td>
<td>1.7</td>
<td>2.6</td>
<td>V</td>
<td>$V_{DS} = V_{GS}$, $I_{DS} = 7 , mA$</td>
</tr>
<tr>
<td>Gate-to-Source Current</td>
<td>$I_{GS}$</td>
<td>0.20</td>
<td>6</td>
<td>mA</td>
<td></td>
<td>$V_{GS} = 6 , V$, $V_{DS} = 0 , V$, $T_J = 150 , ^\circ C$</td>
</tr>
<tr>
<td>Gate Plateau Voltage</td>
<td>$V_{plat}$</td>
<td>3.5</td>
<td>V</td>
<td></td>
<td></td>
<td>$V_{DS} = 100 , V$, $I_{DS} = 90 , A$</td>
</tr>
<tr>
<td>Drain-to-Source Leakage Current</td>
<td>$I_{DSS}$</td>
<td>0.5</td>
<td>50</td>
<td>μA</td>
<td></td>
<td>$V_{DS} = 100 , V$, $V_{GS} = 0 , V$, $T_J = 25 , ^\circ C$</td>
</tr>
<tr>
<td>Drain-to-Source Leakage Current</td>
<td>$I_{DSS}$</td>
<td>100</td>
<td>265</td>
<td>μA</td>
<td></td>
<td>$V_{DS} = 100 , V$, $V_{GS} = 0 , V$, $T_J = 150 , ^\circ C$</td>
</tr>
<tr>
<td>Internal Gate Resistance</td>
<td>$R_{G}$</td>
<td>0.77</td>
<td>Ω</td>
<td></td>
<td></td>
<td>$f = 1 , MHz$, open drain</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{ISS}$</td>
<td>600</td>
<td>pF</td>
<td></td>
<td></td>
<td>$V_{DS} = 50 , V$</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>$C_{OSS}$</td>
<td>250</td>
<td>pF</td>
<td></td>
<td></td>
<td>$V_{GS} = 0 , V$</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>$C_{RSS}$</td>
<td>12</td>
<td>pF</td>
<td></td>
<td></td>
<td>$f = 1 , MHz$</td>
</tr>
<tr>
<td>Effective Output Capacitance, Energy Related (Note 4)</td>
<td>$C_{O(ER)}$</td>
<td>351</td>
<td>pF</td>
<td></td>
<td></td>
<td>$V_{GS} = 0 , V$, $V_{DS} = 0$ to 50 V</td>
</tr>
<tr>
<td>Effective Output Capacitance, Time Related (Note 5)</td>
<td>$C_{O(TR)}$</td>
<td>433</td>
<td>pF</td>
<td></td>
<td></td>
<td>$V_{GS} = 0 , V$, $V_{DS} = 0$ to 50 V</td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>$Q_{G}$</td>
<td>8</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-to-Source Charge</td>
<td>$Q_{GS}$</td>
<td>3.5</td>
<td>nC</td>
<td></td>
<td></td>
<td>$V_{DS} = 0$ to 6 V</td>
</tr>
<tr>
<td>Gate threshold charge</td>
<td>$Q_{GS(th)}$</td>
<td>1.9</td>
<td>nC</td>
<td></td>
<td></td>
<td>$V_{DS} = 50 , V$, $I_{DS} = 90A$</td>
</tr>
<tr>
<td>Gate switching charge</td>
<td>$Q_{GS(sw)}$</td>
<td>4.1</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-to-Drain Charge</td>
<td>$Q_{GD}$</td>
<td>1.7</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Charge</td>
<td>$Q_{OSS}$</td>
<td>21.3</td>
<td>nC</td>
<td></td>
<td></td>
<td>$V_{GS} = 0 , V$, $V_{DS} = 50 , V$</td>
</tr>
<tr>
<td>Reverse Recovery Charge</td>
<td>$Q_{RR}$</td>
<td>0</td>
<td>nC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics (Continued)

<table>
<thead>
<tr>
<th></th>
<th>$E_{oss}$</th>
<th>$\mu J$</th>
<th>$V_{DS} = 50 , V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Capacitance Stored Energy</td>
<td>0.39</td>
<td></td>
<td>$V_{GS} = 0 , V$</td>
</tr>
<tr>
<td>Switching Energy during turn-on</td>
<td>$E_{on}$</td>
<td>2.8</td>
<td>$f = 100 , kHz$</td>
</tr>
<tr>
<td>Switching Energy during turn-off</td>
<td>$E_{off}$</td>
<td>1.6</td>
<td></td>
</tr>
</tbody>
</table>

(3) $C_{QoER}$ is the fixed capacitance that would give the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 V to the stated $V_{DS}$.

(4) $C_{QoTR}$ is the fixed capacitance that would give the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 V to the stated $V_{DS}$.

(5) $L_P$ is the switching circuit parasitic inductance.

(6) See Figure 20 for switching loss test circuit.
Electrical Performance Graphs

**Figure 1:** Typical $I_{ds}$ vs. $V_{ds}$ @ $T_j = 25 \, ^\circ C$

**Figure 2:** Typical $I_{ds}$ vs. $V_{ds}$ @ $T_j = 150 \, ^\circ C$

**Figure 3:** $R_{ds(on)}$ vs. $I_{ds}$ at $T_j = 25 \, ^\circ C$

**Figure 4:** $R_{ds(on)}$ vs. $I_{ds}$ at $T_j = 150 \, ^\circ C$
Electrical Performance Graphs (continued)

Figure 5: Typical $I_{DS}$ vs. $V_{DS}$ @ $V_{GS} = 6$ V

Figure 6: Typical $V_{GS}$ vs. $Q_{G}$ @ $V_{DS} = 50$ V

Figure 7: Typical $C_{ISS}$, $C_{DSS}$, $C_{RSS}$ vs. $V_{DS}$

Figure 8: Typical $C_{DSS}$ Stored Energy
Electrical Performance Graphs (continued)

TDG100E90BSP Reverse Conduction Characteristics

**Figure 9:** Typical $I_{DS}$ vs. $V_{SD}$ at $T_J = 25°C$

**Figure 10:** Typical $I_{DS}$ vs. $V_{SD}$ at $T_J = 150°C$

TDG100E90BSP $I_{DS}$ vs. $V_{GS}$ Characteristic

**Figure 11:** Typical $I_{DS}$ vs. $V_{GS}$

TDG100E90BSP $R_{DS(on)}$ Temperature Dependence

**Figure 12:** Normalized $R_{DS(on)}$ as a function of $T_J$
Electrical Performance Graphs (continued)

**Figure 13: IGS vs VGS - Typical Values**

**Figure 14: IG vs VGS (log scale) - Typical Values**
Electrical Performance Graphs (continued)

Figure 15: $V_{th}$ vs. $V_{ds}$ Voltages
Thermal Performance Graphs

Figure 16: Safe Operating Area @ $T_{case} = 25 \, ^\circ C$

Figure 17: Safe Operating Area @ $T_{case} = 125 \, ^\circ C$

Figure 18: Power Derating vs. $T_{case}$

Figure 19: Transient Thermal Impedance
Test Circuit

Figure 20: TDG100E90BSP Switching Loss Test Circuit
Gate Drive

The recommended gate drive voltage is 0 V to +6 V for optimal \( R_{\text{DS(on)}} \) performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and −20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate. However, it increases the reverse conduction loss. Negative gate bias operation helps to reduce dynamic \( \text{rDSON} \) increases due to trapped charges. Operating at a zero gate bias can result in up to 30% shift in dynamic \( \text{rDSON} \). For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at www.gansystems.com.

Similar to a silicon MOSFET, the external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, \( R_{\text{G(OFF)}} \) is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower \( Q_g \) when compared to equally sized \( R_{\text{DS(on)}} \) MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.
Source Sensing
The TDG100E90BSP has a dedicated source sense pin. The GaNPx® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad on the TDG100E90BSP and returning from the source sense pad on the TDG100E90BSP to the driver ground reference.

Thermal
The substrate is internally connected to the thermal pad on the bottom-side of the TDG100E90BSP. The source pad must be electrically connected to the thermal pad for optimal performance. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling
RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra $R_\theta$ and $C_\theta$ to simulate the Thermal Interface Material (TIM) or Heatsink.

The RC elements are assigned to the internal layers of the TDG100E90BSP as follows

![Thermal Model Diagram]

**RC breakdown of $R_{GIC}$**

<table>
<thead>
<tr>
<th>$R_\theta$ (°C/W)</th>
<th>$C_\theta$ (W·s/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\theta1}$ = 0.024</td>
<td>$C_{\theta1}$ = 3.92E-05</td>
</tr>
<tr>
<td>$R_{\theta2}$ = 0.372</td>
<td>$C_{\theta2}$ = 2.73E-03</td>
</tr>
<tr>
<td>$R_{\theta3}$ = 0.128</td>
<td>$C_{\theta3}$ = 6.14E-04</td>
</tr>
<tr>
<td>$R_{\theta4}$ = 0.026</td>
<td>$C_{\theta4}$ = 9.30E-04</td>
</tr>
</tbody>
</table>

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaNPx® Using RC Thermal SPICE Models” available at www.gansystems.com
Reverse Conduction

GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition ($V_{GS} = +6$ V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, $V_{GD}$, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher $V_F$ and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)} + V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “$V_F$” and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS}$, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated $BV_{DS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 100 V and doesn’t change with negative gate voltage. A transient drain-to-source voltage of 130 V for 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the TDG100E90BSP device to be specified to 150 °C ($T_j$). The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. $T_{min} = 150$ °C, $T_{max} = 200$ °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using “Non-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “Non-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the “Non-Clean” paste residues. For more details, please refer to the soldering application note “GN011-Soldering-Recommendations- for-GaNPX®-Packaged-Devices” at www.gansystems.com
Recommended PCB Footprint for TDG100E90BSP

Recommended Solder Stencil for TDG100E90BSP PCB Footprint

Dimension of stencil aperture
- 0.5 x 0.5 mm
- 1.43 x 0.5 mm
- 0.97 x 0.97 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

Thermal pad
NOTE: Thermal pad must be connected to Source (pad 4) for best performance

**Technical Specifications**

- **Part Number**: TDG100E90BSP
- **Type**: Bottom-side cooled, 100V E-mode GaN transistor
- **Manufacturer**: Teledyne e2v HiRel Electronics

© 2023 Teledyne e2v HiRel Electronics. All rights reserved.
Package Dimensions

Note: Inch measurements are approximate values

GaNpx® Part Marking

Logo

Pin 1

Part number

Pb-free category

e4 - pre-plated Au

Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm
Tape and Reel Box Dimensions

<table>
<thead>
<tr>
<th>Outside dimensions (mm)</th>
<th>7” mini-reel</th>
<th>13” tape-reel</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>197</td>
<td>342</td>
</tr>
<tr>
<td>L</td>
<td>204</td>
<td>355</td>
</tr>
<tr>
<td>H</td>
<td>32</td>
<td>53</td>
</tr>
</tbody>
</table>

Ordering Information

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>Package Type/Part Marking</th>
<th>Packing Method</th>
<th>Qty</th>
<th>Reel Diameter</th>
<th>Reel Width</th>
<th>Origin</th>
<th>ECCN</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDG100E90BSP</td>
<td>GaNPX® bottom cooled / TDG90BE</td>
<td>Mini-Reel</td>
<td>250</td>
<td>7” (180 mm)</td>
<td>16mm</td>
<td>US</td>
<td>EAR99</td>
</tr>
<tr>
<td>TDG100E90BSPF</td>
<td>GaNPX® bottom cooled / TDG90BF</td>
<td>Mini-Reel</td>
<td>250</td>
<td>7” (180 mm)</td>
<td>16mm</td>
<td>EU</td>
<td>EU</td>
</tr>
</tbody>
</table>
Document Definitions and Categories

Advance Information
The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification
The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification
The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact
For additional information, Email us at: tdemarketing@teledyne.com

Disclaimers
The information in this document is believed to be reliable. However, Teledyne e2v HiRel Electronics assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Teledyne e2v's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Teledyne e2v product could create a situation in which personal injury or death might occur. Teledyne e2v assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Copyright and Trademark
Trademarks are the property of their respective owners.

©2023, Teledyne e2v HiRel Electronics. All rights reserved.