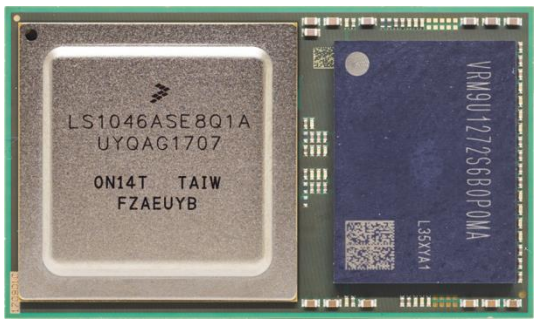
QLS1046A, QLS1026A

Qormino Integrated Multicore communication processor with 4GB of DDR4
Preliminary Product brief



Features

- QLS1046A has four cores and QLS1026A has two cores
- 4GB of DDR4 with ECC
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (FMan)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
  - IEEE 1588™ support
- Two RGMII interfaces
- Eight SerDes lanes for high-speed peripheral interfaces
  - Three PCI Express 3.0 controllers
  - One Serial ATA (SATA 6 Gbit/s) controller
  - Up to two XFI (10 GbE) interfaces
  - Up to five SGMII interfaces supporting 1000 Mbps
  - Up to three SGMII interfaces supporting 2500 Mbps
  - Up to one QSGMII interface
  - Supports 10GBase-KR
  - Supports 1000Base-KX
- Additional peripheral interfaces
  - One Quad Serial Peripheral Interface (QSPI) controller
  - One Serial Peripheral Interface (SPI) controller
  - Integrated flash controller (IFC) supporting NAND and NOR flash
  - Three high-speed USB 3.0 controllers with integrated PHY
  - One Enhanced Secure Digital Host Controller supporting SD 3.0, eMMC 4.4, and eMMC 4.5
  - Four I2C controllers
  - Two 16550-compliant DUARTs and six low-power UARTs (LPUARTs)
  - General purpose IO (GPIO), eight Flextimers
  - One Queue Direct Memory Access Controller (qDMA)
  - One Enhanced Direct Memory Access Controller (eDMA)
  - Global programmable interrupt controller (GIC)
  - Thermal monitoring unit (TMU)
- 1415 FC-PBGA package, 26 mm x 44 mm

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1 INTRODUCTION

The QLS1046A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the TELEDYNE-E2V value-performance line of QorIQ communications processors. Featuring power-efficient 64-bit Arm® Cortex®-A72 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.8 GHz.

The QLS1046A and QLS1026A processors are perfectly suited for a range of embedded applications such as enterprise routers and switches, linecard controllers, network attached storage, security appliances, virtual customer premise equipment (vCPE), service providers gateways, and single board computers.

This figure shows the block diagram of the chip.

Figure 1. QLS1046A block diagram

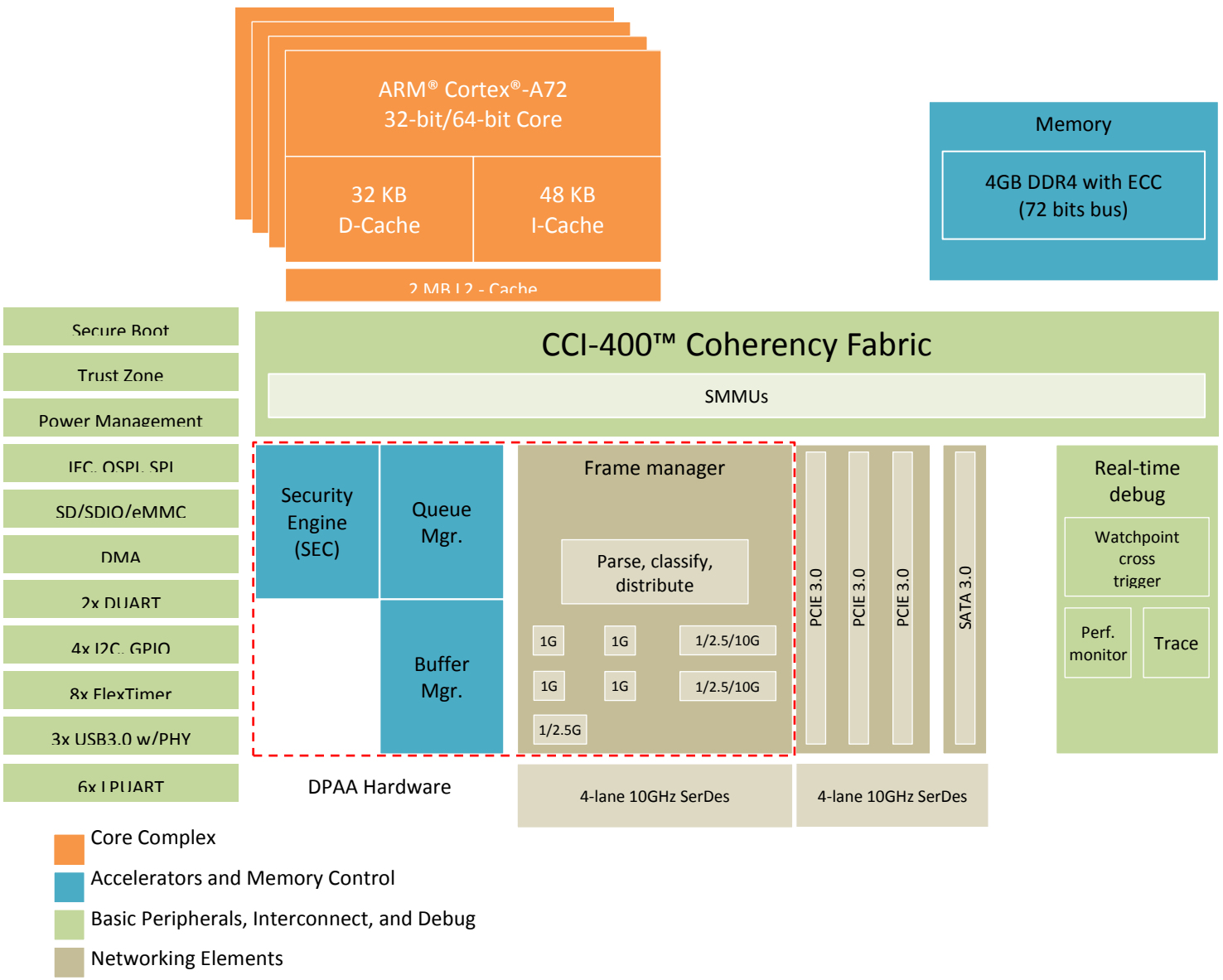
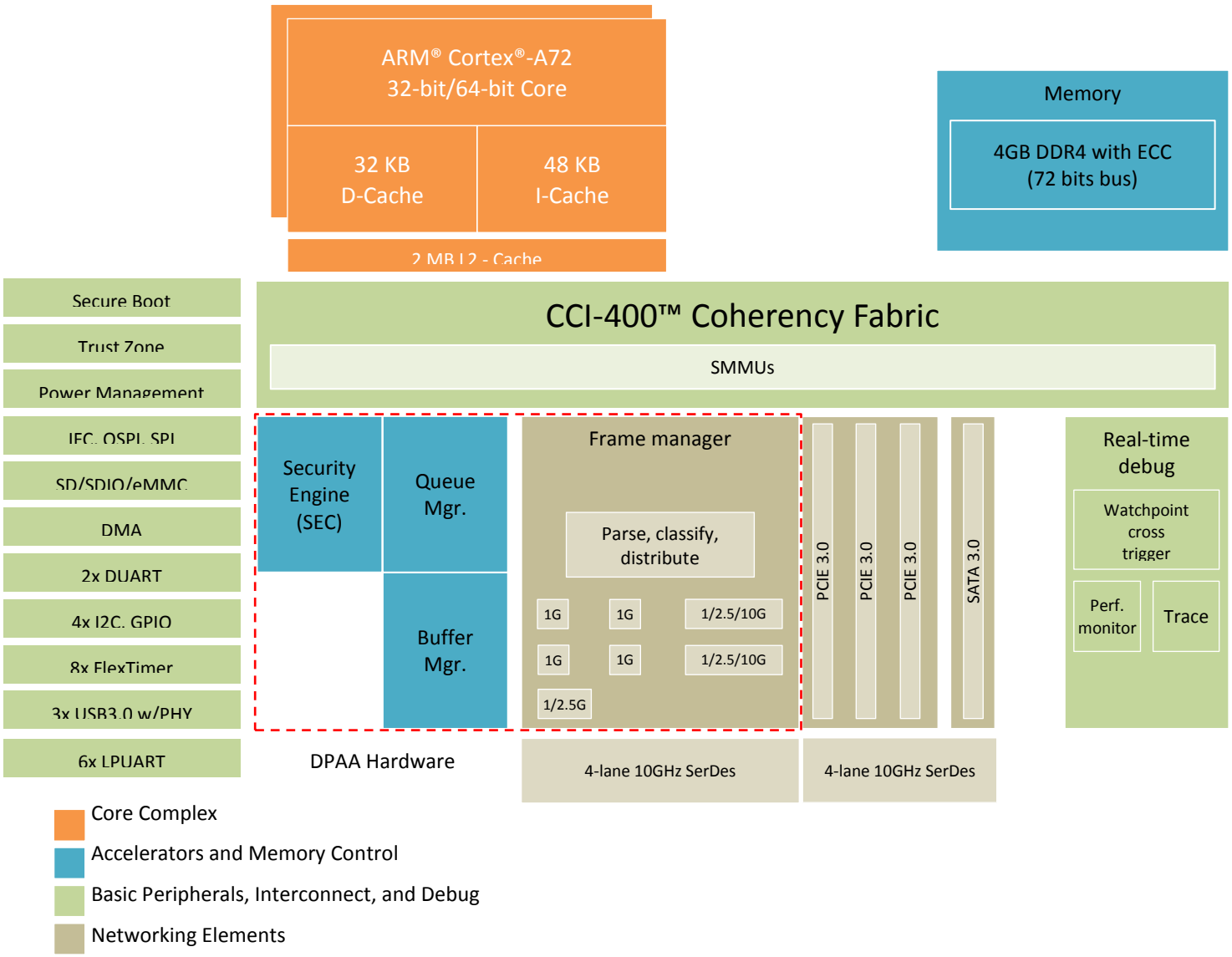


Figure 2. QLS1026A block diagram

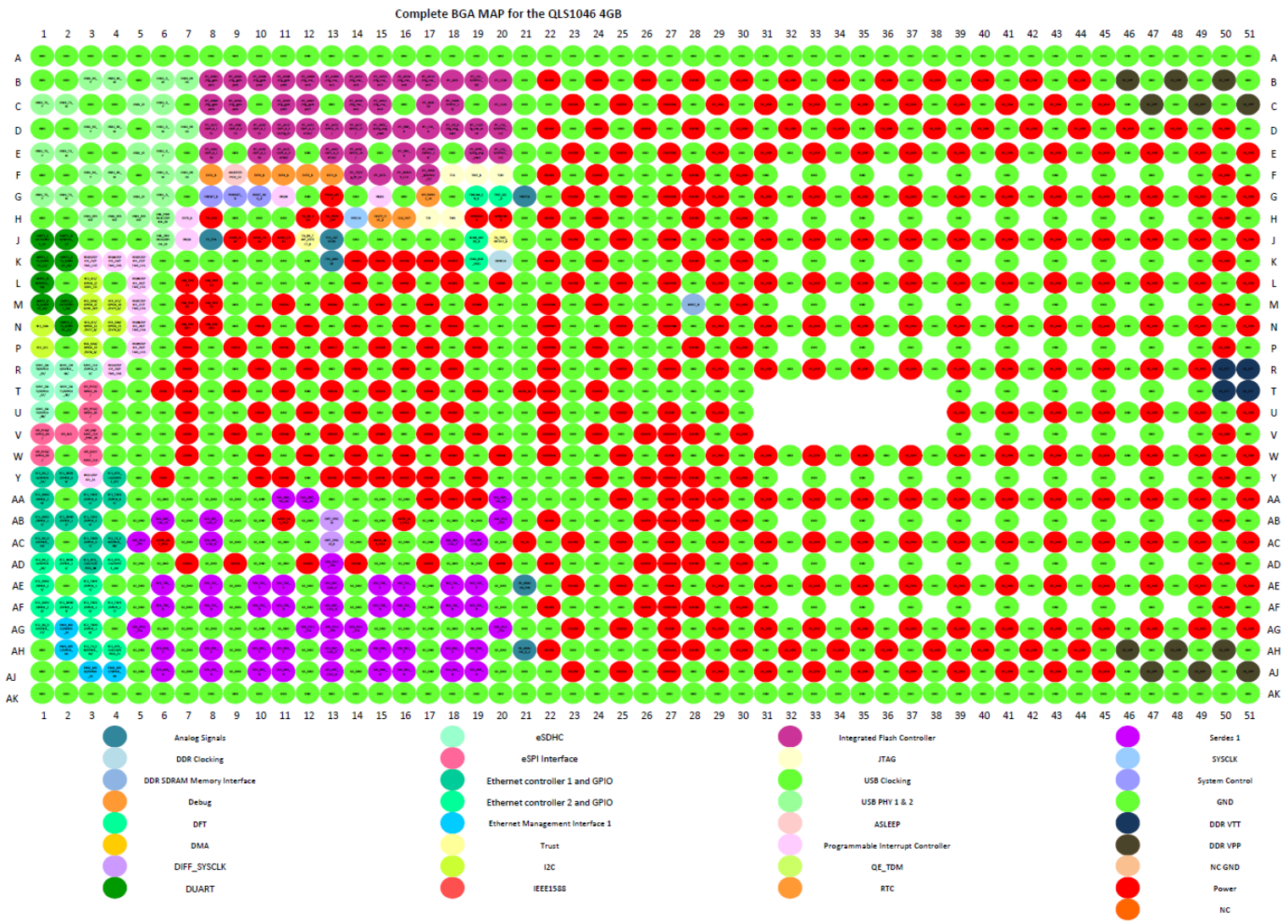


2 PIN ASSIGNMENTS

2.1 1415 BGA ball layout diagrams

This figure shows the complete view of the QLS1046A BGA ball map diagram. Figure 4, Figure 5, Figure 6, and Figure 7 show quadrant views.

Figure 3. Complete BGA Map for the QLS1046A



3 PACKAGE INFORMATION

3.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array.

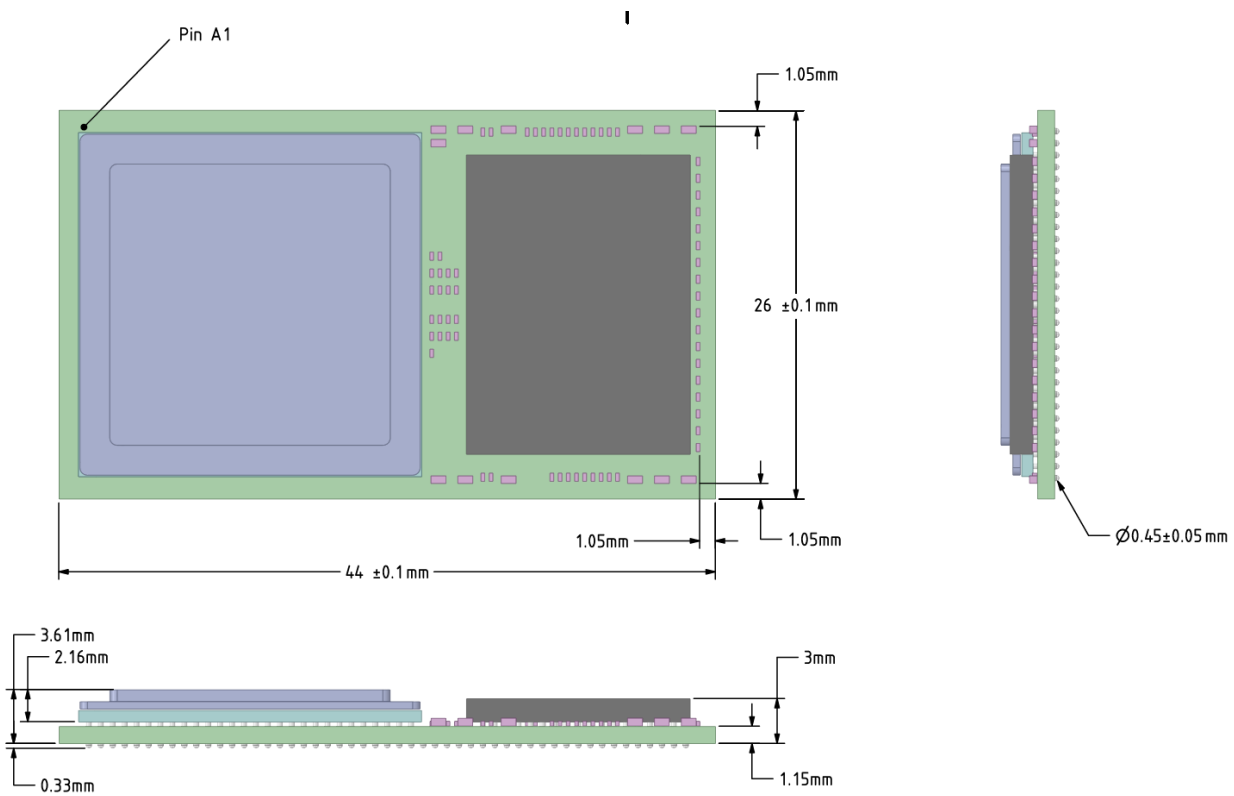
- Package outline - 26 mm x 44 mm
- Interconnects - 1415
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, and 0.5% Cu – C5 Pb free
- Solder Balls Composition - 63% Sn, 37% Pb – C5 leaded
- Module height 3.67 (typical)

3.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Figure 4. Mechanical dimensions of the FC-PBGA

1. Mechanical dimensions of the FC-PBGA – C5 Pb free



1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.

4 ORDERING INFORMATION

This table provides the TELEDYNE-E2V QorIQ platform part numbering nomenclature.

Part numbering nomenclature

Generation	Performance Level	Number of Virtual cores	Unique ID	Core Type	Temperature Range	Encryption	Package Type	CPU Speed (3)	DDR Data Rate	DDR Size	Memory Type	Product Revision
QLS(X) (2) = Layer scape	1	04 = four cores 02 = two cores	6	A = Arm	A = Automotive -40°C – 105°C F = -40°C – 125°C M = Military -55°C – 125°C	E = Encryption N = Non-Encryption	3 = FCPBGA with bottom solder spheres leaded 8 = FCPBGA All Pbfree	M = 1200 MHz P = 1400 MHz Q = 1600 MHz T = 1800 MHz	Q = 1600 MHz 1 = 2100 MHz	4 = 4GB	4 = DDR4	A = Rev 1.0

Notes:

1. For availability of the different versions, contact your local e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.
3. For the QLS1046A and QLS1026A family of devices, parts marked with "M" CPU speed require 0.9 V operating voltage .

5 REVISION HISTORY

This table summarizes revisions to this document.

Issue	Date	Comments
A	August 2018	Initial revision

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