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Peregrine Semiconductor

Product Specification

PE9763

Radiation Tolerant UltraCMOS® Delta-Sigma Modulated Fractional-N Frequency Synthesizer for Low Phase Noise Applications

OBSOLETE No longer available

Product Description

Peregrine's PE9763 is a high performance fractional-N PLL capable of frequency synthesis up to 3.2 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with the existing commercial space PLLs.

The PE9763 features a 10/11 dual modulus prescaler, counters, a delta sigma modulator, a phase comparator and a charge pump as shown in *Figure 1*. Counter values are programmable through either a serial interface or directly hard-wired.

The PE9763 is optimized for commercial space applications. Single event latch-up (SEL) is physically impossible and single event upset (SEU) is better than 10^{-9} errors per bit/day. Fabricated in Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Features

- 3.2 GHz operation
- ÷10/11 dual modulus prescaler
- Selectable phase detector or charge pump output
- Serial or Direct mode access
- Frequency selectivity: Comparison frequency/2^{18}
- Low power: 25–30 mA @ 3V (phase detector/charge pump)
- Radiation tolerant
- 100 kRad(Si) total dose
- Ultra-low phase noise
- 68-lead CQFJ or Die

Figure 1. Block Diagram

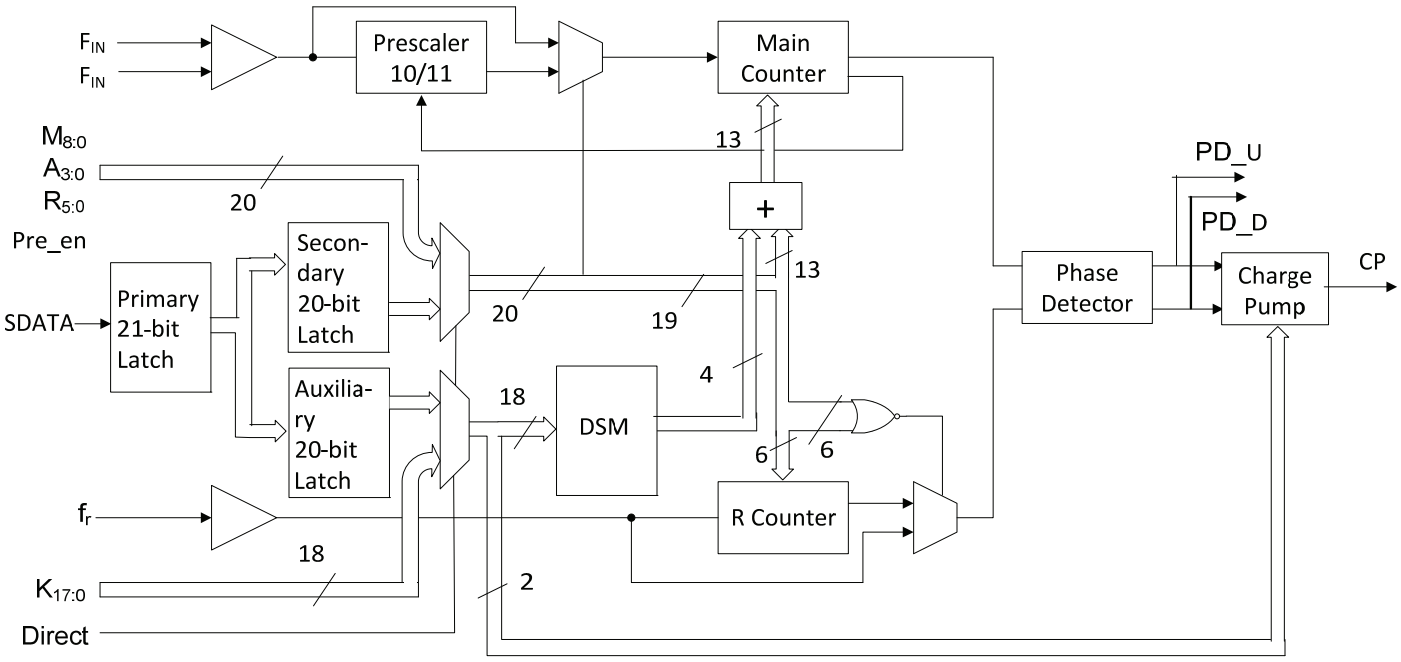


Figure 2. Pin Configuration (Top View)

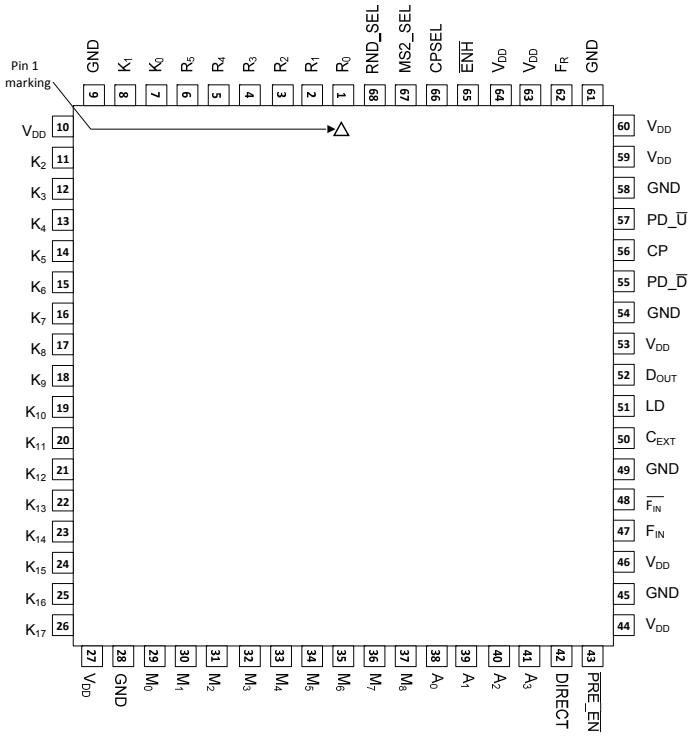


Figure 3. Package Type
68-lead CQFJ

Table 1. Pin Descriptions

Pin #	Pin Name	Valid Mode	Type	Description
1	R_0	Direct	Input	R counter bit0 (LSB).
2	R_1	Direct	Input	R counter bit1.
3	R_2	Direct	Input	R counter bit2.
4	R_3	Direct	Input	R counter bit3.
5	R_4	Direct	Input	R counter bit4.
6	R_5	Direct	Input	R counter bit5 (MSB).
7	K_0	Direct	Input	K counter bit0 (LSB).
8	K_1	Direct	Input	K counter bit1.
9	GND		Downbond	Digital core ground.
	GND		Downbond	ESD ground.
10	V_{DD}		Note 1	ESD V_{DD}.
	V_{DD}		Note 1	Digital core V_{DD}.
11	K_2	Direct	Input	K counter bit2.
12	K_3	Direct	Input	K counter bit3.
13	K_4	Direct	Input	K counter bit4.
14	K_5	Direct	Input	K counter bit5.
15	K_6	Direct	Input	K counter bit6.

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
16	K_7	Direct	Input	K counter bit7.
17	K_8	Direct	Input	K counter bit8.
18	K_9	Direct	Input	K counter bit9.
19	K_{10}	Direct	Input	K counter bit10.
20	K_{11}	Direct	Input	K counter bit11.
21	K_{12}	Direct	Input	K counter bit12.
22	K_{13}	Direct	Input	K counter bit13.
23	K_{14}	Direct	Input	K counter bit14.
24	K_{15}	Direct	Input	K counter bit15.
25	K_{16}	Direct	Input	K counter bit16.
26	K_{17}	Direct	Input	K counter bit17 (MSB).
27	V_{DD}		Note 1	Digital core V_{DD}.
	V_{DD}		Note 1	ESD V_{DD}.
28	GND		Downbond	Digital core ground.
	GND		Downbond	ESD ground.
29	M_0	Direct	Input	M counter bit0 (LSB).
30	M_1	Direct	Input	M counter bit1.
31	M_2	Direct	Input	M counter bit2
32	M_3	Direct	Input	M counter bit3.
33	M_4	Direct	Input	M counter bit4.
	S_WR	Serial	Input	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data are transferred to the secondary register on S_WR or Hop_WR rising edge.
34	M_5	Direct	Input	M Counter bit5.
	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first.
35	M_6	Direct	Input	M counter bit6.
	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 20-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
36	M_7	Direct	Input	M counter bit7.
37	M_8	Direct	Input	M counter bit8 (MSB).
38	A_0	Direct	Input	A counter bit0 (LSB).
39	A_1	Direct	Input	A counter bit1.
	E_WR	Serial	Input	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
40	A_2	Direct	Input	A counter bit2.
41	A_3	Direct	Input	A counter bit3 (MSB).
42	DIRECT	Both	Input	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
43	$\overline{\text{PRE\_EN}}$	Direct	Input	Prescaler enable, active “low”. When “high”, F_{IN} bypasses the prescaler.
44	V_{DD}		Note 1	Digital core V_{DD}.
45	GND		Downbond	Digital core ground.
	GND		Downbond	ESD ground.

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
46	V_{DD}		Note 1	ESD V_{DD}.
	V_{DD}		Note 1	Prescaler V_{DD}.
47	F_{IN}	Both	Input	Prescaler input from the VCO. 3.2 GHz max frequency.
48	$\overline{F}_{IN}$	Both	Input	Prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor directly to the ground plane.
49	GND		Downbond	Prescaler ground.
	GND		Downbond	Prescaler ground.
	GND		Downbond	Output driver/charge pump ground.
50	C_{EXT}	Both	Output	Logical "NAND" of PD_$\overline{U}$ and PD_$\overline{D}$ terminated through an on chip, 2 kΩ series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Both	Output	Lock detect and open drain logical inversion of C_{EXT}. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0").
52	D_{OUT}	Both	Output	Data out function, enabled in enhancement mode.
53	V_{DD}		Note 1	Output driver/charge pump V_{DD}.
54	GND		Downbond	Output driver/charge pump ground.
55	PD_$\overline{D}$	Both	Output	PD_$\overline{D}$ pulses down when f_p leads f_c. PD_$\overline{U}$ is driven to GND when CPSEL = "High".
56	CP	Both	Output	Charge pump output. Selected when CPSEL = "1". Tristate when CPSEL = "Low".
57	PD_$\overline{U}$	Both	Output	PD_$\overline{U}$ pulses down when f_c leads f_p. PD_$\overline{D}$ is driven to GND when CPSEL = "High".
58	GND		Downbond	Output driver/charge pump ground.
59	V_{DD}		Note 1	Output driver/charge pump V_{DD}.
	GND		Downbond	Phase detector GND.
60	V_{DD}		Note 1	Phase detector V_{DD}.
	V_{DD}		Note 1	ESD V_{DD}.
61	GND		Downbond	ESD ground.
	GND		Downbond	Reference ground.
62	f_r	Both	Input	Reference frequency input.
63	V_{DD}		Note 1	Reference V_{DD}.
64	V_{DD}		Note 1	Digital core V_{DD}.
	GND		Downbond	Digital core ground.
65	$\overline{ENH}$	Both	Input	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
66	CPSEL	Both	Input	Charge pump select. "High" enables the charge pump and disables pins PD_$\overline{U}$ and PD_$\overline{D}$ by forcing them "low". A "low" Tri-states the CP and enables PD_$\overline{U}$ and PD_$\overline{D}$.
67	MS2_SEL	Both	Input	MASH 1-1 select. "High" selects MASH 1-1 mode. "Low" selects the MASH 1-1-1 mode.
68	RND_SEL	Both	Input	K register LSB toggle enable. "1" enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency / 2^{19}.

Notes: 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	–0.3	4.0	V
V_I	Voltage on any input	–0.3	V_{DD} + 0.3	V
I_I	DC into any input	–10	+10	mA
I_O	DC into any output	–10	+10	mA
θ_{JC}	Theta JC		12	°C/W
T_j	Junction temperature maximum		+125	°C
T_{STG}	Storage temperature range	–65	+150	°C

Table 3. Operating Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.85	3.15	V
T_A	Operating ambient temperature range	–40	+85	°C

Exceeding absolute maximum ratings may cause permanent device damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating ranges maximum and absolute maximum for extended periods may reduce reliability.

Table 4. ESD Ratings

Symbol	Parameter/Condition	Level	Unit
V_{ESD}	ESD voltage human body model, HBM*	1000	V

Note: * Periodically sampled, not 100% tested. Tested per MIL–STD 883 M3015 C2.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 4*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

Table 5. DC Characteristics @ V_{DD} = 3.0V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current; Prescaler enabled, charge pump disabled	V_{DD} = 2.85–3.15 V		25	35	mA
I_{DD}	Operational supply current; Prescaler enabled, charge pump enabled	V_{DD} = 2.85–3.15 V		20	30	mA
I_{DD}	Operational supply current; Prescaler disabled, charge pump disabled	V_{DD} = 2.85–3.15 V		10	17	mA
I_{DD}	Operational supply current; Prescaler disabled, charge pump enabled	V_{DD} = 2.85–3.15 V		15	25	mA
All digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], DIRECT, $\overline{\text{PRE\_EN}}$, RND_SEL, MS_SEL, CPSEL, $\overline{\text{ENH}}$ (contains a 70 kΩ pull-down resistor)						
V_{IH}	High level input voltage	V_{DD} = 2.85–3.15V	0.7 × V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.85–3.15V			0.3 × V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 3.15V			+100	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 3.15V	–1			µA
Reference divider input: f_r						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 3.15V			+100	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 3.15V	–100			µA
Counter and phase detector outputs: PD_$\overline{\text{D}}$, PD_$\overline{\text{U}}$						
V_{OLD}	Output voltage LOW	I_{OUT} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{OUT} = –3 mA	V_{DD} – 0.4			V
Digital test outputs: D_{OUT}						
V_{OLD}	Output voltage LOW	I_{OUT} = 200 µA			0.4	V
V_{OHD}	Output voltage HIGH	I_{OUT} = –200 µA	V_{DD} – 0.4			V
Charge pump output: CP						
I_{CP} – Source	Drive current	V_{CP} = V_{DD} / 2	–2.6	2	–1.4	mA
I_{CP} – Sink	Drive current	V_{CP} = V_{DD} / 2	1.4	2	2.6	mA
I_{CPL}	Leakage current	1.0V < V_{CP} < V_{DD} – 1.0V	–1		1	µA
I_{CP} – Source vs. I_{CP} – Sink	Sink vs source mismatch	V_{CP} = V_{DD} / 2 T_A = +25 °C			25	%
I_{CP} vs V_{CP}	Output current magnitude variation vs voltage	1.0V < V_{CP} < V_{DD} – 1.0V T_A = 25 °C			15	%
Lock detect outputs: (C_{EXT}, LD)						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{OUT} = 0.1 mA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{OUT} = –0.1 mA	V_{DD} – 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{OUT} = 1 mA			0.4	V

Table 6. AC Characteristics @ V_{DD} = 3.0V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see *Figure 3* and *Figure 4*)						
f_{CLK}	Serial data clock frequency	(Note 1)			10	MHz
t_{CLKH}	Serial clock HIGH time		30			ns
t_{CLKL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time to SCLK rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLk rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
Main divider (including prescaler)						
F_{IN}	Operating frequency		275		3200	MHz
P_{F_IN}	Input level range	External AC coupling	–5		5	dBm
Main divider (prescaler bypassed)						
F_{IN}	Operating frequency		50		300	MHz
P_{F_IN}	Input level range	External AC coupling	-5		5	dBm
Reference divider						
f_r	Operating frequency	(Note 3)			100	MHz
P_{fr}	Reference input power (Note 2)	Single ended input	–2			dBm
Phase detector						
f_c	Comparison frequency	(Note 3)			50	MHz
SSB phase noise (F_{IN} = 1.9 GHz, f_r = 20 MHz, f_c = 10 MHz, LBW = 50 kHz, V_{DD} = 3.0V, Temp = +25 °C)						
Φ_N	Phase noise	1 kHz Offset		–88	–80	dBc/Hz
Φ_N	Phase noise	10 kHz Offset		–92	–85	dBc/Hz

Notes: 1. f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{CLK} specification.
2. CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 V_{PP}. For optimum phase noise performance, the reference input falling edge rate should be faster than 80 mV/ns.
3. Parameter is guaranteed through characterization only and is not tested.

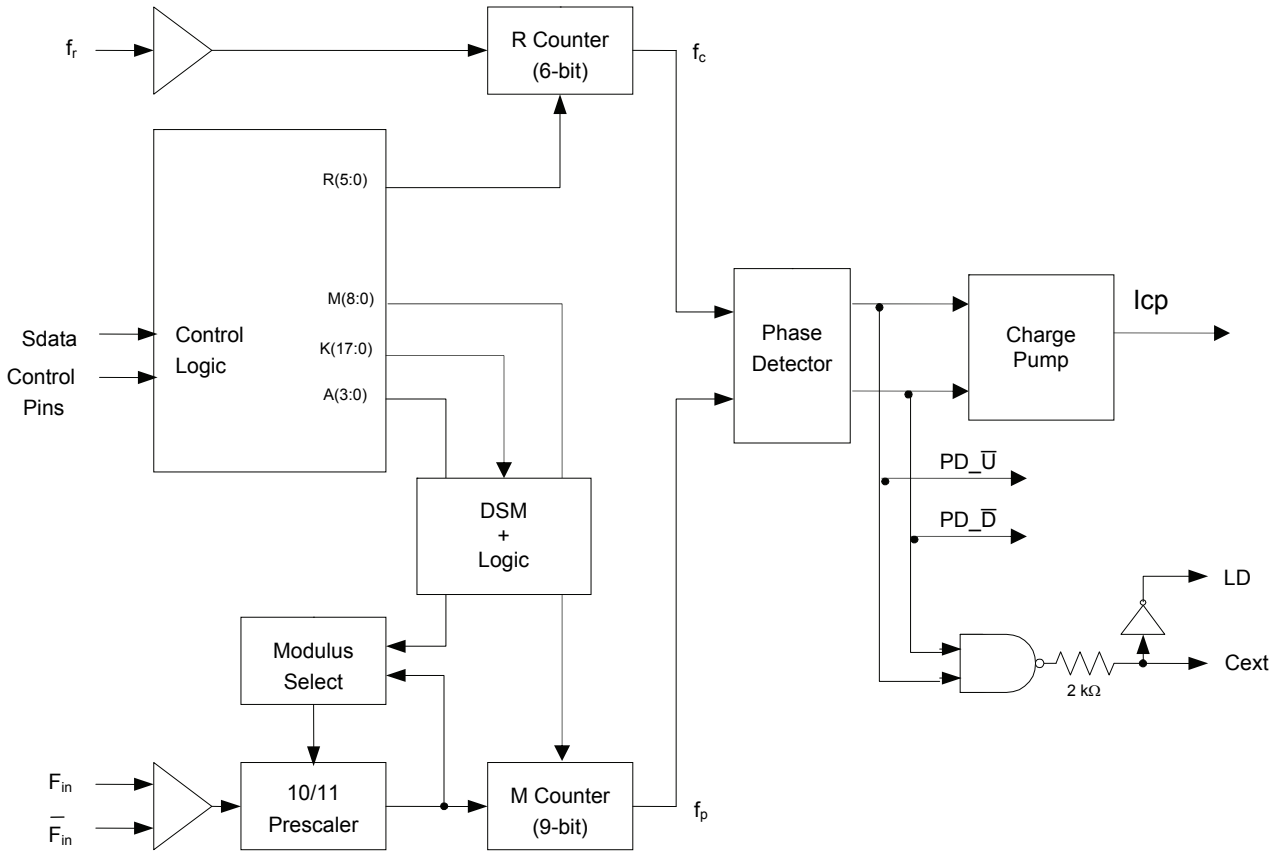
Functional Description

The PE9763 consists of counters, a prescaler, an 18-bit delta-sigma modulator (DSM), a phase detector and a charge pump. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic.

The DSM modulates the “A” counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. These signals can be configured to drive a tri-state charge pump. Data is written into the internal registers via the three-wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 4. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

Setting the PRE_EN control bit "low" enables the ÷10/11 prescaler. The main counter chain then divides the RF input frequency (F_{IN}) by an integer or fractional number derived from the values in the "M", "A" counters and the DSM input word K. The accumulator size is 18 bit, so the fractional value is fixed from the ratio $K/2^{18}$. There is an additional bit in the DSM that acts like an extra bit (19^{th} bit). This bit is enabled by asserting the pin RND_SEL to "high". Enabling this bit has the benefit of reducing the spurious levels. However, a small frequency offset will occur. This positive frequency offset is calculated with the following equation.

$$f_{offset} = [F_R / (R+1)] / 2^{19} \quad (1)$$

All of the following equations do not take into account of this frequency offset. If this offset is important to a specific frequency plan, appropriate account needs to be taken.

In the normal mode, the output from the main counter chain (F_R) is related to the VCO frequency (F_{IN}) by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A + K/2^{18}] \quad (2)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{in} = [10 \times (M+1) + A + K/2^{18}] \times [F_R / (R+1)] \quad (3)$$

where $A \leq M + 1$, $1 \leq M \leq 511$

A consequence of the upper limit on A is that F_{IN} must be greater than or equal to 90 x [F_R / (R+1)] to obtain contiguous channels. The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M.

Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode (*)

Setting the frequency control register bit PRE_EN "high" allows F_{IN} to bypass the ÷10/11 prescaler.

In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{IN} to the reference frequency f_r:

$$F_{IN} = (M+1) \times [F_R / (R+1)] \quad (4)$$

where $1 \leq M \leq 511$

(*) Only integer mode

In frequency bypass mode, neither A counter or K counter is used. Therefore, only integer-N operation is possible.

Reference Counter

The reference counter chain divides the reference frequency F_R down to the phase detector comparison frequency f_c.

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R+1) \quad (5)$$

where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency (F_R) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is "low" and the S_WR input is "low", serial input data (SDATA input), B_0 to B_{20}, are clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The LSB is used as address bit. When "0", the contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in *Figure 4*. When "1", data is transferred to the auxiliary register according to the same timing dia-gram. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in *Table 8* on page 10.

While the E_WR input is “high” and the S_WR input is “low”, serial input data (SDATA input), B_0 to B_7, are clocked serially into the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR ac-cording to the timing diagram shown in *Figure 4*. After the falling edge of E_WR, the data provide control bits as shown in *Table 9* on page 10 will have their bit functionality enabled by asserting the $\overline{ENH}$ input “low”.

Direct Interface Mode

Direct Interface Mode is selected by setting the “Direct” input “high”.

Counter control bits are set directly at the pins as shown in *Table 7* and *Table 8*.

Table 7. Secondary Register Programming

Interface Mode	$\overline{ENH}$	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	Addr
Direct	1	R_5	R_4	M_8	M_7	$\overline{PRE\_EN}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	0

Note: * Serial data clocked serially on SCLK rising edge while E_WR “low” and captured in secondary register on S_WR rising edge.

MSB (first in) … (last in) LSB

Table 8. Auxiliary Register Programming

Interface Mode	$\overline{ENH}$	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	Rsrv	Rsrv	Addr
Direct	1	K_{17}	K_{16}	K_{15}	K_{14}	K_{13}	K_{12}	K_{11}	K_{10}	K_9	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0	X	X	X
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	1

Note: * Serial data clocked serially on SCLK rising edge while E_WR “low” and captured in auxiliary register on S_WR rising edge.

MSB (first in) … (last in) LSB

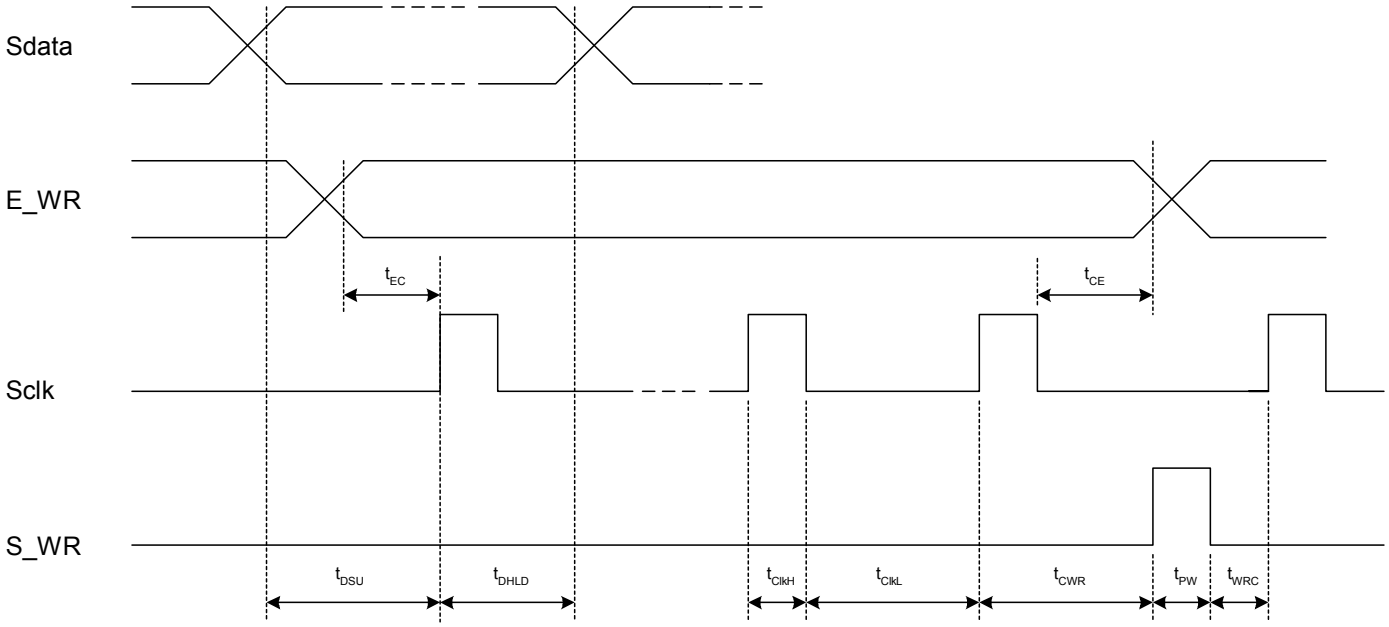
Table 9. Enhancement Register Programming

Interface Mode	$\overline{ENH}$	Reserved	Reserved	f_p output	Power Down	Counter Load	MSEL Output	f_c output	LD Disable
Serial*	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Note: * Serial data clocked serially on SCLK rising edge while E_WR “high” and captured in the double buffer on E_WR falling edge.

MSB (first in) … (last in) LSB

Figure 5. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the reference counter output onto the D_{OUT} output.
Bit 7	LD disable	Disables the LD pin for quieter operation.

Note: * Program to 0.

Phase Detector and Charge Pump

The phase detector is triggered by rising edges from the main counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_D pulses “low”. If the divided reference leads the di-vided VCO in phase or frequency (f_c leads f_p), PD_U pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c.

For the UP and DOWN mode, PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to $V_{DD}/2\ \pi$.

PD_U pulses cause an increase in VCO frequency and PD_D pulses cause a decrease in VCO frequency, for a positive kV VCO.

For the charge pump mode, the phase detector outputs are used internally to drive a tri-state charge pump. However, the PD_U, and PD_D output pins will be drive statically to GND. The charge pump will drive a fixed 2 mA of current.

A lock detect output, LD is also provided, via the pin C_{EXT}. C_{EXT} is the logical “NAND” of PD_U and PD_D waveforms, which is driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides low pass filtering of this signal. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_U and PD_D.

Figure 6. Typical Phase Noise

A typical phase noise plot is shown below. Phase noise results for “Trace 2” is the average values.

Test Conditions: F_{OUT} = 1.9202 GHz, Fcomparison = 20 MHz, MASH 1-1, V_{DD} = 3V, Temp = +25 °C, Loop bandwidth = 80 kHz.

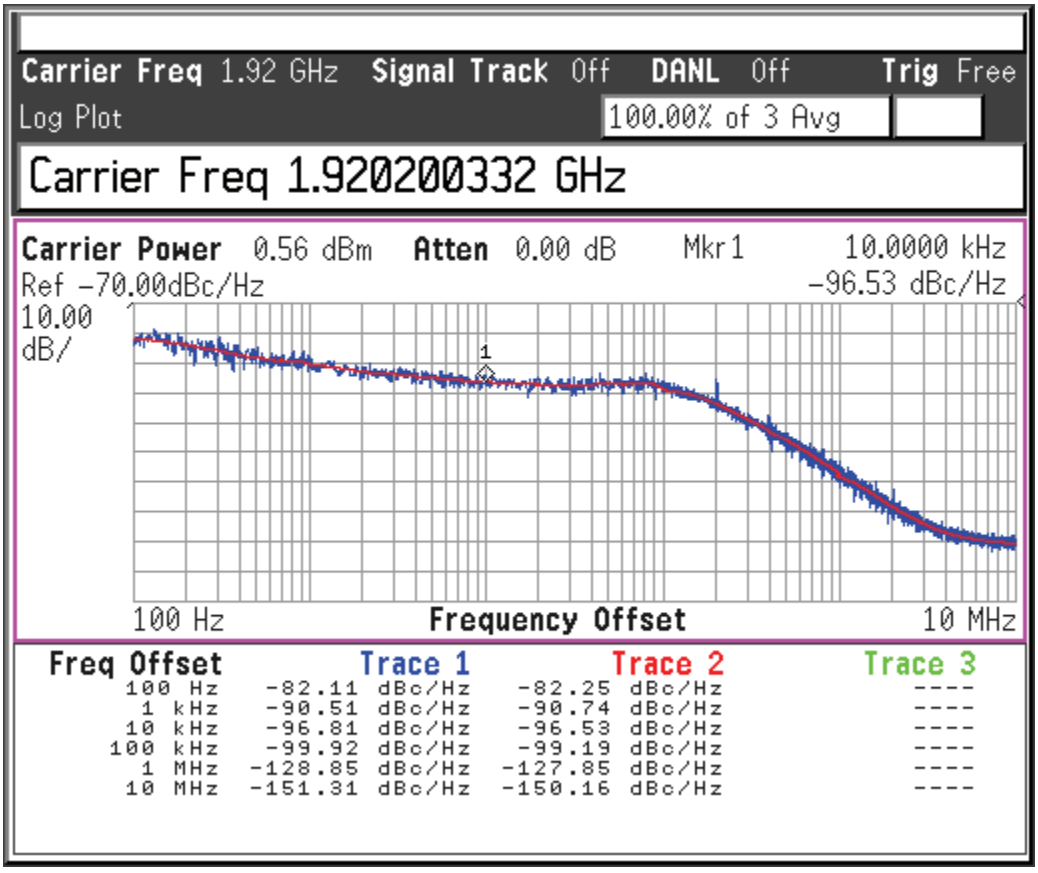


Figure 7. Typical Spurious Plot

Test Conditions: Frequency step = 200 kHz, Loop bandwidth = 80 kHz, F_{OUT} = 1.9202 GHz, Fcomparison = 20 MHz, MASH 1-1, V_{DD} = 3V, Temp = +25 °C.

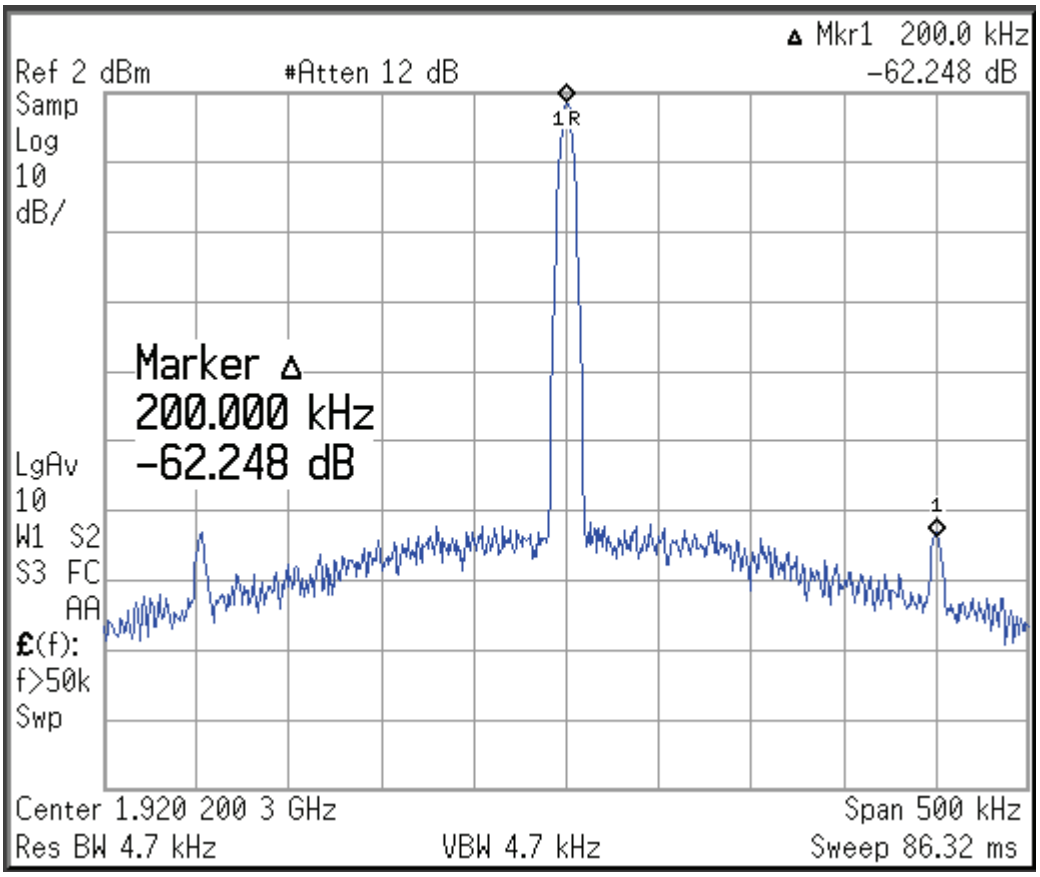
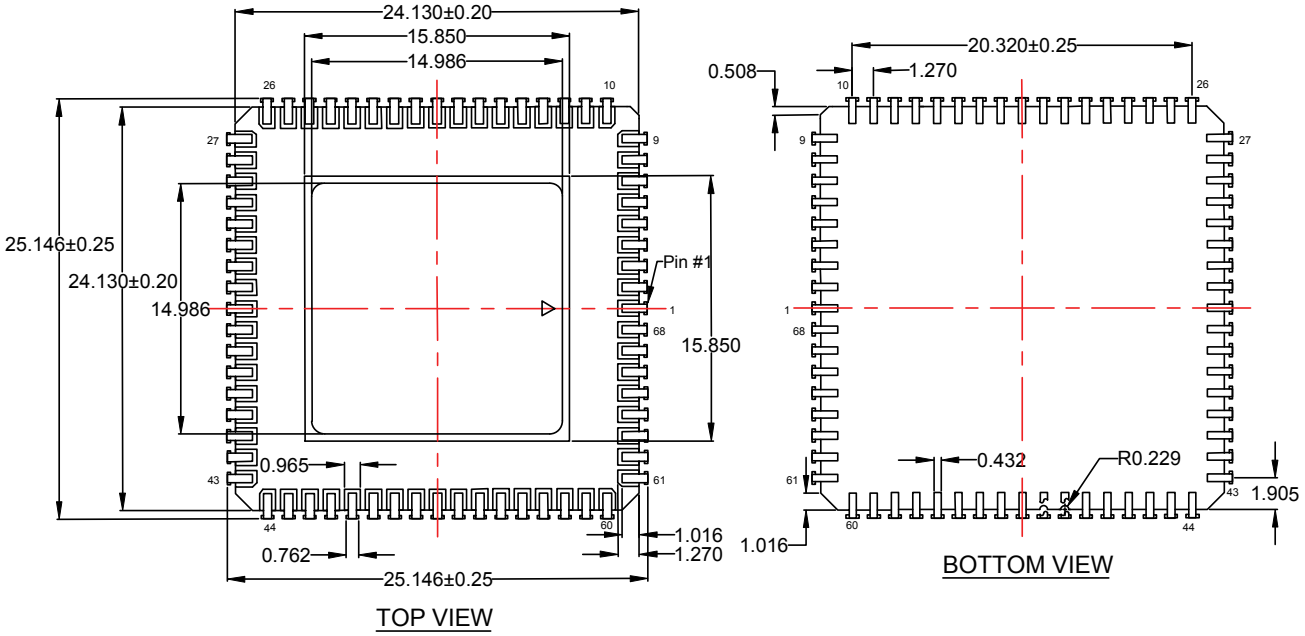
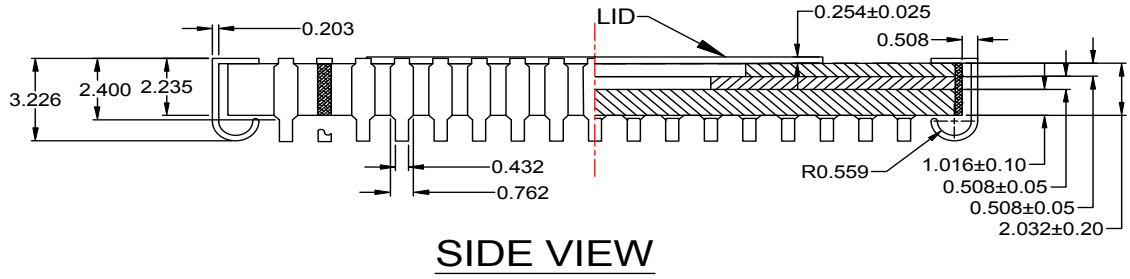
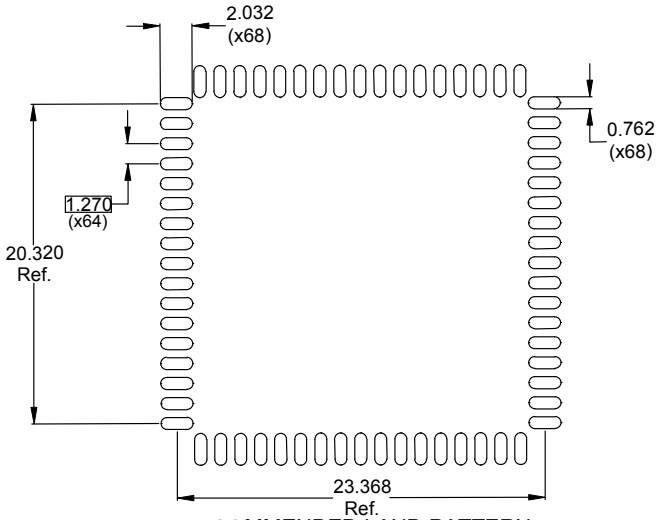


Figure 8. Package Drawing (dimensions in millimeters)
68-lead CQFJ





SIDE VIEW



RECOMMENDED LAND PATTERN

DOC-59989

Figure 9. Top Marking Specifications

Not to scale PRT-50193

Line 1: Pin 1 indicator △, e2v and Peregrine logo
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside marking on any of the Peregrine products.

Table 11. Ordering Information

Order Code	Description	Packaging	Shipping Method
9763-01*	PE9763 Engineering samples	68-lead CQFJ	21 / Tray
9763-11	PE9763 Flight units	68-lead CQFJ	21 / Tray
9763-00	PE9763 Evaluation kit	Evaluation kit	1 / Box

Note: * The PE9763-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE9763-11 flight units. The PE9763-01 device provides the same functionality and footprint as the PE9763-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ http://www.teledyne-e2v.com ~ inquiries@e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice. ***Preliminary Specification:*** The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).