

Product Specification

PE97632

OBSOLETE No longer available

Product Description

Peregrine's PE97632 is a radiation tolerant, high performance fractional-N PLL capable of frequency synthesis up to 3.5 GHz. The device is designed for commercial space use and optimized for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97632 features a $\div 10/11$ dual modulus prescaler, counters, a delta sigma modulator and a phase comparator as shown in *Figure 1*. Counter values are programmable through a serial or direct hardwired mode.

The PE97632 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Radiation Tolerant UltraCMOS® Delta-Sigma Modulated Fractional-N Frequency Synthesizer for Low Phase Noise Applications

Features

- 3.5 GHz operation
- $\div 10/11$ dual modulus prescaler
- Phase detector output
- Serial or direct hardwired mode
- Frequency selectivity: comparison frequency / 2^{18}
- Low power: 40 mA a@ 3.3V
- Phase noise figure of merit: -216 dBc/Hz
- 100 kRad (Si) total dose
- 68-lead CQFJ
- Pin compatible with the PE9763 (reference application note AN24 at www.psemi.com)

Figure 1. Block Diagram

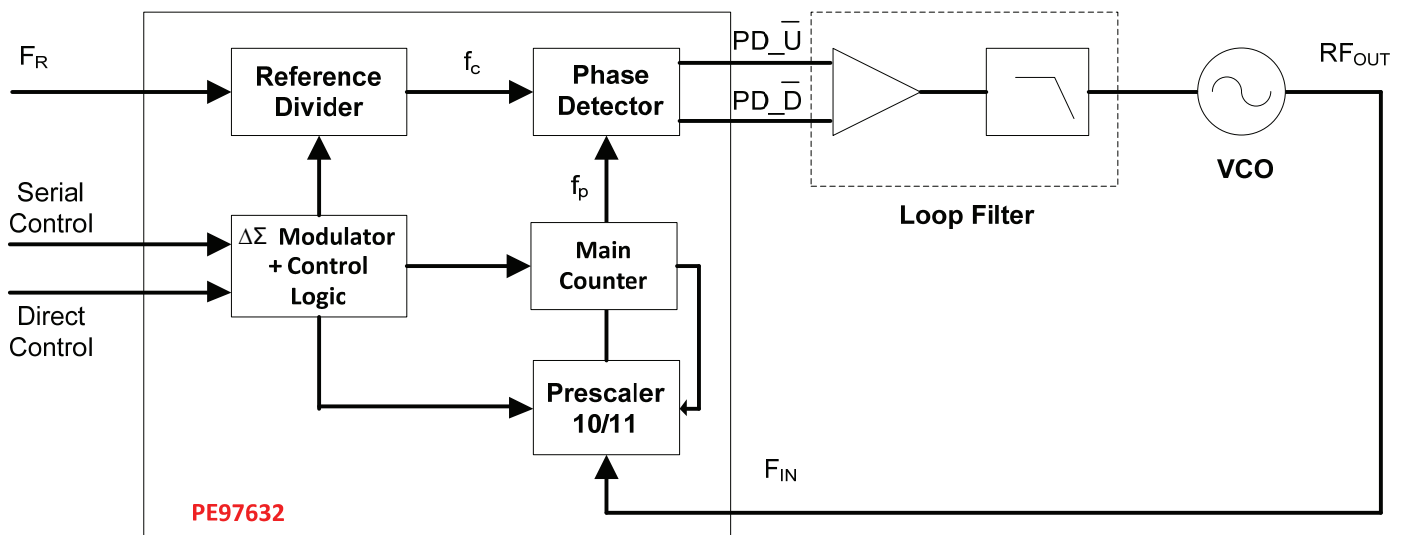


Figure 2. Pin Configuration (Top View)

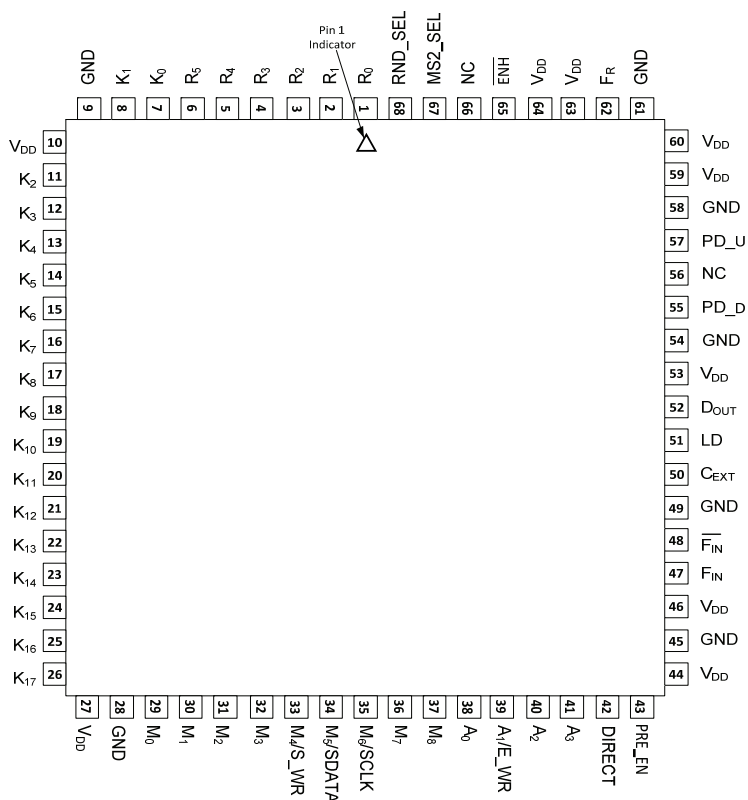


Figure 3. Package Type
68-lead CQFJ

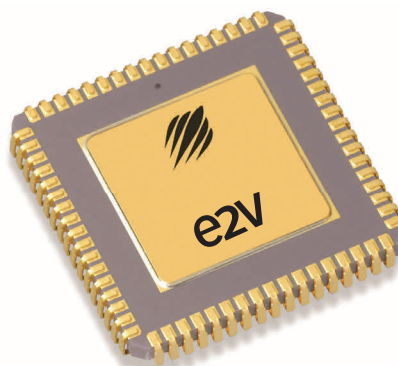


Table 1. Pin Descriptions

Pin #	Pin Name	Valid Mode	Type	Description
1	R ₀	Direct	Note 2	R counter bit0 (LSB)
2	R ₁	Direct	Note 2	R counter bit1
3	R ₂	Direct	Note 2	R counter bit2
4	R ₃	Direct	Note 2	R counter bit3
5	R ₄	Direct	Note 2	R counter bit4
6	R ₅	Direct	Note 2	R counter bit5 (MSB)
7	K ₀	Direct	Note 2	K counter bit0 (LSB)
8	K ₁	Direct	Note 2	K counter bit1
9	GND		Downbond	Ground
10	V _{DD}		Note 1	Digital core V _{DD}
11	K ₂	Direct	Note 2	K counter bit2
12	K ₃	Direct	Note 2	K counter bit3
13	K ₄	Direct	Note 2	K counter bit4
14	K ₅	Direct	Note 2	K counter bit5
15	K ₆	Direct	Note 2	K counter bit6

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
16	K ₇	Direct	Note 2	K counter bit7
17	K ₈	Direct	Note 2	K counter bit8
18	K ₉	Direct	Note 2	K counter bit9
19	K ₁₀	Direct	Note 2	K counter bit10
20	K ₁₁	Direct	Note 2	K counter bit11
21	K ₁₂	Direct	Note 2	K counter bit12
22	K ₁₃	Direct	Note 2	K counter bit13
23	K ₁₄	Direct	Note 2	K counter bit14
24	K ₁₅	Direct	Note 2	K counter bit15
25	K ₁₆	Direct	Note 2	K counter bit16
26	K ₁₇	Direct	Note 2	K counter bit17 (MSB)
27	V _{DD}		Note 1	Digital core V _{DD}
28	GND		Downbond	Ground
29	M ₀	Direct	Note 2	M counter bit0 (LSB)
30	M ₁	Direct	Note 2	M counter bit1
31	M ₂	Direct	Note 2	M counter bit2
32	M ₃	Direct	Note 2	M counter bit3
33	M ₄	Direct	Note 2	M counter bit4
	S_WR	Serial	Note 2	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data are transferred to the secondary register on S_WR rising edge.
34	M ₅	Direct	Note 2	M counter bit5
	SDATA	Serial	Note 2	Binary serial data input. Input data entered MSB first.
35	M ₆	Direct	Note 2	M counter bit6
	SCLK	Serial	Note 2	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
36	M ₇	Direct	Note 2	M counter bit7
37	M ₈	Direct	Note 2	M counter bit8 (MSB)
38	A ₀	Direct	Note 2	A counter bit0 (LSB)
39	A ₁	Direct	Note 2	A counter bit1
	E_WR	Serial	Note 2	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
40	A ₂	Direct	Note 2	A counter bit2
41	A ₃	Direct	Note 2	A counter bit3 (MSB)
42	DIRECT	Both	Note 2	Direct mode select. “High” enables direct mode. “Low” enables serial mode.
43	PRE_EN	Direct	Note 2	Prescaler enable, active “low”. When “high”, F _{IN} bypasses the prescaler.
44	V _{DD}		Note 1	Digital core V _{DD}
45	GND		Downbond	Ground

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Valid Mode	Type	Description
46	V _{DD}		Note 1	Prescaler V _{DD}
47	F _{IN}	Both	Input	Prescaler input from the VCO, 3.5 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and terminated with a 50Ω resistor to ground.
48	$\overline{F}_{IN}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.
49	GND		Downbond	Ground
50	C _{EXT}	Both	Output	Logical "NAND" of PD _U and PD _D terminated through an on chip, 2 kΩ series resistor. Connecting C _{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
51	LD	Both	Output	Lock detect and open drain logical inversion of C _{EXT} . When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0").
52	D _{OUT}	Both	Output	Data out function, enabled in enhancement mode.
53	V _{DD}		Note 1	Output driver/V _{DD}
54	GND		Downbond	Ground
55	PD _D	Both	Output	PD _D pulses down when f _p leads f _c .
56	NC	Both	Note 3	No connect
57	PD _U	Both	Output	PD _U pulses down when f _c leads f _p .
58	GND		Downbond	Ground
59	V _{DD}		Note 1	Output driver/V _{DD}
60	V _{DD}		Note 1	Phase detector V _{DD}
61	GND		Downbond	Ground
62	F _R	Both	Input	Reference frequency input
63	V _{DD}		Note 1	Reference V _{DD}
64	V _{DD}		Note 1	Digital core V _{DD}
	GND		Downbond	Ground
65	$\overline{ENH}$	Both	Note 2	Enhancement mode. When asserted low ("0"), enhancement register bits are functional.
66	NC	Both	Note 3	No connect
67	MS2_SEL	Both	Note 2	MASH 1-1 select. "High" selects MASH 1-1 mode. "Low" selects the MASH 1-1-1 mode.
68	RND_SEL	Both	Note 2	K register LSB toggle enable. "1" enables the toggling of LSB. This is equivalent to having an additional bit for the LSB of K register. The frequency offset as a result of enabling this bit is the phase detector comparison frequency / 2 ¹⁹ .

Notes: 1. All V_{DD} pins are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.
3. No Connect pins can be left open or floating.

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	$V_{DD} + 0.3$	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
θ_{JC}	Theta JC		12	°C/W
T_J	Junction temperature maximum		+125	°C
T_{stg}	Storage temperature range	-65	+150	°C
V_{ESD}	ESD voltage HBM ¹ All pins except pin 52		1000	V
	ESD voltage HBM ^{1,2} On pin 52		300	V

Notes: 1. Human Body Model (MIL-STD-883 Method 3015).
2. Pin 52 is a test pin only. It is not used in normal operation.

Table 3. Operating Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	-40	+85	°C

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating ranges maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in *Table 3*.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

Table 4. Single Event Effects¹

SEE Mode	Effective Linear Energy Transfer (LET) ²
SEL	90 MeV•cm ² /mg ³
SEB, SEGR, SEFI	90 MeV•cm ² /mg ³
SEU	60 MeV•cm ² /mg ⁴
SET	60 MeV•cm ² /mg ⁵

Notes: 1. Testing performed using serial programming mode.
2. Au ion/60° incidence.
3. No SEL, SEB, SEGR, SEFI observed.
4. No frequency upsets observed at LET<60.
5. Minor transients (phase errors) observed resulting in self-recovering operation without intervention.

Table 5. DC Characteristics @ $V_{DD} = 3.3V$ $-40^{\circ}C < T_A < +85^{\circ}C$, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{DD}	Operational supply current;	Prescaler enabled V _{DD} = 2.85–3.45V		40	50	mA
		Prescaler disabled V _{DD} = 2.85–3.45V		15	20	mA
All digital inputs: K[17:0], R[5:0], M[8:0], A[3:0], DIRECT, PRE_EN, RND_SEL, MS2_SEL, ENH (have a 70 kΩ pull-down resistor)						
V _{IH}	High level input voltage	V _{DD} = 2.85–3.45V	0.7 x V _{DD}			V
V _{IL}	Low level input voltage	V _{DD} = 2.85–3.45V			0.3 x V _{DD}	V
I _{IH}	High level input current	V _{IH} = V _{DD} = 3.45V			100	μA
I _{IL}	Low level input current	V _{IL} = 0, V _{DD} = 3.45V	–1			μA
Reference divider input: F _R						
I _{IHR}	High level input current	V _{IH} = V _{DD} = 3.45V			100	μA
I _{ILR}	Low level input current	V _{IL} = 0, V _{DD} = 3.45V	–100			μA
Counter and phase detector outputs: PD_D, PD_U						
V _{OLD}	Output voltage LOW	I _{OUT} = 6 mA			0.4	V
V _{OHD}	Output voltage HIGH	I _{OUT} = –3 mA	V _{DD} – 0.4			V
Digital test outputs: D _{OUT}						
V _{OLD}	Output voltage LOW	I _{OUT} = 200 μA			0.4	V
V _{OHD}	Output voltage HIGH	I _{OUT} = –200 μA	V _{DD} – 0.4			V
Lock detect outputs: (C _{EXT} , LD)						
V _{OLC}	Output voltage LOW, C _{EXT}	I _{OUT} = 0.1 mA			0.4	V
V _{OHC}	Output voltage HIGH, C _{EXT}	I _{OUT} = –0.1 mA	V _{DD} – 0.4			V
V _{OLLD}	Output voltage LOW, LD	I _{OUT} = 1 mA			0.4	V

Table 6. AC Characteristics @ $V_{DD} = 3.3V$, $-40^{\circ}C < T_A < +85^{\circ}C$, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see Figure 10)						
f _{Clk}	Serial data clock frequency ¹				10	MHz
t _{ClkH}	Serial clock HIGH time		30			ns
t _{ClkL}	Serial clock LOW time		30			ns
t _{DSU}	SDATA set-up time to SCLK rising edge		10			ns
t _{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t _{PW}	S_WR pulse width		30			ns
t _{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t _{CE}	SCLK falling edge to E_WR transition		30			ns
t _{WRC}	S_WR falling edge to SCLK rising edge		30			ns
t _{EC}	E_WR transition to SCLK rising edge		30			ns
Main divider (prescaler enabled)						
P _{Fin}	Input level range	External AC coupling 275 MHz ≤ Freq ≤ 3200 MHz	−5		5	dBm
		External AC coupling 3.2 GHz < Freq ≤ 3.5 GHz 3.15 V ≤ V _{DD} ≤ 3.45 V	0		5	dBm
Main divider (prescaler bypassed)						
F _{IN}	Operating frequency		50		300	MHz
P _{Fin}	Input level range	External AC coupling	−5		5	dBm
Reference divider						
F _R	Operating frequency ³				100	MHz
P _{FR}	Reference input power ²	Single ended input	−2		10	dBm
Phase detector						
f _c	Comparison frequency ³				50	MHz
SSB phase noise (F _{IN} = 1.9 GHz, F _R = 20 MHz, f _c = 20 MHz, LBW = 50 kHz, V _{DD} = 3.3V)						
Φ _N	Phase noise	100 Hz offset		−89	−83	dBc/Hz
Φ _N	Phase noise	1 kHz offset		−96	−91	dBc/Hz
Φ _N	Phase noise	10 kHz offset		−101	−96	dBc/Hz
SSB phase noise (F _{IN} = 1.9 GHz, F _R = 20 MHz, f _c = 20 MHz, LBW = 50 kHz, V _{DD} = 3.0V)						
Φ _N	Phase noise	100 Hz offset		−84	−70	dBc/Hz
Φ _N	Phase noise	1 kHz offset		−92	−81	dBc/Hz
Φ _N	Phase noise	10 kHz offset		−100	−89	dBc/Hz

- Notes: 1. f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{CLK} specification.
2. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For Sin wave inputs, the minimum amplitude needs to be $0.5 V_{PP}$. The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above V_{DD} or below GND. The DC voltage at the Reference input is $V_{DD}/2$.
3. Parameter is guaranteed through characterization only and is not tested.

Figure 4. Typical Spurious Plot

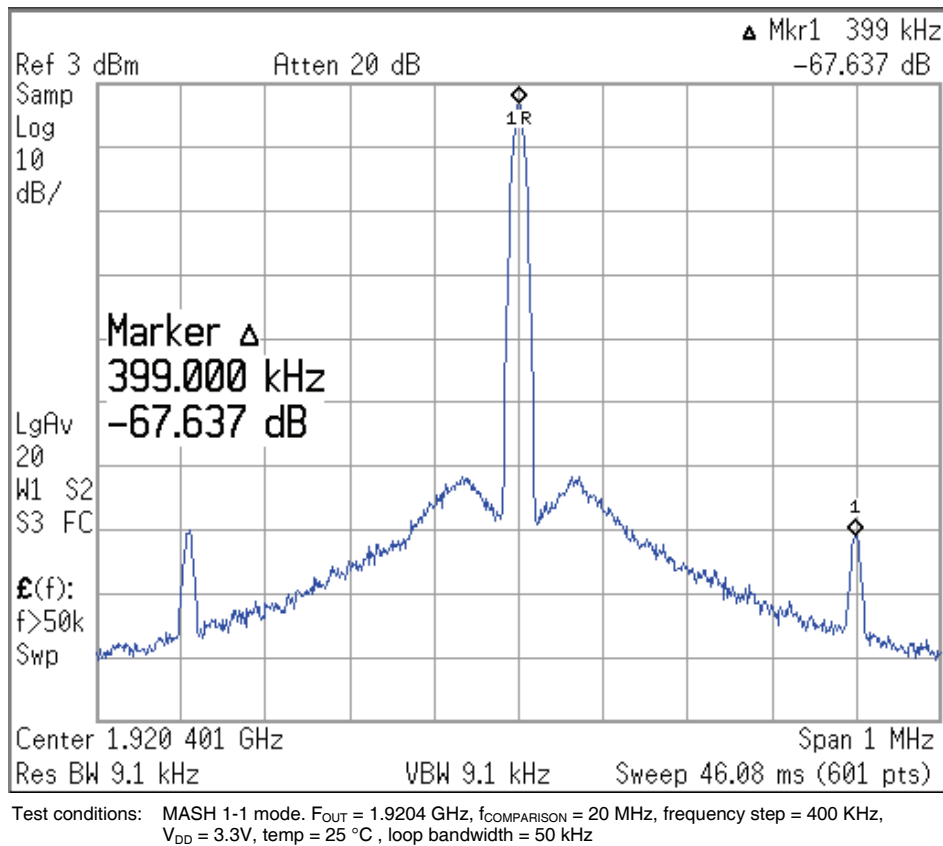


Figure 5. RF Sensitivity vs Frequency (typical device at temperature = +25 °C)

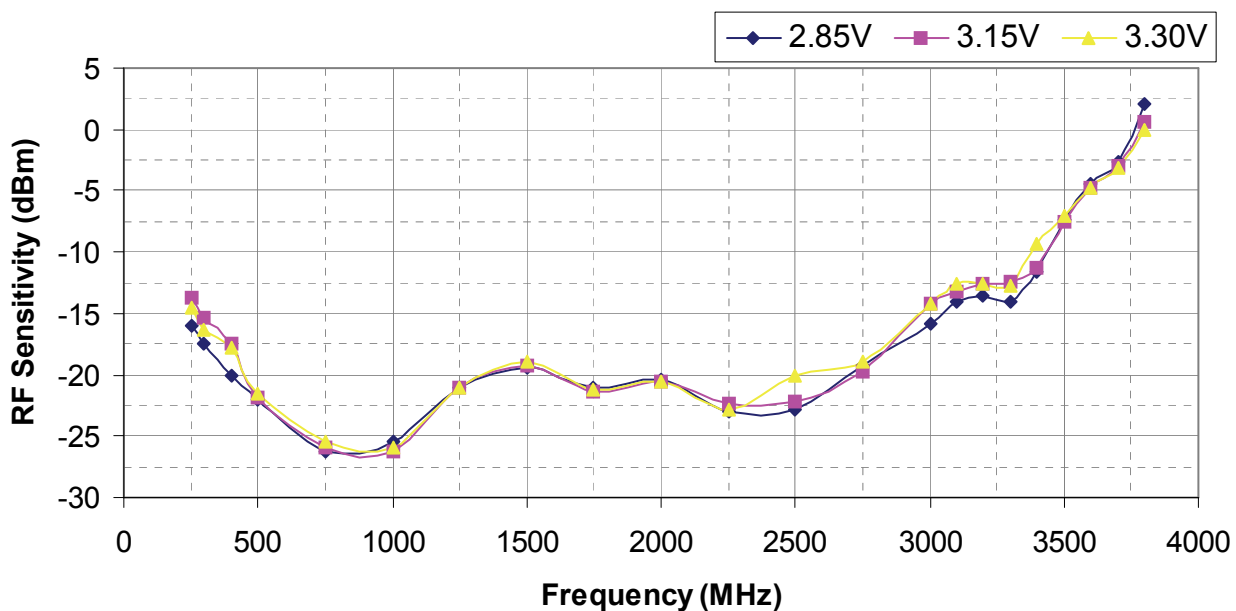
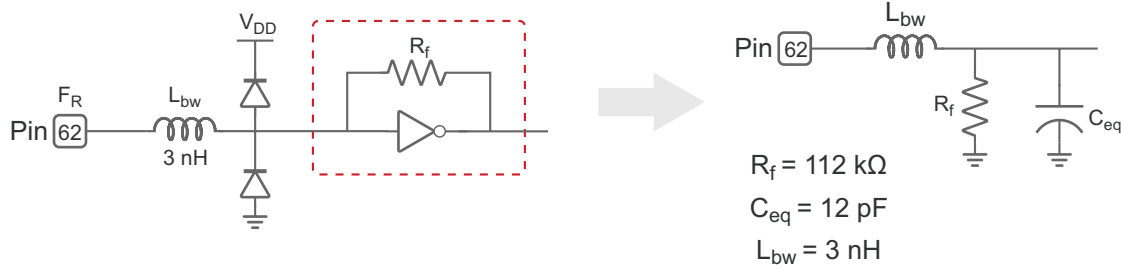
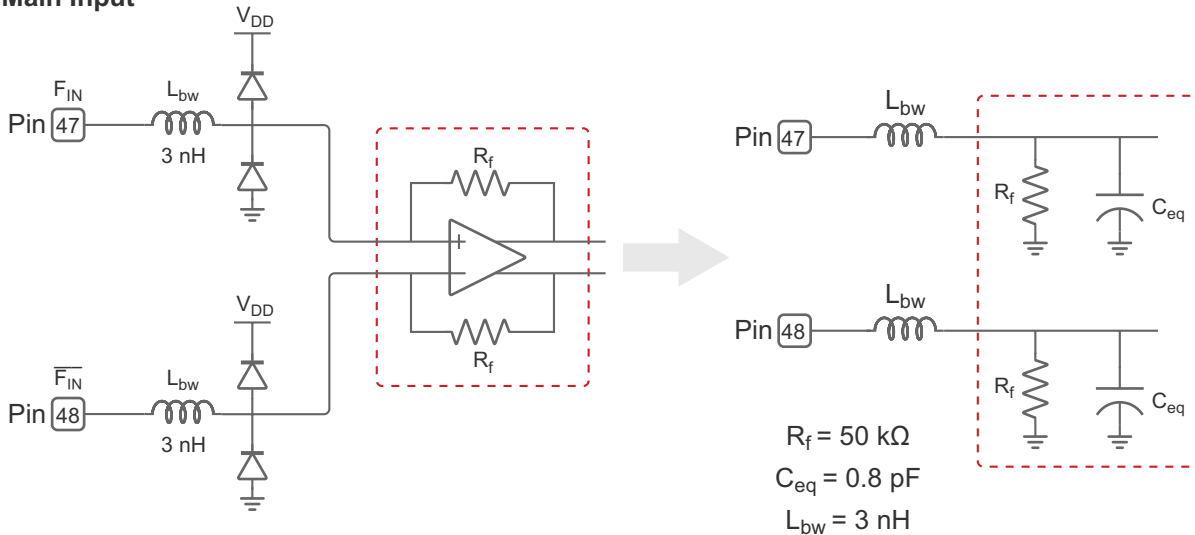


Figure 6. Equivalent Input Diagram: Reference Input
Reference Input



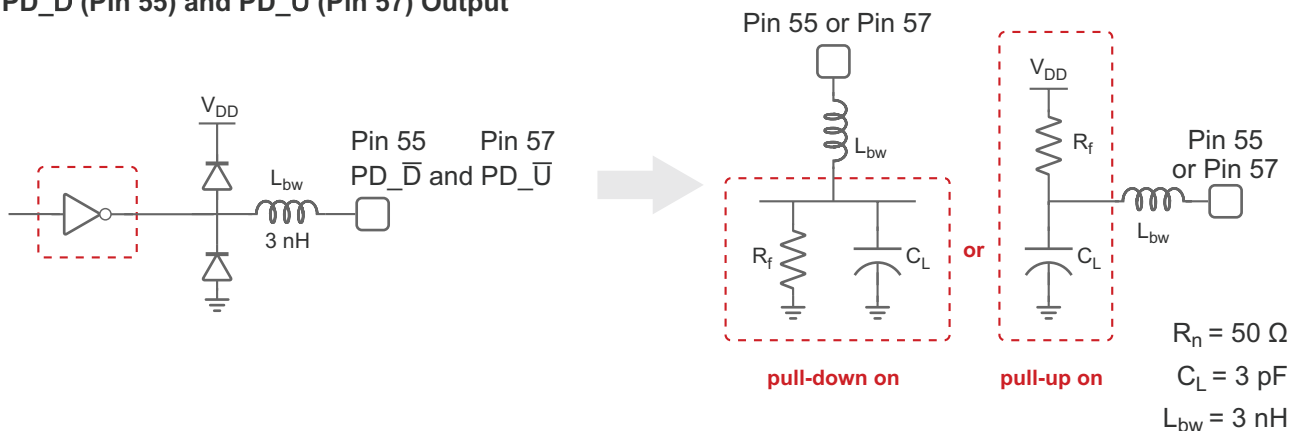
DOC-02126-3

Figure 7. Equivalent Input Diagram: Main Input
Main Input



DOC-02127-2

Figure 8. Equivalent Output Diagram: PD_D & PD_U Outputs
PD_D (Pin 55) and PD_U (Pin 57) Output



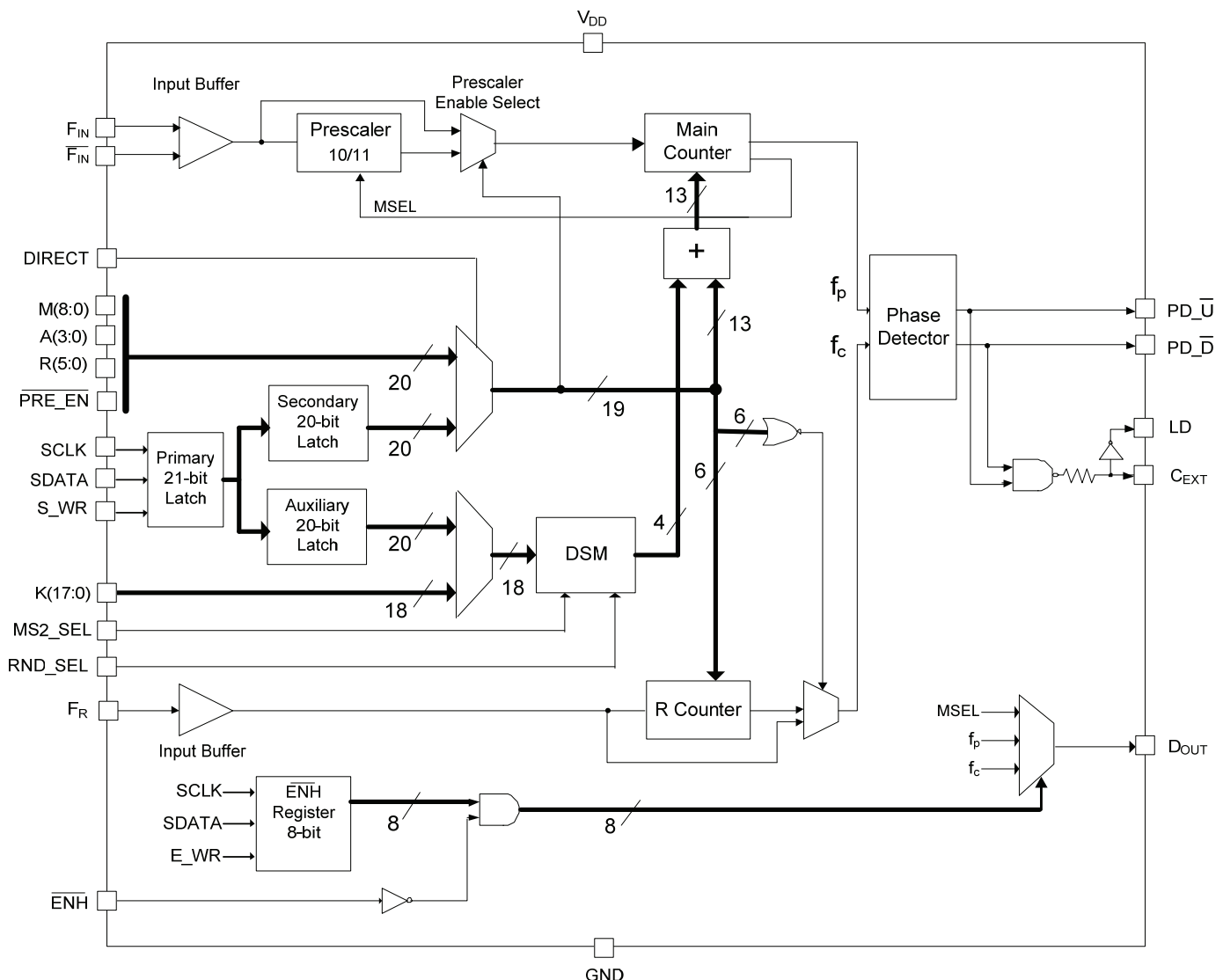
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Functional Description

The PE97632 consists of a prescaler, counters, an 18-bit delta-sigma modulator (DSM) and a phase detector. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The DSM modulates the “A” counter outputs in order to achieve the desired fractional step.

The phase-frequency detector generates up and down frequency control signals. Data is written into the internal registers via the three wire serial bus. There are also various operational and test modes and a lock detect output.

Figure 9. Functional Block Diagram



Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency (F_{IN}) by an integer or fractional number derived from the values in the M and A counters, and the DSM input word K.

The part can be operated in integer-N mode or in two different fractional-N modes. Setting K and $RND_SEL = 0$ operates the part in integer-N mode. Setting K to a non-zero value operates the part in either fractional-N mode.

The fractional-N modes use a MASH (Multi-stage noise Shaping) decimation structure.

The MASH-1-1 mode is a 2nd order fractional dithering using four (2^2) N values: N-1, N, N+1, N+2.

MASH-1-1-1 mode is a 3rd order fractional dithering using eight (2^3) N values: N-3, N-2, N-1, N, N+1, N+2, N+3, N+4.

Setting the MS2_SEL pin HIGH enables MASH-1-1 mode and LOW enables MASH-1-1-1 mode. MASH-1-1 has a 40 dB/dec slope away from the carrier while MASH-1-1-1 has a 60 dB/dec slope.

The 18-bit accumulator size fixes the fractional value to $K/2^{18}$. However, there is an additional bit in the DSM that acts like an extra bit (19^{th} bit). This bit is enabled by setting the RND_SEL pin HIGH. Enabling this bit has the benefit of reducing the spurious levels. However, a small, positive frequency offset will occur which is calculated as:

$$F_{offset} = [F_R / (R + 1)] / 2^{19} \quad (1)$$

Using the part in either MASH mode will yield a fractional spur at

$$F_{spur} = \begin{aligned} &[(2K + RND_SEL) / 2^{19}] \times f_c \quad 1 \leq K \leq 2^{17} \quad (2) \\ &[1 - (2K + RND_SEL) / 2^{19}] \times f_c \quad (2^{17} + 1) \leq K \leq (2^{18} - 1) \end{aligned}$$

Where f_c is the comparison frequency.

MASH-1-1-1 mode reduces this spur for an increase in the phase noise and decrease in the number of valid programming frequencies.

All of the following equations do not take into account the frequency offset from RND_SEL . If this offset is important to a specific frequency plan, it should be taken into account accordingly.

During normal operation, the output from the main counter chain (f_p) is related to the VCO frequency (F_{IN}) by the following equations:

$$f_p = F_{IN} / (N + K/2^{18}) \quad (3)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1, 1 \leq M \leq 511$$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = (N + K/2^{18}) \times [F_R / (R + 1)] \quad (4)$$

where

$$N = 10 \times (M + 1) + A$$

$$A \leq M + 1, 1 \leq M \leq 511$$

A consequence of the upper limit on A is that:

In integer-N mode, to obtain contiguous channels, F_{IN} must be $\geq 90 \times [F_R / (R + 1)]$.

In MASH-1-1 mode, to obtain contiguous channels, F_{IN} must be $\geq 91 \times [F_R / (R + 1)]$.

In MASH-1-1-1 mode, to obtain contiguous channels, F_{IN} must be $\geq 93 \times [F_R / (R + 1)]$.

The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M. Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode ()*

Setting the frequency control register bit $\overline{\text{PRE_EN}}$ HIGH allows F_{IN} to bypass the $\div 10/11$ prescaler. In this mode, the prescaler and A counter are powered down, and the input VCO frequency is divided by the M counter directly.

The following equation relates F_{IN} to the reference frequency F_{R} :

$$F_{\text{IN}} = (M + 1) \times [F_{\text{R}} / (R + 1)] \quad (5)$$

where

$$1 \leq M \leq 511$$

(*) Only Integer-N mode

In the frequency bypass mode, neither A counter nor K counter is used; therefore, only integer-N operation is possible.

Reference Counter

The reference counter chain divides the reference frequency (F_{R}) down to the phase detector comparison frequency f_{C} .

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_{\text{C}} = F_{\text{R}} / (R + 1) \quad (6)$$

where

$$0 \leq R \leq 63$$

Note that programming R with a “0” will pass the reference frequency (F_{R}) directly to the phase detector.

Register Programming

Serial Interface Mode

While the E_WR input is LOW and the S_WR input is LOW, serial input data (SDATA input), B₀ to B₂₀, are clocked serially into the primary register on the rising edge of SCLK, MSB (B₀) first. The LSB is used as an address bit. When 0, the contents from the primary register are transferred into the secondary register on the rising edge of either S_WR according to the timing diagrams shown in *Figure 10*. When 1, data is transferred to the auxiliary register according to the same timing diagram. The secondary register is used to program the various counters, while the auxiliary register is used to program the DSM.

Data are transferred to the counters as shown in *Table 8*.

While the E_WR input is HIGH and the S_WR input is LOW, serial input data (SDATA input), B₀ to B₇, are clocked serially into the enhancement register on the rising edge of SCLK, MSB (B₀) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 10*. After the falling edge of E_WR, the data provide control bits as shown in *Table 9* will have their bit functionality enabled by asserting the ENH input LOW.

Direct Interface Mode

Direct Interface mode is selected by setting the DIRECT input HIGH.

Counter control bits are set directly at the pins as shown in *Table 7* and *Table 8*.

Table 7. Secondary Register Programming

Interface Mode	ENH	R ₅	R ₄	M ₈	M ₇	PRE_EN	M ₆	M ₅	M ₄	M ₃	M ₂	M ₁	M ₀	R ₃	R ₂	R ₁	R ₀	A ₃	A ₂	A ₁	A ₀	Addr
Direct	1	R ₅	R ₄	M ₈	M ₇	PRE_EN	M ₆	M ₅	M ₄	M ₃	M ₂	M ₁	M ₀	R ₃	R ₂	R ₁	R ₀	A ₃	A ₂	A ₁	A ₀	X
Serial*	1	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇	B ₈	B ₉	B ₁₀	B ₁₁	B ₁₂	B ₁₃	B ₁₄	B ₁₅	B ₁₆	B ₁₇	B ₁₈	B ₁₉	0

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in secondary register on S_WR rising edge.

↑
MSB (first in)

↑
(last in) LSB

Table 8. Auxiliary Register Programming

Interface Mode	ENH	K ₁₇	K ₁₆	K ₁₅	K ₁₄	K ₁₃	K ₁₂	K ₁₁	K ₁₀	K ₉	K ₈	K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀	Rsrv	Rsrv	Addr
Direct	1	K ₁₇	K ₁₆	K ₁₅	K ₁₄	K ₁₃	K ₁₂	K ₁₁	K ₁₀	K ₉	K ₈	K ₇	K ₆	K ₅	K ₄	K ₃	K ₂	K ₁	K ₀	X	X	X
Serial*	1	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇	B ₈	B ₉	B ₁₀	B ₁₁	B ₁₂	B ₁₃	B ₁₄	B ₁₅	B ₁₆	B ₁₇	B ₁₈	B ₁₉	1

Note: * Serial data clocked serially on SCLK rising edge while E_WR LOW and captured in auxiliary register on S_WR rising edge.

↑
MSB (first in)

↑
(last in) LSB

Table 9. Enhancement Register Programming

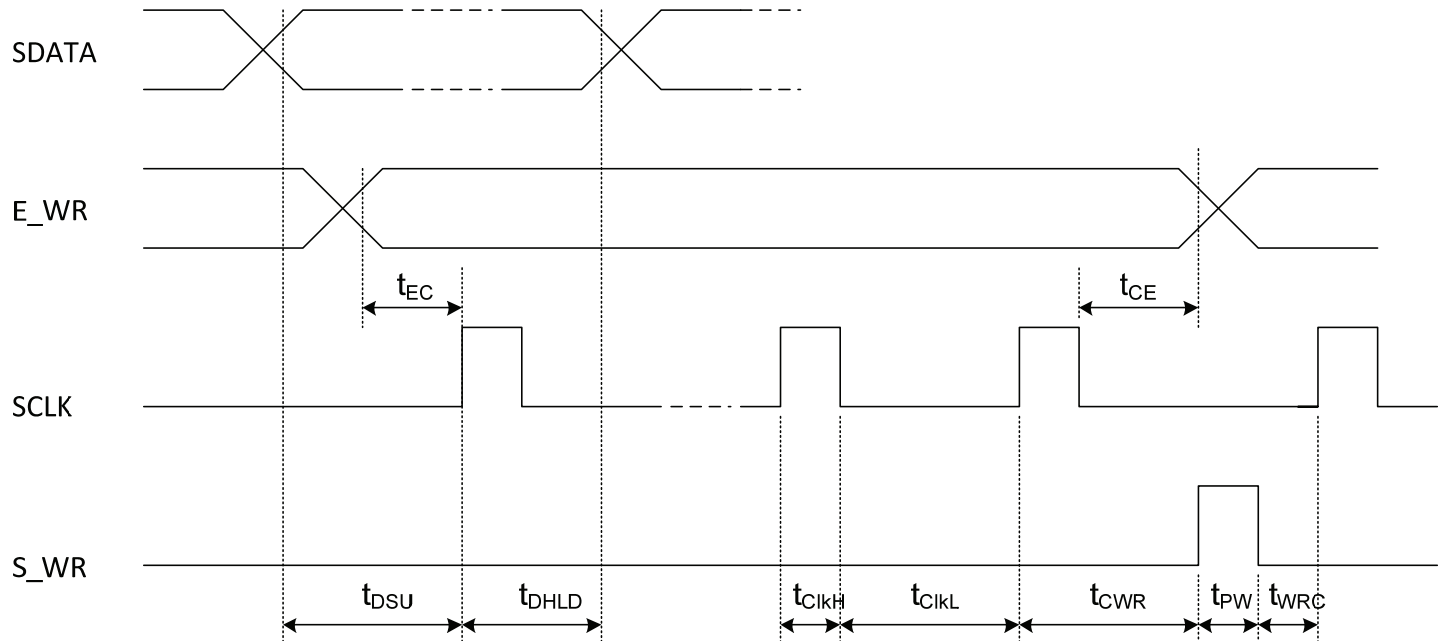
Interface Mode	ENH	Reserved	Reserved	f _p output	Power Down	Counter load	MSEL output	f _c output	LD Disable
Serial*	0	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇

Note: * Serial data clocked serially on SCLK rising edge while E_WR HIGH and captured in the double buffer on E_WR falling edge.

↑
MSB (first in)

↑
(last in) LSB

Figure 10. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 10. Enhancement Register Bit Functionality

Bit	Bit Function	Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	f_p output	Drives the M counter output onto the D _{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D _{OUT} output.
Bit 6	f_c output	Drives the reference counter output onto the D _{OUT} output.
Bit 7	LD Disable	Disables the LD pin for quieter operation.

Note: * Program to 0.

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely $PD_{\bar{U}}$ and $PD_{\bar{D}}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), $PD_{\bar{D}}$ pulses LOW. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), $PD_{\bar{U}}$ pulses LOW. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c .

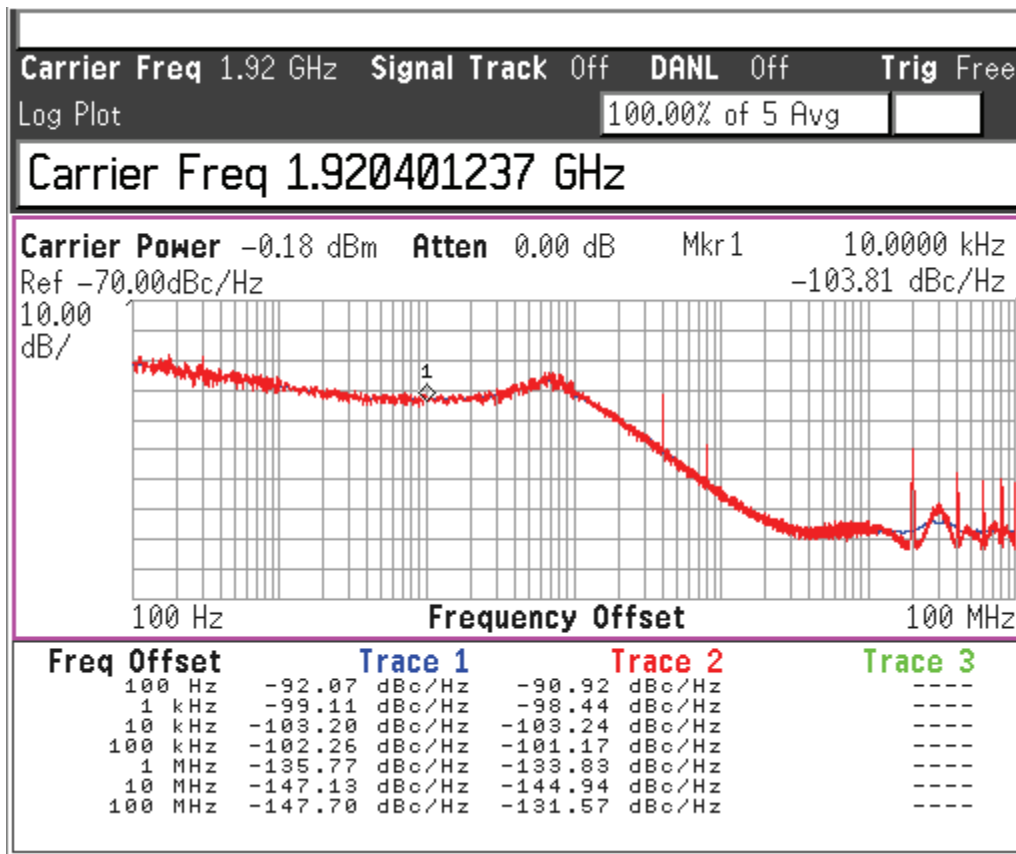
For the UP and DOWN mode, $PD_{\bar{U}}$ and $PD_{\bar{D}}$ drive an active loop filter which controls the VCO tune voltage. The phase detector gain is equal to $V_{DD}/2\pi$.

$PD_{\bar{U}}$ pulses cause an increase in VCO frequency and $PD_{\bar{D}}$ pulses cause a decrease in VCO frequency, for a positive K_v VCO.

A lock detect output, LD is also provided, via the pin C_{EXT} . C_{EXT} is the logical “NAND” of $PD_{\bar{U}}$ and $PD_{\bar{D}}$ waveforms, which is driven through a series 2 k Ω resistor. Connecting C_{EXT} to an external shunt capacitor provides low pass filtering of this signal. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of $PD_{\bar{U}}$ and $PD_{\bar{D}}$.

Figure 11. Typical Phase Noise

A typical phase noise plot is shown below. “Trace 1” is the smoothed average, and “Trace 2” is the raw data.



Test conditions: MASH-1-1 mode, $F_{OUT} = 1.9204$ GHz, $f_{COMPARISON} = 20$ MHz, $V_{DD} = 3.3$ V, temp = +25 °C, loop bandwidth = 50 kHz.

Figure 12. Package Drawing (dimensions are in millimeters)
68-lead CQFJ

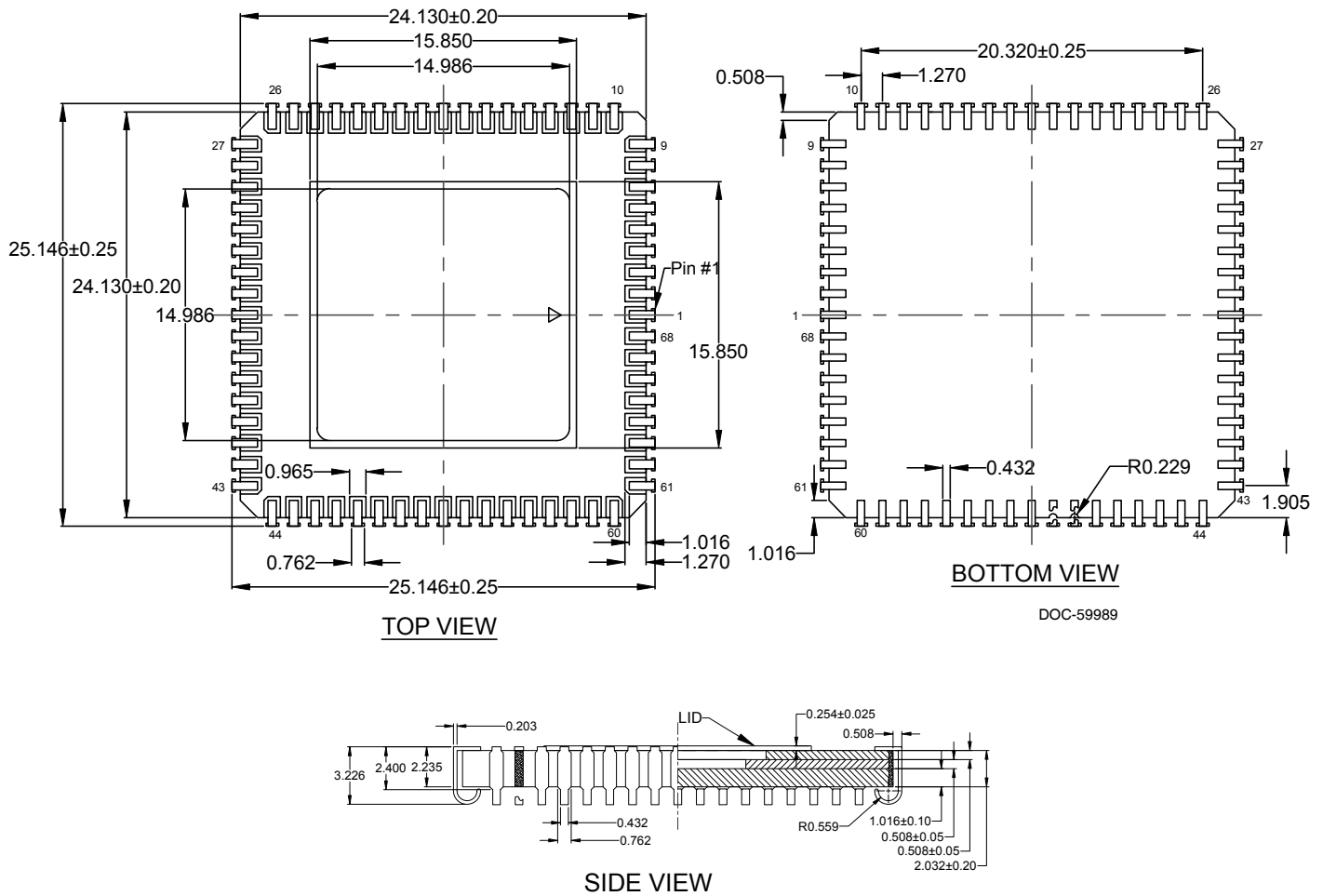
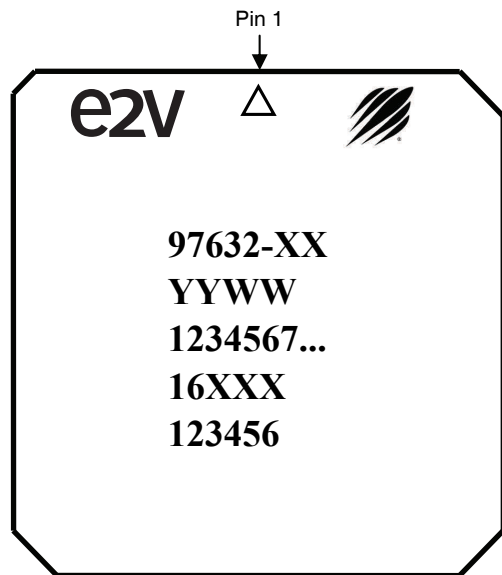


Figure 13. Top Marking Specifications



Not to scale

PRT-25223

Line 1: Pin 1 indicator $\triangle$, e2v and Peregrine logo
Line 2: Part number (XX will be specified by the purchase order)
Line 3: Date code (last two digits of the year and work week)
Line 4: Wafer lot # (as many characters as room allows)
Line 5: DOP # (e2v internal / 5 digits / optional, as room allows)
Line 6: Serial # (5 digits minimum)

Note: There is **NO** backside marking on any of the Peregrine products.

Table 11. Ordering Information

Order Code	Description	Packaging	Shipping Method
97632-01 ¹	Engineering samples	68-lead CQFJ	21 units / tray
97632-11	Flight units	68-lead CQFJ	21 units / tray
97632-00	Evaluation kit		1/Box

Note: * The 97632-01 devices are engineering sample (ES) prototype units intended for use as initial evaluation units for customers of the PE97632-11 flight units. The PE97632-01 device provides the same functionality and footprint as the PE97632-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. no burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ <http://www.teledyne-e2v.com> ~ inquiries@e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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