# Considerations for GaN power devices for low-temperature operation and Space Applications – by James F. Salzman

Quality and test standards have evolved over many years, from a few simple methods to large documents such as MIL-STD-883, 750, 38584, 38535, Q100, Q101 ESCCxxx, etc. These standards change over time, due to technology advances, operational findings, historical data, better test methods, etc. Various standard committees meet several times each year to update and provide inputs to these various standard documents through their associated standard bodies. Many yearly workshops also contribute to these standards bodies. The Reliability of Compound Semiconductors (ROCS) is an example of a yearly workshop sponsored by JEDEC, section JC-14.7, a recent committee established to investigate reliability of compound semiconductors, i.e., GaAs, SiC, InP, GaN, etc. Over the past few years a growing number of papers and publications deal with reliability findings of these compound semiconductors. A presentation recently presented at ROCS, by Transphorm **" Reliability Testing of AlGaN/GaN Power Switch Devices at Low and High Temperature"** discusses reliability testing of MISHEMT GaN FETs using low temperatures which can result in low activation energy for certain tests, like HVOS, where historically most reliability tests are performed at elevated temperatures where most power devices operate at elevated junction temperatures.

There are application where GaN devices are used, even at cryogenic temperatures, in optical sensor arrays, etc. , and associated reliability studies performed, i.e., **"Investigation of AlGan/Gan HEMTs degradation with gate pulse stressing at cryogenic temperature".** Ning Wang, Hui Wang, Xinpeng Lin, Yongle Qi, Tianli Duan, Lingli Jiang, AIP Advances 7,095317 (September 2017)

Transphorm reported HVOS failures at low temperatures, such as -55°C. It is well know that GaN FET failure often occurs between the gate and drain due to high electric fields. The Transphorm GaN FETs are based on a GaN D-mode cascode arrangement using a D-mode GaN MISHEMT in series with an E-mode Si MOSFET. The Transform technology, similar to Texas Instruments, and others use MISHEMT gate structures where an insulated gate is used similar to standard silicon MOSFETS. The gate dielectric can be oxide, nitride or a combination of these and must with stand high electric fields. Gate dielectric breakdown and channel length contributing to RDSon is often a trade-off that needs to be made. Field plates are often used in these devices to spread the electric field between gate and drain. Transistor layout is very important in these structures. A disadvantage of MISHEMT technology is its weakness to traps in the gate dielectric layer or at the dielectric/AlGaN interface. This has been shown to be a critical element that contributes to device performance and reliability as reported by G. Meneghesso, M. Menehini, D. Bisi, I. Rossetto, T. L. Wu, M. V. Hove, D. Marcon, S. Stoffels, S. Decoutere, and E. Zanoni, Microelectronics Reliability 58, 151 (2016).

GaN Systems HEMT does not use an insulated gate but rather a MESA gate structure with a Schottky junction, nor does it need a cascode silicon FET. It is a true Enhancement Mode HEMT device. The patented GaN systems "Island" gate technology is one reason GaN Systems FETs can withstand a higher gate voltage vs RDSon than MISHEMT type GaN FETs.

GaN Systems FET structures also do not have a direct nitride interface to the AlGaN layer further reducing trapping that normally occurs with GaN FETS that use a SiN/AlGaN interface layer.

GaN systems also uses an effective triple-field plate, with a unique layout structure to spread the electric field in the channel between the gate and drain allowing operation @650 volts drain potential, but can tolerate short durations exceeding 1 000 volts. The key to controlling this effect is the use of field plates to control and minimize any peaks in the electric field in this gate to drain region. Field plates depend on optimized metal layers and interlevel dielectrics. GaN Systems has characterized their devices over a temperature range from -55°C to 150°C. Further work on pulsed-temperature cycling is an ongoing process. As with any technology, it is important to control voltage spikes and stay within maximum device ratings.

To further address FET failure modes, it is important to compare failure modes vs applications, measurements, and existing test standards as mentioned in the beginning of this paper. The failure of power FETs, in general, occurs in "semi-on" conditions. That is, close to the maximum of hot-electron generation which can be detected with the aid of electroluminescence (EL) measurements from excessive heat being generated, however this is not easily demonstrated in GaN devices and usually results in catastrophic destruction of the device due to the short channel lengths (spacing) and limited thermal dissipation area often associated with GaN FETs normally used in high power switching similar to mechanical switches. As indicated in the Transphorm paper, intrinsic parameters, like mobility, Idsat and Rdson, will improve at lower temperatures due to an increase in the channel mean free path. This is also true with **silicon**-based power FETs. As the temperature decreases, the mean free path increases and impact ionization will increase, resulting in more energy gain between collisions. The following paper further describes this. **Anomalous behavior of** AlGaN⁄GaNAlGaN⁄GaN **heterostructure field-effect transistors at cryogenic temperatures: From current collapse to current enhancement with cooling.** Appl. Phys. Lett. **90**, 123505 (2007). “While current collapse effects of AlGaN/GaNAlGaN/GaN hetrojunction field-effect transistors (HFETs) around room temperature, it gradually gives place to a current enhancement with cooling—below 200K, electrically stressed devices do show higher currents than in their *prestressed* state. This behavior can be explained by increased levels of channel impact ionization at lower temperatures.“

At elevated electric fields (higher drain voltage) or lower temperatures, impact ionization will increase due to an increase of the mean free path. It should be noted that electric field disruption, caused by heavy ions in space applications, will also increase impact ionization resulting in a lower LET tolerance…unless parasitic bipolar avalanche is the major failure mode causing burnout at high temperatures in silicon-based FETs. Existing JEDEC 57 test methods recommend high temperature testing for single-event latch-up (SEL) and single-event burnout (SEB), where parasitic bipolar avalanche has dominated SEB failures historically in silicon-based power FETs. If impact ionization is the dominating factor in FET SEB, then testing at lower temperatures, where impact ionization is greater, will result in a lower SEB LET as

indicated in the following paper where SEB susceptibility of the power MOSFET decreases with increasing temperature.

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 39, NO. 6. DECEMBER 1992 TEMPERATURE **DEPENDENCE OF SINGLE-EVENT BURNOUT IN N-CHANNEL POWER MOSFETS** + Gregory H. Johnson, Ronald D. Schrimpf, and Kenneth F. Galloway

Channel impact ionization is a concern and can be addressed with proper field plates and buffer layer engineering. As previously mentioned, GaN systems has characterized its GaN devices to -55°C at rated High Voltage Off State (HVOS) conditions. However, as mentioned above, impact ionization will increase at lower temperatures thus producing lower Linear Energy Transfer (LET) tolerance for both silicon and compound semiconductors. JEDEC and other standards bodies will continue to address improved test methods, but existing test standards do not address some of these issues…especially with applications associated with space use. I do plan to bring up this issue in the next JEDEC JC-13.4 and JC-14.7 meetings.

For example, existing test standards, such as MIL-STD-883 test methods, do not address TID or Displacement Damage Dose (DDD) at temperatures other than room temperature. A large gap exists with bipolar technologies whereby gain (hFE) is greatly reduced by DDD, low TID rate, and low temperature (-55°C). These tests are all conducted separately, and it's left up to the user to carefully examine the total combined effects. GaN HEMT devices are not plagued by parasitic bipolar avalanche breakdown, nor do they have a back-channel diode junction typically found in silicon-based MOSFETs. Existing JEDEC standards include an HTRB (High Temperature Reverse Bias) test which historically has been used as a test for the reverse body diode and parasitic bipolar transistor that exists in standard silicon MOSFETS.

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