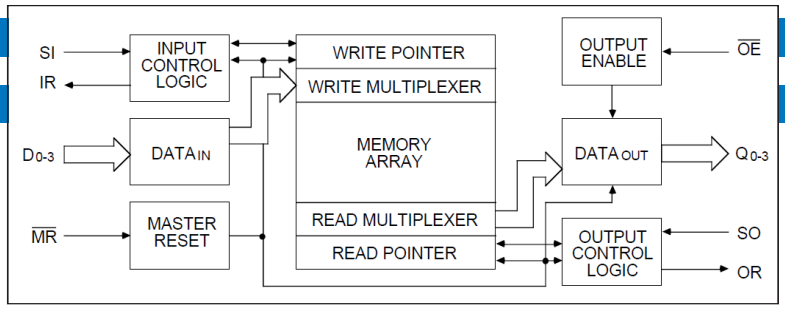
TD72403L10DB

February 2021

CMOS PARALLEL FIFO 64 x 4-BIT, 10 MHZ



Functional Description

The TD72403 is an asynchronous, high performance First-In/First-Out (FIFO) memory organized 64 words by 4 bits. The IDT72403 has an Output Enable (OE) pin. The FIFO accepts 4-bit data at the data input (D0-D3). The stored data is stacked on a first-in/ first-out basis.

The Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data moves down one location in the stack. The Input Ready (IR) signal functions as a flag indicating when the input is ready for new data (IR = HIGH) or to signal when the FIFO stack is full (IR = LOW).

The Output Ready (OR) signal functions as a flag indicating that the output remains valid data (OR = HIGH) or indicating that the FIFO is empty (OR = LOW).

Reading and writing operations are completely asynchronous allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 10 MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

This military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535, Class level B.

Features

- First-In/First-Out Dual-Port memory
- 64 x 4 organization
- RAM-based FIFO with low fall-through time
- Low-power consumption
  — Active: 175 mW (typ.)
- Maximum shift frequency — 10 MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CMOS technology
- 16-CERDIP package CDIP2-T16
- Military MIL-PRF-38535, Class level B processing
- Military temperature range (–55°C to +125°C)

Functional Block Diagram

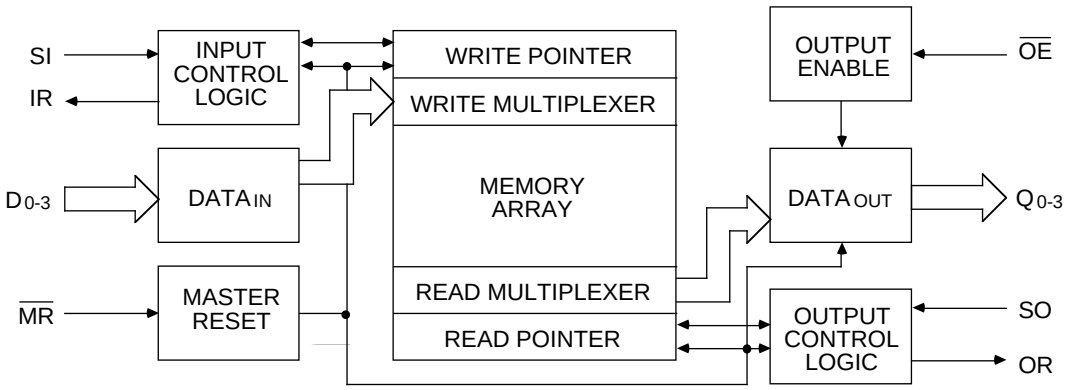
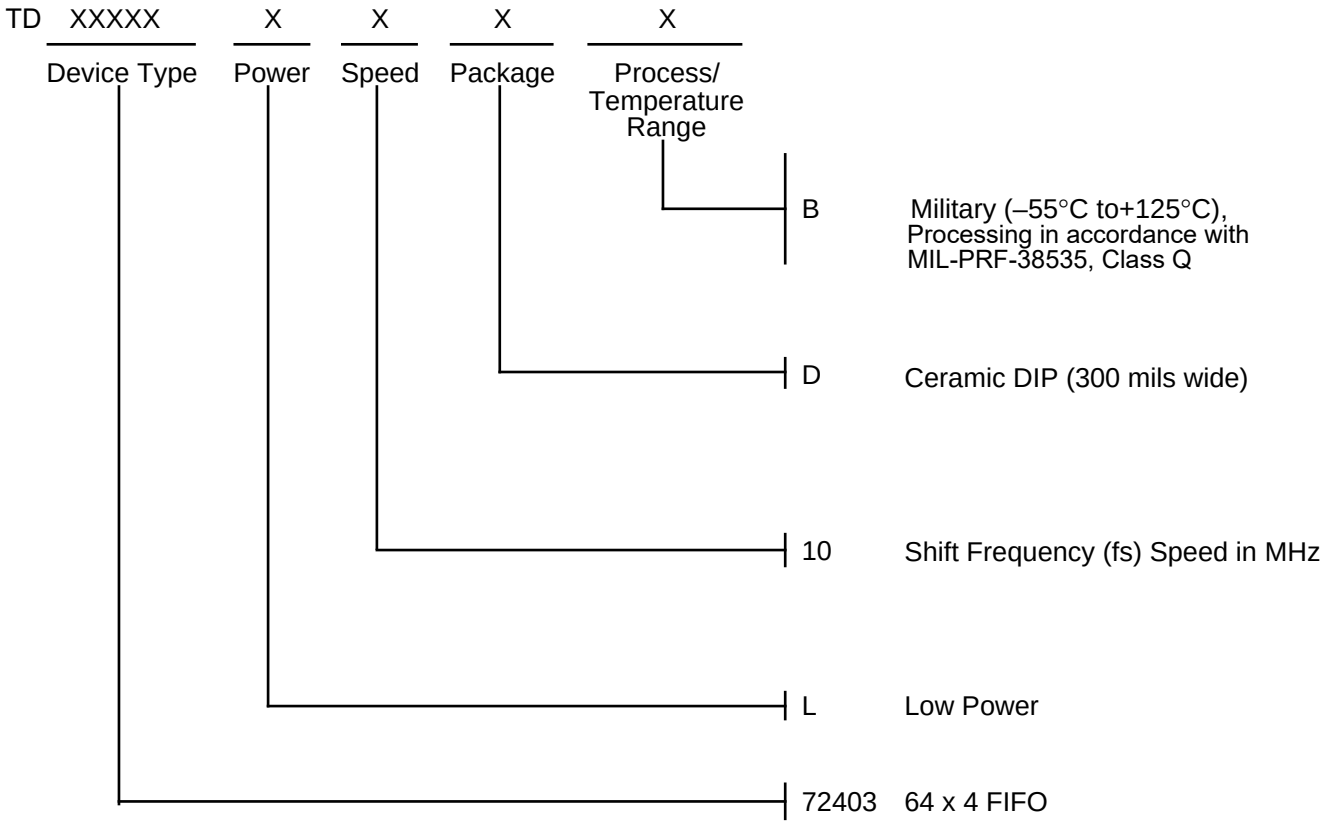
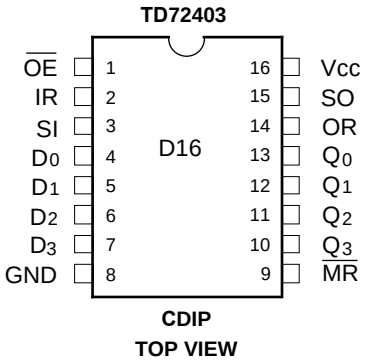


FIGURE 1. TD72403 Logic Block Diagram

Part Number Key



Pin Configuration



Note: The case outline is as designated in MIL-STD-1835 and as follows:

Descriptive designator	Terminals	Package style
GDIP1-T16	16	Dual-in-line package

1. Scope

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Terminal voltage with respect to ground	-0.5 V dc to +7.0 V dc
DC output current	50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (GND)	0 V dc
Input high voltage (SI & SO V_{IH})	2.35 V dc minimum
Input high voltage (V_{IH} all others)	2.0 V dc minimum
Input low voltage (SI V_{IL})	0.6 V dc maximum
Input low voltage (V_{IL} all others)	0.8 V dc maximum 2/
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short-circuit, test e.g., I_{OS}.
2/ -1.5 V undershoots are allowed for 10 ns once per cycle.

2. Electrical Performance

2.1 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

Note: Only Device Types All and 01 shall be applicable.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low current	I_{IL}	0 V ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All	-10		µA
Input high current for OE	I_{IH}	0 V ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All		+50	µA
Input high current for all others	I_{IH}	0 V ≤ V_{IN} ≤ 5.5 V, V_{CC} = 5.5 V	1, 2, 3	All		+10	µA
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output short-circuit current 1/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V	1, 2, 3	All	-20	-110	mA
Off-state output high current	I_{HZ}	V_{CC} = 5.5 V, V_O = 2.4 V	1, 2, 3	01-04		+20	µA
Off-state output low current	I_{LZ}	V_{CC} = 5.5 V, V_O = 0.4 V	1, 2, 3	01-04	-20		µA
Operating supply current	I_{CC}	All inputs = 0.0 V to 3.0 V, V_{CC} = 5.5 V, outputs open, f = 10 MHz	1, 2, 3	All		45	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz, T_A = +25°C, see 4.3.1c	4	All		10	pF
Functional test		See 4.3.1d	7, 8A, 8B	All			
Shift in rate	f_{IN}	See figures 2 - 8 as applicable 2/	9, 10, 11	01,05		10	MHz
				02,06		15	
				03,07		25	
				04,08		35	
Shift in to input ready low 3/	t_{IRL}		9, 10, 11	01,05		40	ns
				02,06		35	
				03,07		21	
				04,08		18	
Shift in to input ready high 3/	t_{IRH}		9, 10, 11	01,05		45	ns
				02,06		40	
				03,07		28	
				04,08		20	
Shift out rate	f_{OUT}		9, 10, 11	01,05		10	MHz
				02,06		15	
				03,07		25	
				04,08		35	

See footnotes at end of table.

Note: Only Device Types All and 01 shall be applicable.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shift out to output ready low 3/	t_{ORL}	See figures 2 - 8 as applicable 2/	9, 10, 11	01,05		40	ns
				02,06		35	
				03,07		19	
				04,08		18	
Shift out to output ready high 3/	t_{ORH}		9, 10, 11	01,05		55	ns
				02,06		40	
				03,07		34	
				04,08		20	
Output data hold, previous word	t_{ODH}		9, 10, 11	All	5.0		ns
Output data shift (next word)	t_{ODS}		9, 10, 11	01,02,05,06		55	ns
				03,07		35	
				04,08		25	
Data throughput or "fall through"	t_{PT}		9, 10, 11	01,02,05,06		65	ns
				03,07		40	
				04,08		28	
$\overline{\text{MASTER RESET}}$ to OR low	t_{MRORL}		9, 10, 11	01,05		40	ns
				02,03,06,07		35	
				04,08		28	
$\overline{\text{MASTER RESET}}$ to IR high	t_{MRIRH}		9, 10, 11	01,05		40	ns
				02,03,06,07		35	
				04,08		28	
$\overline{\text{MASTER RESET}}$ to data output low	t_{MRQ}		9, 10, 11	01,05		40	ns
				02,06		35	
				03,07		25	
				04,08		20	
Output valid from $\overline{OE}$ low	t_{OOE}		9, 10, 11	01		35	ns
				02		30	
				03		20	
				04		15	
Output high impedance from $\overline{OE}$ high 4/	t_{HZOE}		9, 10, 11	01		30	ns
				02		25	
				03		15	
				04		12	
Input ready pulse high 4/	t_{IPH}		9, 10, 11	01,02, 03,05,06,07	11		ns
				04,08	9.0		
Output ready pulse high 4/	t_{OPH}		9, 10, 11	01, 02, 03	10		ns
				04	5.0		

See footnotes at end of table.

Note: Only Device Types All and 01 shall be applicable.

TABLE I. Electrical performance characteristics – continued.

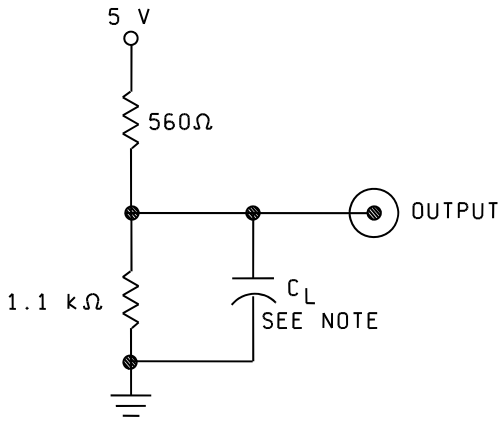
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Shift in high time 3/	t_{SIH}	See figures 2 - 8 as applicable 2/	9, 10, 11	01,02,05,06	11		ns
				03,07	11		
				04,08	9.0		
Shift in low time	t_{SIL}		9, 10, 11	01,05	30		ns
				02,06	25		
				03,07	24		
				04,08	17		
Input data setup time	t_{IDS}		9, 10, 11	All	0		ns
Input data hold time	t_{IDH}		9, 10, 11	01,05	40		ns
				02,06	30		
				03,07	20		
				04,08	15		
Shift out high time 3/	t_{SOH}		9, 10, 11	01,02,05,06	11		ns
				03,07	11		
				04,08	9.0		
Shift out low time	t_{SOL}		9, 10, 11	01,02,05,06	25		ns
				03,07	24		
				04,08	17		
$\overline{\text{MASTER RESET}}$ pulse width	t_{MRW}		9, 10, 11	01,05	30		ns
				02,03,04,06, 07,08	25		
$\overline{\text{MASTER RESET}}$ pulse to SI	t_{MRS}		9, 10, 11	01,02	35		ns
				05,06	25		
				03,04,07,08	10		
Data setup to IR	t_{SIR}		9, 10, 11	01,02,03,05, 06,07	5.0		ns
				04,08	3.0		
Data hold from IR	t_{HIR}		9, 10, 11	01,02,05,06	30		ns
				03,07	20		
				04,08	15		
Data setup to OR high 4/	t_{SOR}		9, 10, 11	All	0		ns

1/ Not more than one output should be shorted at a time. Duration of the short-circuit condition should not exceed one second. This parameter may not be tested, but shall be guaranteed to the limits specified in table I.

2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance. Output timing reference is 1.5 V.

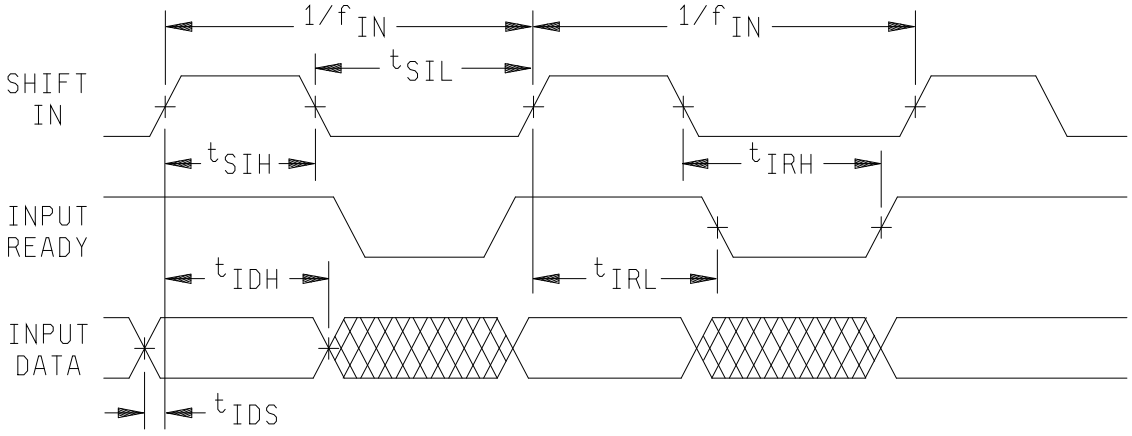
3/ Since these devices are very high speed, care must be exercised in the design of the hardware and timing utilized in the design. Device grounding and decoupling are crucial to correct operation as the device will respond to very small glitches due to long reflective lines, high capacitances or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead lengths is recommended.

4/ May not be tested, but shall be guaranteed to the limits specified in table I.



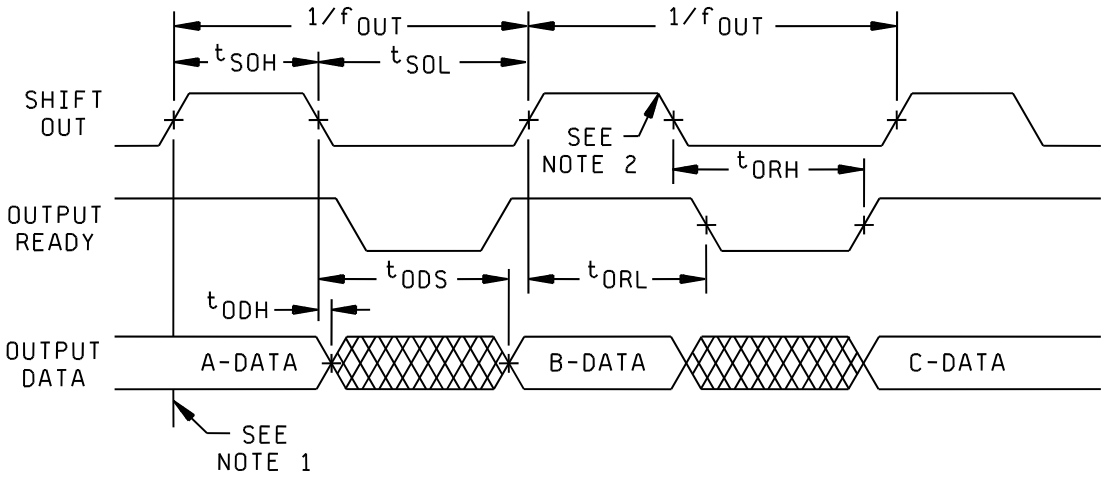
NOTE: C_L = 30 pF and includes jig and scope capacitance.

FIGURE 2. Output load circuit.



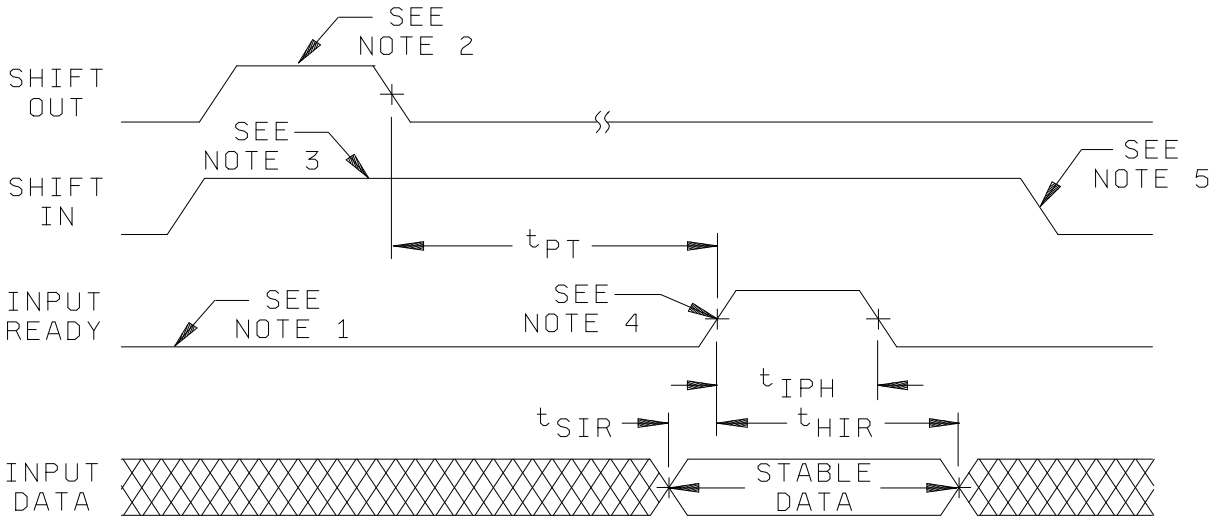
Note: IR/OR generated on rising or falling edges of their respective clocks.

FIGURE 3. Input timing diagram.



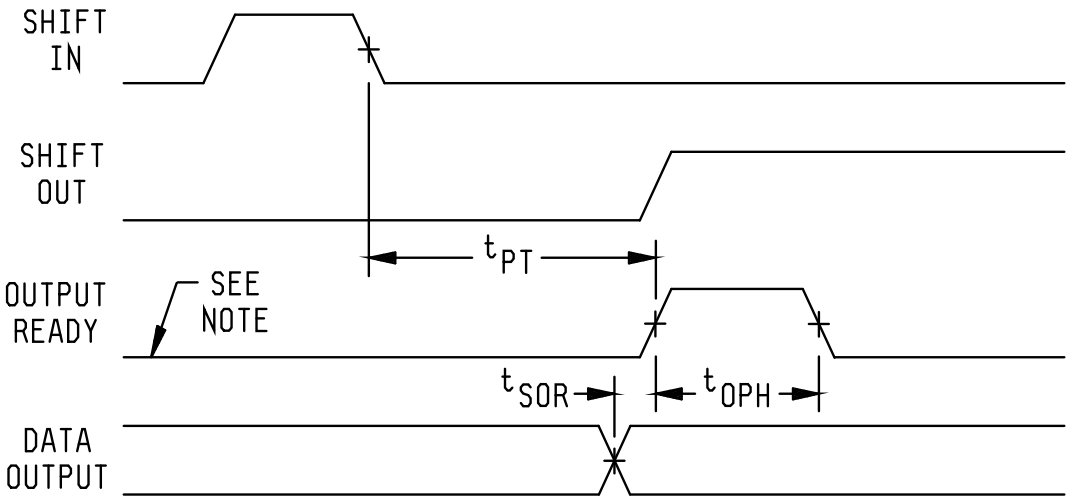
NOTES:
1. This data is loaded consecutively, A, B, C.
2. Data is shifted out when SHIFT OUT makes a high to low transition.

FIGURE 4. Output timing diagram.



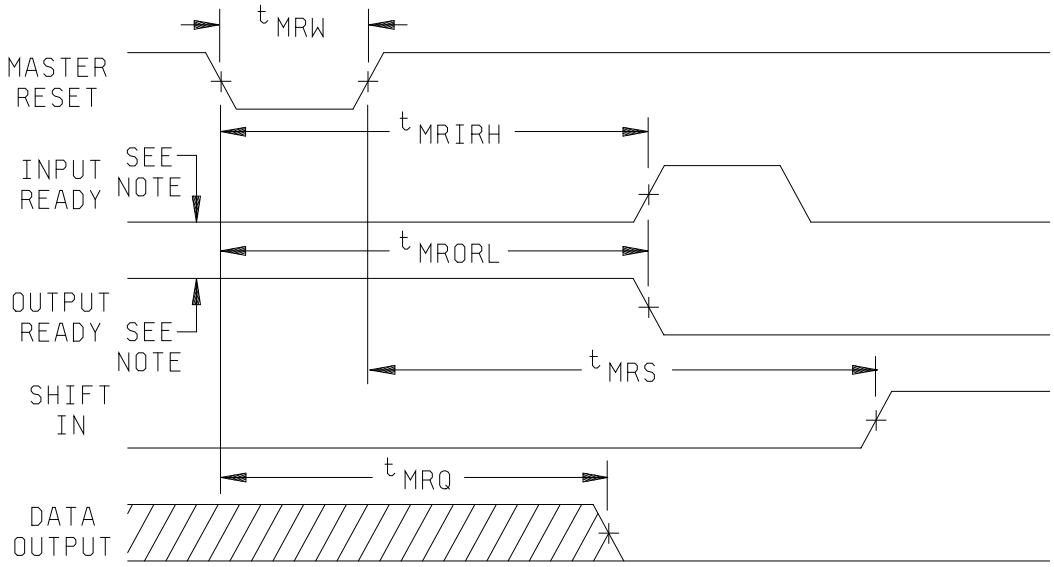
NOTES:
1. FIFO is initially full.
2. SHIFT OUT pulse is applied.
3. SHIFT IN is held high.
4. As soon as input ready becomes high the input data is loaded into the FIFO. IR/OR generated on rising or falling edges of their respective clocks..
5. The write pointer is incremented.

FIGURE 5. t_{IPH}, t_{HIR}, and t_{SIR} timing diagram.



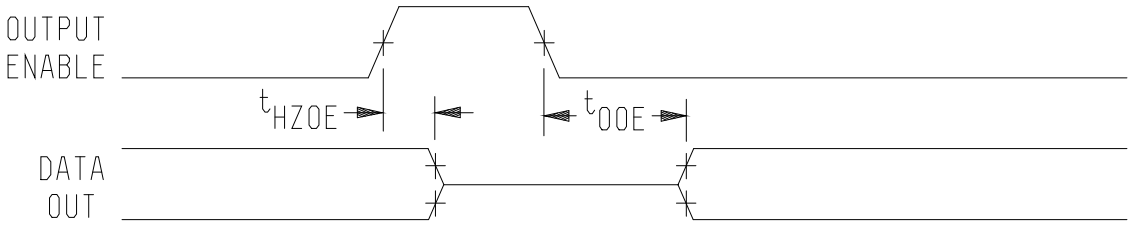
NOTE: FIFO initially empty.

FIGURE 6. t_{PT} and t_{OPH} timing diagram.



NOTE: Worst case, FIFO initially full.

FIGURE 7. $\overline{\text{MASTER RESET}}$ timing.



NOTE: High-Z transitions are referenced to the steady-state V_{OH} - 500 mV and V_{OL} + 500 mV levels on the output.

FIGURE 8. Output enable timing (device types 01-04 only).

3. Verification

3.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

3.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

3.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

3.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the device to function correctly.

3.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8A, 8B

1/ * Indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** See 4.3.1c.

4/ As a minimum, subgroups 7 and 8 shall consist of verifying the data pattern.

4. Packaging

4.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

5. Notes

5.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

5.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

5.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

5.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

5.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

5.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

Ordering Information

Order Code	Description	Package	Shipping Method
TD72403L10DB	First-In/First-Out (FIFO) memory 64 words by 4 bits	16-CDIP	28 per Tube

Revision Information

Document	Description / Date	Change/Revision Details
TD72403-2-2021 Rev 1	TD72403L10DB / February 2021	Initial Release

Document Categories:

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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Product Specification

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