MMIC MODULE FOR A K_U-BAND MINIATURE AIRBORNE ACTIVE ARRAY RADAR

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Abstract

Monolithic Microwave Integrated Circuits (MMICs) and transmit/receive (T/R) modules are being used extensively in systems such as active array radars. The development of sensors for small UAV platforms demands light weight, compact dimensions, low cost and reliability. These requirements have led to the development of highly integrated MMICs in packages where double-sided thick film multilayer substrates are used. The components needed for the MMICs are phase shifters, attenuators, switches, Low Noise Amplifiers (LNA) and power amplifiers. Component re-use is achieved by switching both phase shifter and attenuator, shared in the transmit and receive paths. Each complete T/R module fits within the half wavelength spacing constraints demanded by the associated antenna array with which the modules are integrated.

1 Introduction

Unmanned aerial vehicles (UAVs) have become increasingly of interest in recent years, due to the capabilities that they provide [1]. In military applications, the emphasis of using a UAV is primarily for intelligence, surveillance, target acquisition and reconnaissance (ISTAR). Due to the UAV's small size, conventional sensors are too large and heavy; therefore small volume and light weight alternatives are needed.

One of the RF payloads for these vehicles is a synthetic aperture radar (SAR) which by incorporating an active phased array antenna, provides high flexibility in complex missions for ISTAR. The key element of the active antenna is the transmit/receive (T/R) module. Each of these modules feeds a single radiating element in the antenna. An antenna can consist of hundreds of these elements; therefore, a reliable, reproducible and cost effective technology is essential. QinetiQ has investigated the implementation of a miniature active array radar that is suitable for use in SAR applications. With further development it can be made suitable for a conformal array.

Most of the radars for SAR applications use X-band. This spectrum is heavily utilized and so it is difficult to accommodate a wide band radar into it. Moreover, a higher operating frequency reduces the size of the module and hence the overall antenna size, which is beneficial as outlined above. However, as operating frequency increases, and antenna element spacing decreases, element separation becomes too restrictive for conventional T/R module components to fit in. Therefore new module integration techniques have to be invented including extension to the third dimension, i.e. 3D stacked module. Furthermore, the cost for this module is a prime driver for the total cost of the antenna array. A modest saving at the module level can result in significant savings at the array level due to the large number of modules involved in the array.

QinetiQ has demonstrated a compact integration of a T/R module that is suitable for volume assembly.

2 Design considerations

The aim of the module design is to achieve the radar system requirements within the half wavelength space constraint. At high frequencies, the available spacing between elements is reduced. At Ku band, the maximum footprint for the module is less than 9x9 mm^2. The common-leg architecture has been adopted to maximise space usage. The advantages and disadvantages of common-leg and separate architectures have been studied by McLachlan *et. al*. [2]. The following key factors for the T/R module of an airborne radar have been considered in the design process:

- Low noise figure
- High dynamic range
- High transmit/receive isolation
- Low power consumption
- 0°-360° phase control
- Amplitude control
- Compact size
- Low cost

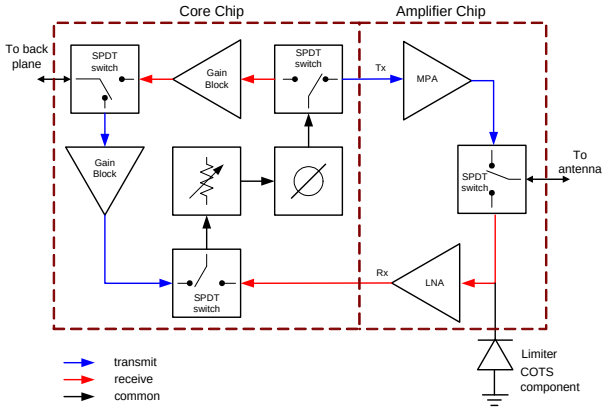

Figure 1 Functional block diagram of module

Figure 1 shows the functional block diagram. The T/R module consists of a phase shifter, attenuator, two buffer amplifiers, power amplifier, low noise amplifier (LNA) and four SPDT switches. This system has been realized in two MMICs, these were the "core chip" and the "amplifier chip". The core chip consisted of the phase and amplitude control elements, two gain block and three switches. The amplifier chip included the power amplifier, the LNA and a T/R switch. The PIN limiter however, could not be integrated. This was an additional component to be integrated at the module level; however, the matching circuit for this limiter was included in the amplifier chip.

The three switches in the core chip were required in order to reuse the phase and amplitude control components. In both transmit and receive modes the signals were routed so that they went through the phase and amplitude control blocks in the same direction. The buffer amplifiers (gain blocks) were placed before the phase and amplitude control devices in the transmit path. However, they were placed after the control elements on the receive path to maximise dynamic range. Gain distribution of the system was important in order to achieve noise and the third order inter-modulation product (IP3) requirements. This was carried out using the system analysis tool in Agilent ADS. In the receive path, the LNA was placed in close proximity to the antenna immediately after the T/R switch. This was to minimise the system noise figure. The output of the LNA was connected to the amplitude and phase control elements via a T/R switch in the core chip. A buffer amplifier was connected at the end of the receive chain to maximise the dynamic range. In transmit mode, the signal fed from the back plane was initially boosted by the buffer amplifier. The functions of the buffer amplifier were a) to provide isolation between the module and the distribution network and b) to boost the signal level prior to the phase and amplitude control blocks. This signal was then fed to the power amplifier on the amplifier MMIC via a T/R switch. The output of the power amplifier was connected to the transmit side of the antenna T/R switch which was in close proximity to the antenna to maximise power delivered to the antenna.

To minimise loop gain, isolation was maximised. This was achieved by a) good isolation in the switch circuit and b) switching the drain bias supplies of the amplifiers alternately between the transmit and receive periods. DC power consumption was also minimised.

The yield of MMIC dies is related to the circuit complexity, such as the number of active devices used. The more functions there are on one die, the lower the yield. However, assembly cost and yield is proportional to the complexity in module assembly, such as die-attach and wire bonding. Furthermore, due to the size constraint, the optimised solution was to integrate the system in two MMICs.

3 MMIC circuit design

In choosing a foundry process, it is important that the process can achieve the performance required at the lowest cost. The UMS PH25 low noise process has been chosen for the fabrication of the MMIC. This is a mature process that can achieve the performance requirement. This process employs a quarter micron gate length pHEMT technology that has a cut off frequency at 90GHz. Applications of up 50GHz have been reported. The noise figure quoted is 2dB at 10GHz. This process is optimised for low noise performance and it has a power density of 250mW/mm. This is sufficient for the power amplifier in the present application. Having both chips on the same process also minimises the development cost and achieves repeatable performance.

The circuit design was carried out using the Agilent ADS microwave circuit design tools. A process design kit provided by the foundry was also required for the foundry models. The design kit contained scalable active device models, a switch model and other passive component models such as inductors, capacitors and resistors. The automatic layout feature also reduced the design cycle time by removing the manual layout task. The final reticle layout was carried out on a MMIC layout tool - Wavemaker.

The component specifications were derived from the system simulation. This was carried out using the system analysis tools from Agilent ADS.

The T/R module functional block diagram showed in Figure 1 has been realized in two MMICs. These were called "core" and "amplifier" chips. The core chip had a 5 bit digital phase shifter, a 3 bit digital attenuator, two buffer amplifier and three T/R switches. The amplifier chip had a medium power amplifier, an LNA and a T/R switch.

3.1 Core chip

A micrograph of the core chip is shown in Figure 2. The core chip comprised the phase and amplitude control block, two gain blocks and three switches for routing transmit and receive signals.

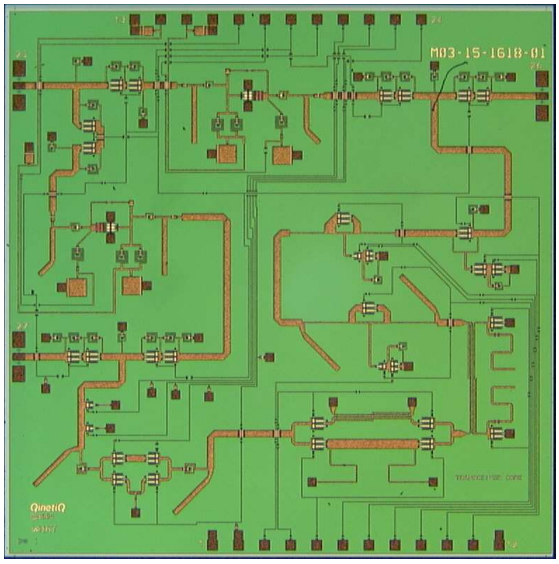

Figure 2 Micrograph of core chip

The common-leg topology required three switches for routing the signals between transmit and receive periods. The T/R switch was, therefore, important for the accuracy of the phase and amplitude control. A conventional approach has been adopted for the switch design where a cold FET (0V drain bias) was used as the switching element. The source and drain conductance was controlled by the voltage applied to the gate terminal. At "0V" gate bias, where the Schottky barrier was at equilibrium and the depletion region was at minimum, the channel conductance was at maximum value. Although the Schottky barrier could be reduced further by a positive bias, this would, however, compromise reliability of the device. On the other hand, channel pinch off was achieved by a "-1.5V" gate voltage. Maximum channel resistance was achieved between the source and drain terminals. The associated source and drain capacitance could not be ignored at these frequencies. An external inductor was connected in shunt configuration across the source and drain terminals to form a parallel resonant circuit at the desired frequency. This resulted in high impedance at resonance. Such circuit provide isolation better than 15dB. Figure 3 shows the measured and simulated response of such a circuit.

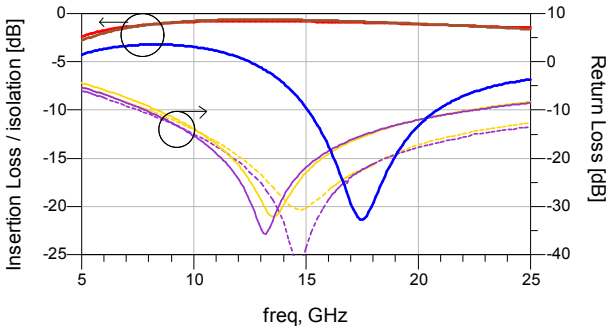

Figure 3 Response of a switch element

Figure 4 shows a schematic of the T/R switch. Two stages of the switch element were employed to achieve isolation of better than 30dB. It should be noted that the switch implemented here was a reflection type. This was because the amplifiers were switched on and off alternately. An absorptive switch does not add any benefit but increases real estate. A simulated response of such a switch is shown in Figure 5.

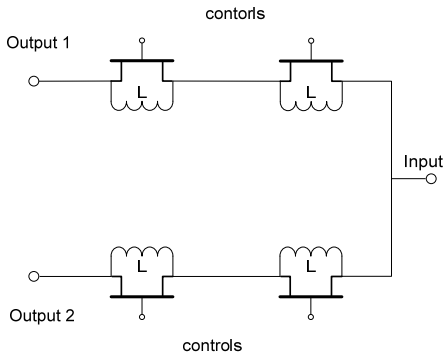

Figure 4 Schematic of a T/R switch

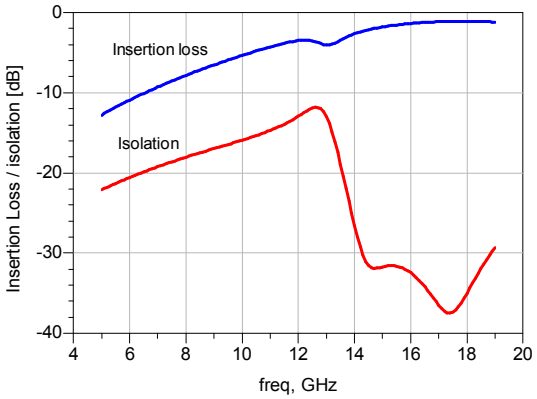

Figure 5 Insertion Loss and Isolation of a T/R switch - simulated

A five bit phase shifter was designed for the phase control block. Various circuit topologies were used in order to provide the phase shift requirement over the frequency range at small foot prints. For lower significant bits, switched filters were employed, while at higher significant bits, both reflection type and Boire type phase shifters [3] were used. Relative phase states are shown in Figure 6.

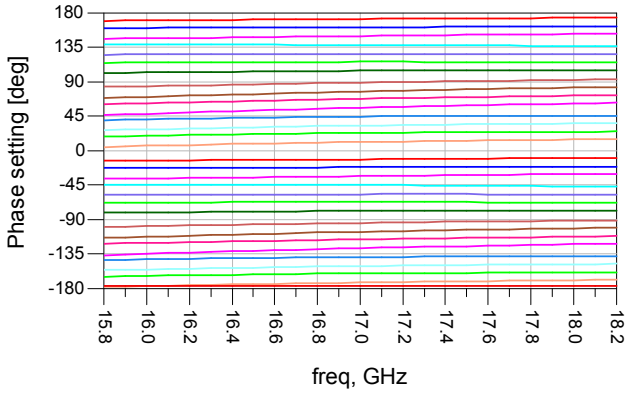

Figure 6 Relative phase states of phase shifter - simulated

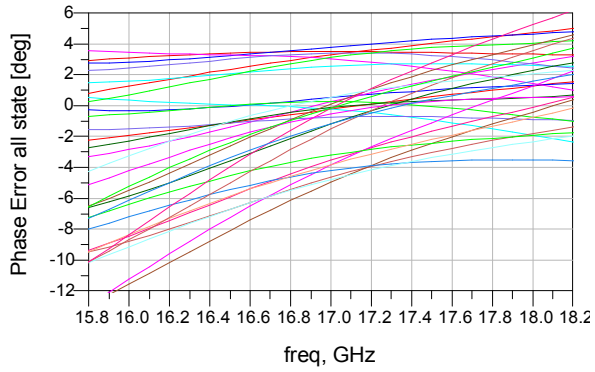

Figure 7 Phase error of all phase state - simulated

The corresponding phase error is shown in Figure 7. The maximum phase error was 17°, which occurred at the lower frequency range. This was due to the distributive load used in one of the reflective phase shifter bits. The absolute insertion loss was about 5dB with gain variation of 1.4dB over the frequency range at all phase states. The port match was 11dB at worst case.

The amplitude control of the active antenna was primarily realized using the antenna distribution network. A three bit attenuator was implemented in the core chip for calibration. The lower significant bits were implemented using loaded lines and a switched attenuator was used for the most significant bit. Figure 8 shows the simulated response. The phase error across the frequency band for all states was 2.2° at worst case.

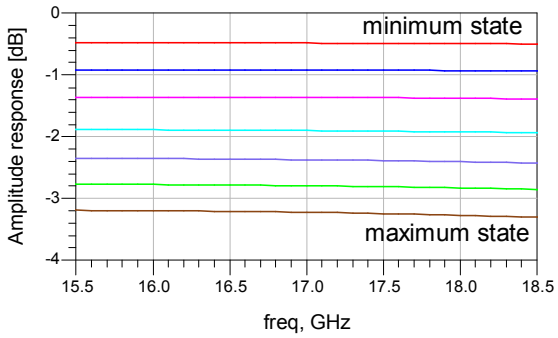

Figure 8 Amplitude response of the attenuator - simulated

Two gain blocks were used in the core chip to compensate for the loss due to the control elements so that the overall insertion loss was about 0dB. The drain bias of these amplifiers was switched alternately during transmit and receive periods to maximize transmit/receive isolation. A single stage feed back amplifier was designed for this purpose. The gain of the amplifier was 10dB with a gain slope of 0.5dB across the band. The positive gain slope was designed to compensate for the negative gain slope in both LNA and power amplifier. Figure 9 shows the amplifier response.

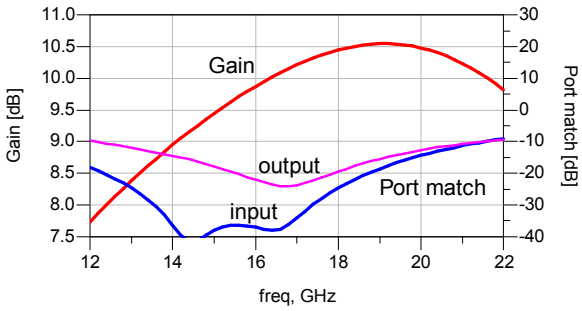

Figure 9 Gain and port match of buffer amplifier

RF on wafer measurements was carried out on the core chip. The bias supply and the control signals were controlled by a modular DC source monitor unit (SMU 4142).

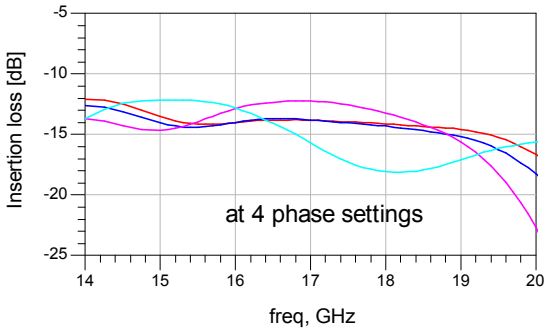

Figure 10 Inertion loss of core chip - measured

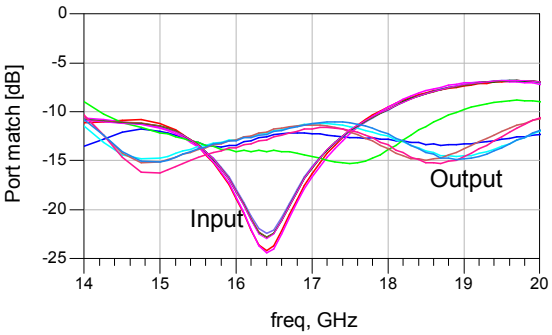

Figure 11 Port match of core chip - measured

Figure 10 shows the measured insertion loss of the core chip with different settings at the phase shifter while the attenuator was at the minimum setting. A higher than expected insertion loss was observed due to the leakages in the switch devices. This problem has been identified and a second iteration design is underway to correct it. Figure 11 shows the port match of the core chip. A worst case of 10dB was recorded at the upper end of the frequency band.

3.2 Amplifier chip

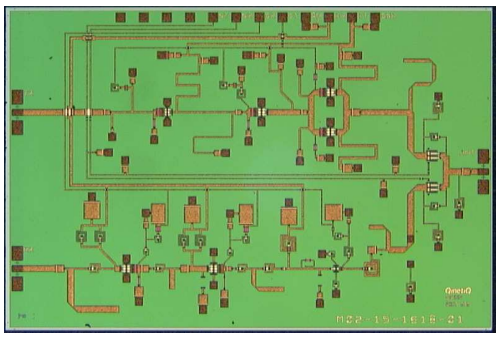

Figure 12 Micrograph of amplifier chip

A micrograph of the amplifier chip is shown in Figure 12. The aims of the amplifier chip design were to provide sufficient gain and output power to drive the antenna in the transmit mode and to provide a low noise amplification for the receive path. This chip was located in close proximity to the antenna so that there was minimum power loss at the antenna feed and minimised loss at the receiver front end to achieve optimum dynamic range of the radar T/R module. The amplifier chip therefore consisted of a medium power amplifier, an LNA and a T/R switch to switch between transmit and receive mode.

In designing the power amplifier, the prime task was to provide the required output power to drive the antenna. A three stage amplifier was designed. The gate periphery of the final stage was 0.6mm. Figure 13 showed the predicted output power of the MPA.

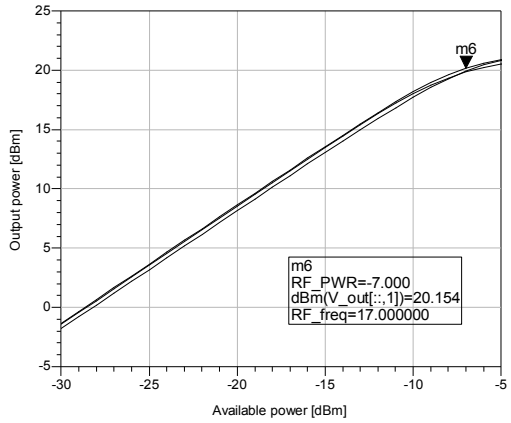

Figure 13 Simulated Output power of MPA

The measured result showed very good agreement with the predicted output power; however, it was not unconditionally stable, despite decoupling capacitors mounted close to the chip. A second iteration of the design is underway to achieve an unconditionally stable amplifier.

The design criteria for an LNA were to provide a low noise figure, high dynamic range and sufficient gain. A three stage LNA was designed with the first and second stages being designed for low noise figure and the final stage for gain. The gain and output power of the LNA is shown in Figure 14. The predicted noise figure was 2.5dB. However, due to a leakage problem at the T/R switch, the noise figure could not be measured accurately. After de-embedding, the RF on wafer noise measurement on the amplifier chip showed that the noise figure agreed with the prediction.

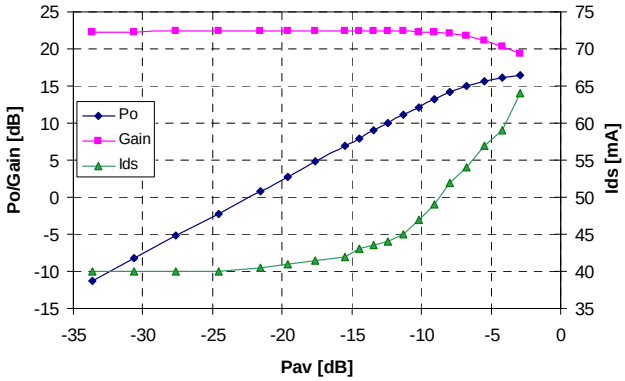

Figure 14 Measured gain and output power of LNA

4 MMIC Module

In MMIC module design, the prime aims are to provide both RF and DC connections from the outside world to the MMICs and a good thermal solution for heat dissipation. A unique T/R antenna and MMICs architecture has been investigated with the objective of achieving a low profile planar or even conformal array. This required the design of highly integrated and compact packaging to encapsulate each of the MMICs together with the radiating element to form the complete antenna.

A number of key constraints and considerations were applied during the design of the package which were summarised by the following:

- Low cost
- External size constraints (9mm x 9mm)
- Low loss RF signal performance
- RF, Control signal and bias routing
- Thermal management
- Mechanical rigidity
- Assembly and interface technology
- Provision of electrical screening

Low cost objectives were important, particularly for large sized arrays. The key factors in achieving low cost solutions are i) the choice of materials, ii) ease of assembly and iii) interface technology. The substrate materials suitable for use are LTCC and liquid crystal polymer (LCP). LCP was chosen since it offered low development cost and suitable for standard processing.

Package dimension is critical to both MMIC assembly and packaging interface technology. The size of the package is governed by the half wavelength limit. This in turn places a restriction on the space available to facilitate mounting and assembly of MMICs and to provide suitable interface technology for both RF and DC connections between the backplane and the package.

MMICs can be mounted in three ways, i) flip-chip [4], ii) direct backside interconnects technology (DBIT) [5] and iii) conventional die attached and wire bonding. Both flip-chip and DBIT are relatively new technologies that do not require wire bonding. The flip-chip technology connects MMICs directly onto the package surface using solder bumps. The disadvantage of flip-chip technology is that it does not provide any thermal path for heat dissipation since the backside of the MMIC is left unattached. DBIT provides connections at the back side of the MMIC where RF, DC bias and control signals are connected through vertical vias in the MMIC. Solder bumps are used to make connections to the package. Heat conduction can be made by additional solder bumps connected to the ground plane. The conventional method requires a ledge for wire bonding. This reduces the usable area inside the package where MMICs are mounted. Nevertheless, the direct die attach onto the metal surface provides most efficient thermal path for heat dissipation.

Since heat dissipation is important for an active array, the conventional die-attach and wire bonding technique was chosen. Wire-bonding is also a standard low risk assembly technology.

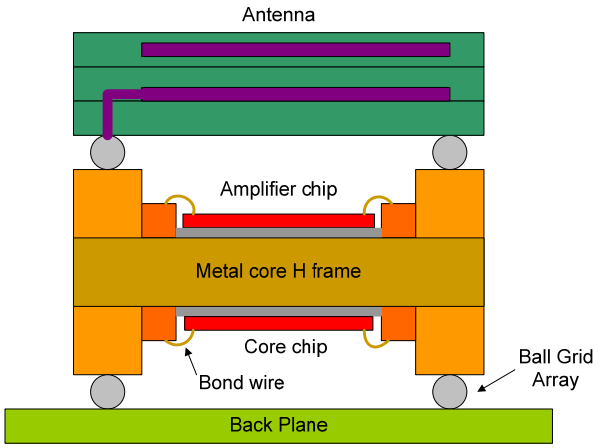

Figure 15 Schematic of MMIC module (not to scale)

Figure 15 illustrates the concept of the module construction that was based on an H-frame structure formed from multiple-layer substrate materials.

A metal core was situated at the centre of the H-frame where MMICs and decoupling capacitors were attached. The metal core layer provided the mechanical rigidity as well as the main heat-sinking element. Gold loaded epoxy was used to attach the MMICs onto the metal frame. The boundary of the H-frame was formed from several layers of substrate each having independent cut-out regions to form the wire-bonding and chip mounting regions. The base of the package contained electrical pads for each of the RF, DC bias, grounding and control signals – 34 contacts were required in total.

Ball Grid Array (BGA) technology was chosen for the package electrical interface since it provided the ability to realise a high degree of connectivity within a small confined space and also features "self-alignment" during the reflow assembly process. Vias were embedded within the H-frame for routing electrical signals. These vertical interconnects provided the connections from the base of the package to each of the MMICs. Coaxial vias were also made through the centre metal core that provided connections (including RF) through different layer levels. This process requires precision alignment since a via through the metal core was drilled initially and then back filled prior to a second drilling required for the centre conductor. The success of the package is measured by the ability to carry the RF signals between the radiating element and the backplane. The intricate interconnects were modelled by a 3D electromagnetic simulation tool from AnSoft (HFSS). This included the BGA interface and via routings. The model is shown in Figure 16.

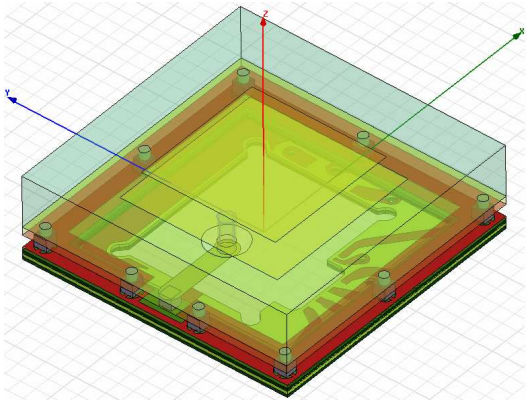

Figure 16 HFSS model of the T/R module package

To minimise interference, the outside walls of each individual module were plated for electrical screening. These platings were connected to the ground plane.

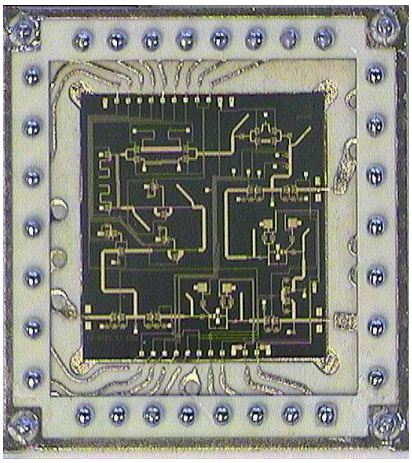

Figure 17 Photograph of MMIC module – underside

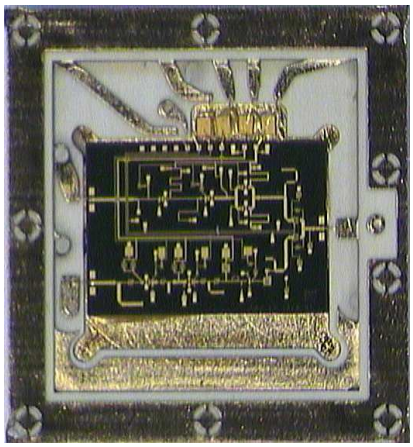

Figure 18 Photograph of MMIC module - top side

Figure 17 shows a photograph of the assembled module viewed from the underside showing the core chip mounted in place. Also evident on this photograph are the BGA solder ball contacts. Figure 18 shows a photograph of the top side of the module showing the amplifier chip in place together with contact pads for mounting the antenna.

Complete T/R modules have been built and performance has been evaluated. Measured losses within the packaging agreed with prediction. A second iteration of the module design is underway. The size of the module is less than 9x9x4 mm^3 with a weight of less than 7 grams.

A fully populated space model of antenna array populated with package only is shown in Figure 19. In this antenna, slightly less than 700 modules were populated with over 20,000 solder ball contacts. NDT showed a complete success in the self aligned BGA soldering technology. It is showed that this T/R module is suitable for future light weight SAR applications.

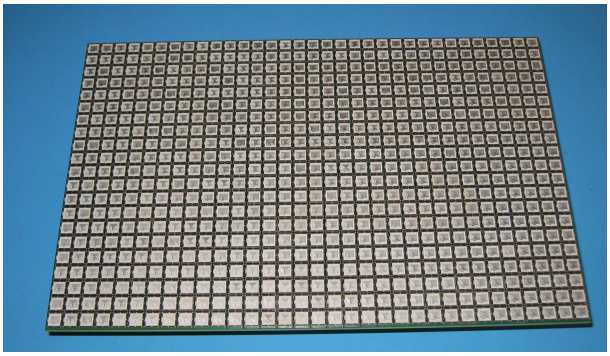

Figure 19 Photograph of a complete antenna array

5 Summary

A new light weight MMIC T/R module for a Ku band active array antenna was described. It achieved a noise figure of 2.5dB and an output power of 20dBm. Key features are high integration density, small size and low profile. Simulations and preliminary measured results were also shown. With a high level of integration and a compact design, QinetiQ has demonstrated a low profile T/R module that is suitable for light weight SAR applications.

6 Acknowledgements

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