Novel Cost-efficient Packaging Technology for High-Power LDMOS Devices

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Abstract: Packaging is crucial factor in maximizing the RF power transistors performance. Since the RF power device is the most expensive component within a high-power amplifier there is a substantial market pressure to reduce the cost of the transistor and its packaging. This paper presents a novel packaging technology which uses the high-frequency laminates as a base material replacing the currently dominant ceramic packages.

1. INTRODUCTION

For many years ceramic packages [1], [2] have been used to house the RF power transistors, due to its good thermal and electrical performance this kind of packages managed to fulfil the performance and reliability demands on RF power transistors. However, the resulting costs per package comprise a significant part of the overall price of the high-power transistor, hence, numerous developments have been undertaken in the past to develop more cost-effective packaging.

This paper presents a novel packaging technology suitable for high power applications (>30 Watts). The new package is based on high-frequency laminates, allowing for parallel simultaneous processing of several hundreds of packages, hence reducing the price per package. In addition, the employed printing board technology has low tooling costs making it viable for smaller markets.

2. PACKAGE DESCRIPTION

The employed laminates are ceramic-filled PTFE composites, which provide an excellent dielectric constant, thermal expansion and mechanical stability over a wide temperature range of -55 to 250 C°. These specifications make this board very suitable for high power applications. The package technology is demonstrated on a 30 Watt package design for LDMOS devices and is shown in Fig. 1.

The new package consists of gold plated copper heat sink with 1 *mm* thickness, a laminate frame which has been cut using laser technology to form a laminate ring which isolates the input and output leads from the electrically conductive heat sink. The laminate structure is bonded to the heat sink using FR4 film. For environmental protection, the package is capped with a lid made of the same laminate material (or any other suitable material) which in turn glued to the laminate ring and the input and output leads. The gold plated copper leads thickness is 100 μm, based on the die thickness the laminate thickness could be chosen to mate the die accordingly to reduce the required bond wire length.

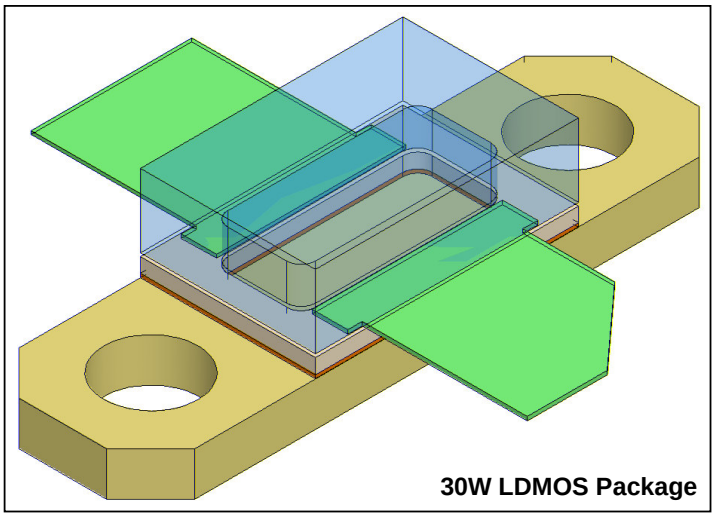

Fig. 1: HFSS Representation for 30 Watt LDMOS Package Structure.

3. EM SIMULATION

For the first evaluation of the novel package, EM simulations have been carried out. To examine the package electrical performance, a small section of the package of Fig.1 has been selected which represents either I/O ports of the package, this package section is shown in Fig.2 below. HFSS simulator was used to simulate the package RF behaviour, the package port response is shown in Fig.2 below,

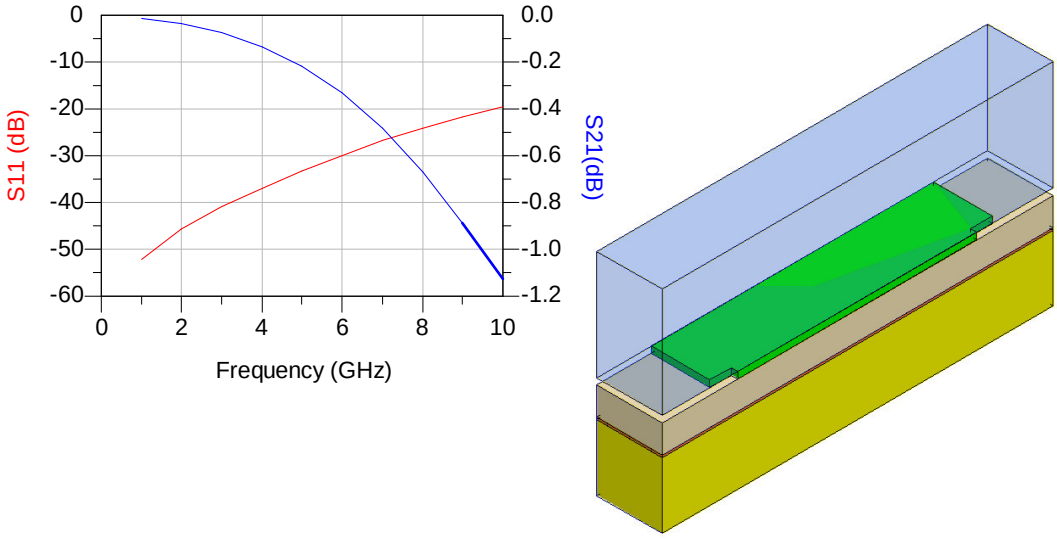

Fig. 2: HFSS Simulation on One Port Package Using RO3003 (635 μm) Laminate.

At 2.1 GHz the package EM simulation shows -45 dB return loss and -0.1 dB insertion loss normalised to 15 Ohm I/O port characteristic impedance, this response makes it a very effective package suitable for the next generation UMTS systems.

To improve the electrical performance beyond 5 GHz different laminate materials and dielectric thicknesses could be used to extend the electrical performance to higher frequency ranges.

4. THERMAL ANALYSIS

To analyze the thermal effect in the package consider the package of Fig.1, where the high power transistor die will be attached to the copper heat sink directly but due to the fact that the die temperature is concentrated on the die top surface therefore some of the heat will flow inside the package including the laminate and the lid. Therefore a good heat sink should be provided underneath the package to dissipate as much as possible of the excessive heat generated by the active device. For LDMOS device 125 C˚ is specified as the transistor operating temperature while 200 C˚ is considered to be the limit where the transistor junction will breakdown.

Therefore 200 C˚ has been chosen for simulation to represent the worse case scenario. The model of Fig.1 was simulated for its thermal behaviour, in order to observe the package thermal capabilities two thermal simulations had been performed one without the heat sink and another with the heat sink underneath the device. Fig.3a ,b shows the simulation results respectively.

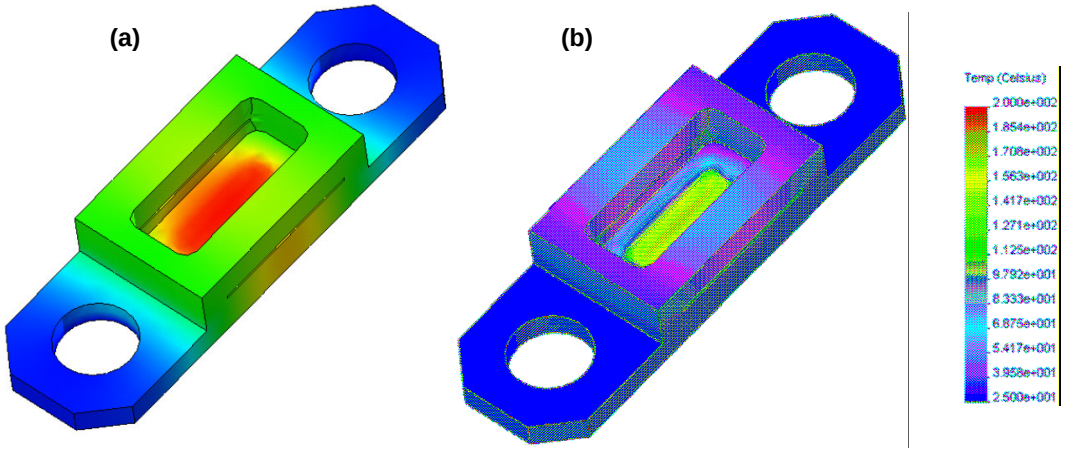

Fig. 3: High Power Package Thermal Simulation Results **a.** no Heat Sink Underneath the Device, **b.** Heat Sink Available Under the Whole Package.

The thermal resistance (R_{th}) for the package copper heat sink can be estimated [3] using $R_{th}=L/A \cdot k$ where L is the heat sink thickness (1 *mm*), A is the die area (1.15X4.55 *mm*) and *k* is the copper thermal conductivity (390 W/m·K), which gives R_{th}= 0.49 ˚C/W. Applying the same formula to a typical ceramic package, which uses a copper tungsten CuW alloy for the heat sink, gives R_{th}=0.77 ˚C/W. For this calculation of a thermal conductivity *k* = 250 W/m·K was used, which is the highest thermal conductivity for this kind of alloys.

Conclusively, the new laminate-based package reduces the thermal resistivity by approximately 35% compared to the currently utilised ceramic packages.

5. MEASUREMENT RESULTS

The package shown in Fig.1 has been manufactured by Labtech Ltd UK using RO3003 laminate and the lid was made of FR4 material, a 30 Watt Philips LDMOS device (PHILIPS ILSG4-4) was then mounted and measured. The transistor was load-pulled [4] at 2.1 GHz under class AB operation with V_{GS}=3.2V and V_{DS}=20V.

Following a comprehensive search for the optimum load impedance, it's found to be Z_{opt}=1.6-j4.7 Ohm which is very close to the specified manufacturer optimum load (1.31-j3.28 Ohm), hence confirming the good RF performance obtained from the EM

simulations. While maintaining the same optimum load impedance an input power sweep had been performed while measuring the transistor output power, efficiency and gain, the results are shown in Fig.5.a below. The same measurement procedures applied on the same device packaged using Alumina Philips package (Fig. 3.b); the optimum load for this packaged device was found to be 1.479-j4.19 Ohm.

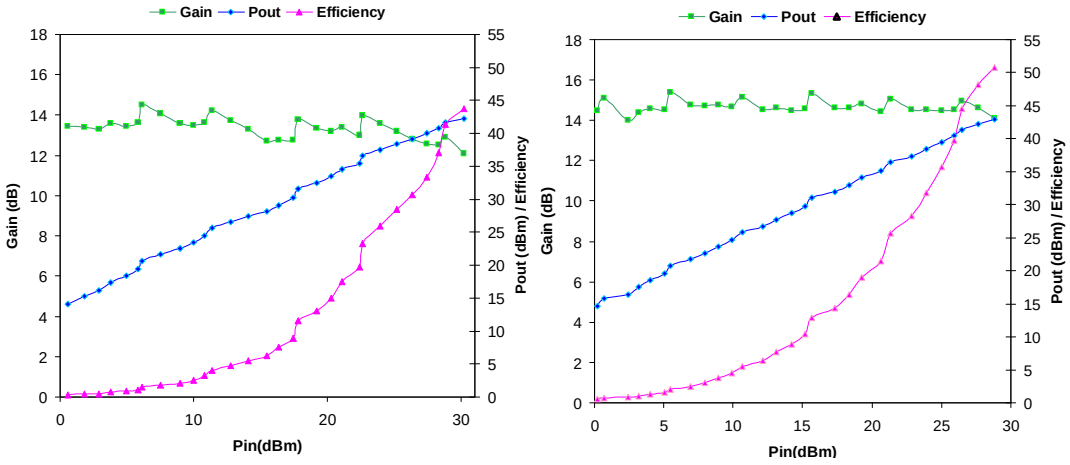

Fig 5. Pin Vs Pout, Gain and Efficiency at V_{GS}=3.2V, V_{DS}=20V, **a.** Novel Labtech Packaged Device, **b.** Philips Packaged Device.

Comparison with the measurements obtained from same device mounted into a ceramic package show similar results with the small difference in gain and efficiency being attributable to the difference in DC drain currents, approximately 200mA, between the measurements.

6. Conclusion

A novel low cost high power package design, simulation and measurement are presented in this paper. The new package offers significant cost savings compared to conventional ceramic models while maintaining an excellent electrical and thermal performance.

Acknowledgement

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