QPV2500 Family
L, H, B, BL, BQ & BQL

July 21, 2008

QPV2500 Programmable Logic Device, UV Erasable, High Speed

General Description

The QPV2500 Family features total compatibility with applications developed for the Atmel® ATV2500 family of parts. QP Semiconductor manufacturers all six variants of this product family, each one is a direct replacement for it's Atmel® counterpart.

- Logic Array with 416 product terms.
- Output Macrocells with two flip-flops per Macrocell, 48 total, 72 Sum Terms.
- Macrocell Configurations:
    - o D-type or T-Type Flip-Flops (B, BL, BQ & BQL)
    - o Direct Input Pin or Product Term Clocking
    - o Combinational or Registered Internal Feedback
- Power ConsumptionTypical
    - o QP2500L 0.5 mA
    - o QP2500H 80 mA
    - o QP2500B 110 mA
    - o QP2500BL 2 mA
    - o QP2500BQ 30 mA
    - o QP2500BQL 2 mA
- The B, BL, BQ and BQL are software compatible with their respective counterparts and are backward compatible with the L and H versions. The L and H products are compatible with their counterparts, and like their counterparts are not forward compatible with the B, BL, BQ and BQL products.

The QPV2500 family is organized with a universal single and/or array. All feedback terms and I/O pins are always available to every macrocell. Each of the 38 logic pins can be used as array inputs, along with the outputs of each flip-flop.

Four product terms are input to each sum term that can also be combined with each macrocell's three sum terms to provide up to 12 product terms per sum term. For B, BL, BQ or BQL devices, each flip-flop can be individually selected to be either a D-Type or T-Type flip-flop. 24 flip-flops may be bypassed to provide internal combinational feedback.

Product terms can provide individual clocks and asynchronous resets for each flip-flop. Flip-flops can be individually configured for direct input pin clocking. Each output has an individual enable product term. 8 synchronous preset product terms serve groups of either 4 or 8 flip-flops. Preload register functions are provided to simplify application testing. All registers are automatically "reset" upon power up.

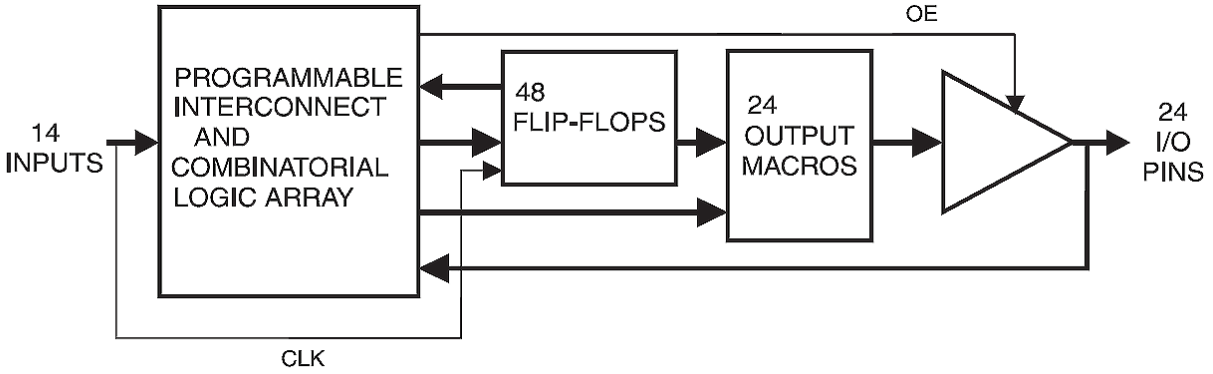
The QPV2500 family are straightforward and uniform PLDs. Macrocells are numbered from zero to 23. Each macrocell, contains 17 AND gates. All AND Gates have 172 inputs. The five lowest product terms provide AR_1, CK_1, CK_2 AR_2 and OE functionsl

Each Register can be loaded with either a one or a zero. Any state can be forced into the registers (one/H or zero/L). The preload state is accessed by placing a 10.25-10.75 Vdc level on pin 38 (DIP) or pin 42 (Chip Carrier), and then when the clock term (pin 21 – DIP / pin 23 – Chip Carrier) is pulsed high, the data on the I/O pins is loaded into the 12 registers selected by the Q select and even/odd select pins. The Register 2 observability mode is

entered by placing a 10.25 – 10.75 V signal on pin 2 (either DIP or Chip Carrier). The contents of the buried register bank will appear on the associated outputs when the OE control signals are active.

The device/family is constructed using an advanced UV CMOS wafer fab process.

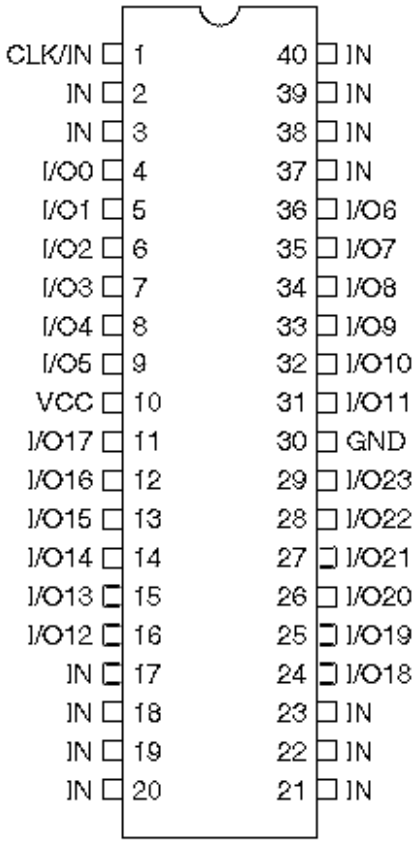
Block Diagram



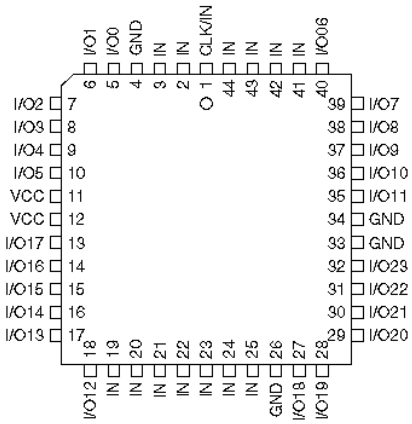
Connection Diagrams

QPV2500
B, BL, BQ & BQL

CERDIP

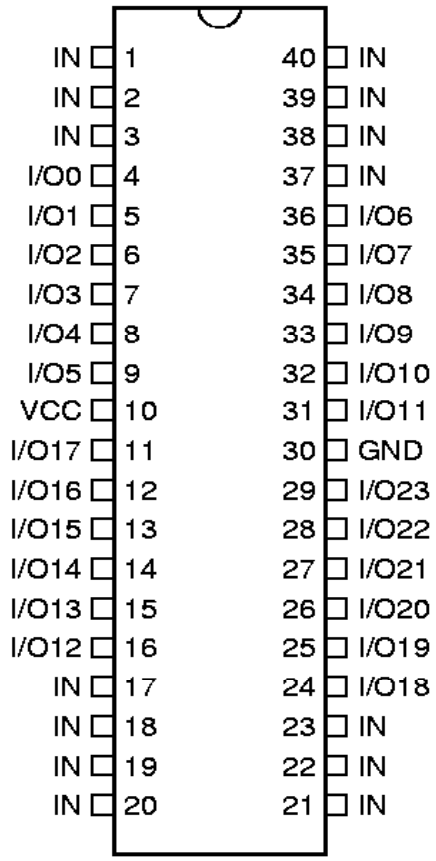


JLCC / LCC

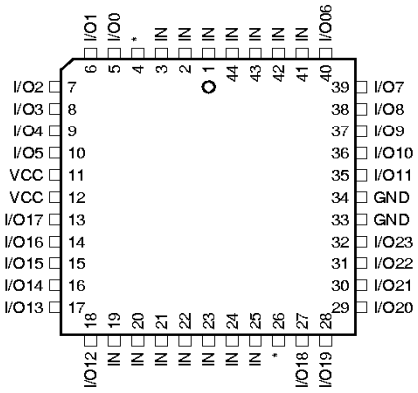


QPV2500 H & L

CERDIP



JLCC / LCC



Pins 4 and 26
Are No Connects

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Power Supply, Input or Output Pins to GND	-0.6 to +7.0	Volts DC	1/
Voltage on Input Pins to GND during programming	-0.5 to +14.0	V	1/
Programming Voltage to GND	-0.6 to +14.0	V	1/
Storage Temperature Range	-65 to +150	ºC	
Lead Temperature (soldering, 10 seconds)	+300	ºC	
Junction Temperature (T_J)	+175	ºC	

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
Input or Output Voltage Range	0.0 to V_{CC}	Volts DC	/1
Minimum High-Level Input Voltage (V_{IH})	2.0	Volts DC	
Maximum Low-Level Input Voltage (V_{IL})	0.8	Volts DC	
Maximum high level output current	-4.0	mA	
Maximum low level output current	6.0	mA	
Case Operating Range (T_c)	-55C to +125	ºC	/2

1/ – Minimum voltage may undershoot to –2.0V for less than 20ns. Maximum Voltage is V_{CC}+0.75Vdc, which may overshoot to +7.0V for less than 20ns.
2/ – Maximum PD, Maximum TJ Are Not to Be Exceeded

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Output High Voltage	V_{OH}	V_{CC} = 4.5V, V_{IL} = 0.8V V_{IH} = 2.0V, I_{OH}= -4mA	All	2.4		V
Output Low Voltage	V_{OL}	V_{CC} = 4.5V, V_{IL} = 0.8V V_{IH} = 2.0V, I_{OL}= 6mA	All		0.5	V
Tri-State Output Current 4/	I_{OZL}	VCC = 5.5V, VOUT = 0.5V	All	-10	+10	µA
(High Impedance State)	I_{OZH}	VCC = 5.5V,VOUT = 2.4V	All	-10	+10	µA
High Level Input Current	I_{IH}	V_{IH} = 5.5V	All		25	µA
		V_{IH} = 2.4V	All		10	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	All	-10		µA
		V_{IL} = 0.0V	All	-10		µA
Power Supply Standby Current	I_{CC1}	V_{CC} = 5.5V V_{IN} = GND or V_{CC} Outputs Open f = 0 MHz	2500B		210	mA
			2500H		180	mA
			2500BQ		85	mA
			2500L/BL		10	mA
			2500BQL		5	mA
Short Circuit Current	I_{OS}	V_{CC} = 5.5V, V_{OUT} = 0V Duration not to exceed 1 second, one output at a time	All	-25	-90	mA
Input Capacitance 6/ 7/	C_I	V_I = 0V, V_{CC} = 5.0V T_A = 25°C, f = 1MHz	All		20	pF
Output Capacitance 6/ 7/	C_O	V_O = 0V, V_{CC} = 5.0V T_A = 25°C, f = 1MHz	All		12	pF
Input to Output Enable	t_{EA}	V_{CC} = 4.5V C_L = 5pf R_L=580Ω►5V/280Ω►G_{ND}	2500L/ H-35		35	ns
			2500BQ/H-25		25	ns
			2500B		15	ns
			2500BL		20	ns
			2500BQL		30	ns
Input to Output Disable	t_{ER}	V_{CC} = 4.5V C_L = 5pf R_L=580Ω►5V/280Ω►G_{ND}	2500L/H-35		35	ns
			2500BQ/H-25		25	ns
			2500B		15	ns
			2500BL		20	ns
			2500BQL		30	ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Input or Feedback to Nonregistered Output	t_{PD}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500L/H-35 1-		35	ns
			2500/H-25 1-		25	ns
			2500B 2-		15	ns
			2500BL 2-		20	ns
			2500BQ 2-		25	ns
			2500BQL 2-		30	ns
Clock to Output	t_{CO}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500L/H-35 1-		35	ns
			2500H-25 1-		25	ns
			2500B 2-		15	ns
			2500BL 2-		20	ns
			2500BQ 2-		25	ns
			2500BQL 2-		30	ns
Clock Period (t_{CF} + t_{SF})	t_P	C_L = 5pf R_L=580Ω►5V/280Ω►G_{ND}	2500L/ H-35	35		ns
			2500H-25	25		ns
			2500B	17		ns
			2500BL	24		ns
			2500BQ	28		ns
			2500BQL	30		ns
Clock Pulse Width	t_w	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	15		ns
			2500H-25 1-	10		ns
			2500L 1-	17		ns
			2500B 2-	7.5		ns
			2500BL 2-	11		ns
			2500BQ 2-	14		ns
			2500BQL 2-	15		ns
Setup Time 8/ Output Register	t_{SI1}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	15		ns
			2500H-25 1-	10		ns
			2500L 1-	22		ns
			2500B 2-	5		ns
			2500BL 2-	10		ns
			2500BQ 2-	15		ns
			2500BQL 2-	19		ns
Setup Time 9/ 10/ Buried Register	t_{SI2}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	5		ns
			2500H-25 1-	5		ns
			2500L 1-	22		ns
			2500B 2-	5		ns
			2500BL 2-	10		ns
			2500BQ 2-	15		ns
			2500BQL 2-	19		ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Clock to Feedback 10/	t_{CF}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	15	20	ns
			2500H-25 1-	10	18	ns
			2500L 1-	15	20	ns
			2500B 2-	5	12	ns
			2500BL 2-	10	16	ns
			2500BQ 2-	12	18	ns
			2500BQL 2-	13	20	ns
Feedback Setup Time 10/	t_{SF}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	15		ns
			2500H-25 1-	7		ns
			2500L 1-	15		ns
			2500B 2-	5		ns
			2500BL 2-	8		ns
			2500BQ 2-	10		ns
			2500BQL 2-	10		ns
Hold Time	t_H	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	5		ns
			2500H-25 1-	5		ns
			2500B 2-	5		ns
			2500BL 2-	10		ns
			2500BQ 2-	12		ns
			2500BQL 2-	13		ns
Hold Time Output Register	t_{H1}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND}	2500L 1-	15		ns
Hold Time Buried Register	t_{H2}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND}	2500L 1-	5		ns
Maximum Clock Frequency 6/ 8/	f_{MAX}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	28		MHz
			2500H-25 1-	40		MHz
			2500L 1-	28		MHz
			2500B 2-	66		MHz
			2500BL 2-	45		MHz
			2500BQ 2-	36		MHz
			2500BQL 2-	33		MHz
Asynchronous Reset Pulse Width	t_{AW}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	20		ns
			2500H-25 1-	15		ns
			2500L 1-	20		ns
			2500B 2-	8		ns
			2500BL 2-	12		ns
			2500BQ 2-	15		ns
			2500BQL 2-	18		ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Asynchronous Reset Recovery Time	t_{AR}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-	20		ns
			2500H-25 1-	15		ns
			2500L 1-	20		ns
			2500B 2-	8		ns
			2500BL 2-	12		ns
			2500BQ 2-	15		ns
			2500BQL 2-	18		ns
Asynchronous Reset to Registered Output Reset	t_{AP}	V_{CC} = 4.5V 1- C_L = 50pf R_L=580Ω►5V/280Ω►G_{ND} 2- C_L = 35pf RL=167 Ω►2V	2500H-35 1-		35	ns
			2500H-25 1-		25	ns
			2500L 1-		35	ns
			2500B 2-		18	ns
			2500BL 2-		22	ns
			2500BQ 2-		28	ns
			2500BQL 2-		30	ns
Clock to Output, Input Pin Clock	t_{COS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		10	ns
			2500BL 2-		11	ns
			2500BQ 2-		12	ns
			2500BQL 2-		15	ns
Clock to Feedback, Input Pin Clock 10/	t_{CFS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	0	5	ns
			2500BL 2-	0	6	ns
			2500BQ 2-	0	7	ns
			2500BQL 2-	0	8	ns
Input Setup Time, Input Pin Clock	t_{SIS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	9		ns
			2500BL 2-	14		ns
			2500BQ 2-	20		ns
			2500BQL 2-	23		ns
Feedback Setup Time, Input Pin Clock 10/	t_{SFS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	9		ns
			2500BL 2-	14		ns
			2500BQ 2-	20		ns
			2500BQL 2-	23		ns
Hold Time, Input Pin Clock	t_{HS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	0		ns
			2500BL 2-	0		ns
			2500BQ 2-	0		ns
			2500BQL 2-	0		ns
Clock Width, Input Pin Clock	t_{WS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	6		ns
			2500BL 2-	7		ns
			2500BQ 2-	8		ns
			2500BQL 2-	9		ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions 3/ -55ºC≤TA≤+125ºC, V_{SS}=0V 4.5V ≤ V_{CC} ≤ 5.5V Unless Otherwise Specified	Device	Min	Max	Unit
Clock Period, Input Pin Clock	t_{PS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	12		ns
			2500BL 2-	14		ns
			2500BQ 2-	16		ns
			2500BQL 2-	18		ns
Maximum Clock Frequency Input Pin Clock	f_{MAXS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		83	MHz
			2500BL 2-		71	MHz
			2500BQ 2-		62	MHz
			2500BQL 2-		55	MHz
Asynchronous Reset/, Preset Recovery Time, Input Pin Clock	t_{ARS}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-	12		ns
			2500BL 2-	15		ns
			2500BQ 2-	20		ns
			2500BQL 2-	25		ns
Feedback to Non-Registered Output 10/	T_{PD2}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		15	ns
			2500BL 2-		20	ns
			2500BQ 2-		25	ns
			2500BQL 2-		30	ns
Input to Non-Registered Feedback 10/	T_{PD3}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		11	ns
			2500BL 2-		15	ns
			2500BQ 2-		18	ns
			2500BQL 2-		20	ns
Feedback to Non-Registered Feedback 10/	T_{PD4}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		11	ns
			2500BL 2-		15	ns
			2500BQ 2-		18	ns
			2500BQL 2-		20	ns
Feedback to Output Enable 10/	T_{EA2}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		15	ns
			2500BL 2-		20	ns
			2500BQ 2-		25	ns
			2500BQL 2-		30	ns
Feedback to Output Disable 10/	T_{ER2}	V_{CC} = 4.5V 2- C_L = 35pf RL=167 Ω►2V	2500B 2-		15	ns
			2500BL 2-		20	ns
			2500BQ 2-		25	ns
			2500BQL 2-		30	ns

NOTES

3/ All voltages are referenced to ground.
4/ I/O terminal leakage is the worst case of IIX or IOZ.
5/ Only one output shorted at a time.
6/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
7/ All pins not being tested are to be open.
8/ Test applies only to register outputs.

9/ Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinational.

10/Values guaranteed by design and are not tested.

Programming Characteristics

The QPV2500 family of devices program identically to the Atmel® series of parts in their matching family of products. This allows applications developed for the mating Atmel® device to be used "as-is". To program the QP Semiconductor device use a good quality third party programming (QP Semiconductor uses the Data I/O Unisite family of programmers), select the appropriate programming algorithm by selecting "Atmel" as the device manufacturer and then 2500H, 2500L, 2500B, 2500BL, 2500BQ or 2500BQL (depending on the QP device being programmed) along with the package style if appropriate.

Erasure Characteristics

The memory array of the QP2500 family can be erased when exposed to ultraviolet light. Erasure requires a minimum of 20 minutes exposure to a light of 2537Å wavelength using 12,000 μW/cm^2 intensity lamps spaced 1" away from the integrated circuit (for windowed products only). The erasure time can be calculated from the minimum integrated dose of 15 Wsec/cm^2. To prevent accidental erasure, an opaque label cover for the clear "window" on any UV erasable product is recommended. This is especially critical for any windowed part that will be subjected to long term exposure(s) to fluorescent lighting or sunlight.

Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
5962-9154501MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-35DM/883
5962-9154501MXA	LCC - CQCC1-N44	QPV2500H-35LM/883
5962-9154501MYA	J-Leaded Chip Carrier	QPV2500H-35KM/883
5962-9154502MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-25DM/883
5962-9154502MXA	LCC - CQCC1-N44	QPV2500H-25LM/883
5962-9154502MYA	J-Leaded Chip Carrier	QPV2500H-25KM/883
5962-9154503MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500L-30DM/883
5962-9154503MXA	LCC - CQCC1-N44	QPV2500L-30LM/883
5962-9154503MYA	J-Leaded Chip Carrier	QPV2500L-30KM/883
5962-9154504MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500B-15DM/883
5962-9154504MXA	LCC - CQCC1-N44	QPV2500B-15LM/883
5962-9154504MYA	J-Leaded Chip Carrier	QPV2500B-15KM/883
5962-9154505MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BL-20DM/883
5962-9154505MXA	LCC - CQCC1-N44	QPV2500BL-20LM/883
5962-9154505MYA	J-Leaded Chip Carrier	QPV2500BL-20KM/883
5962-9154506MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQ-25DM/883
5962-9154506MXA	LCC - CQCC1-N44	QPV2500BQ-25LM/883
5962-9154506MYA	J-Leaded Chip Carrier	QPV2500BQ-25KM/883
5962-9154507MQA	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQL-30DM/883
5962-9154507MXA	LCC - CQCC1-N44	QPV2500BQL-30LM/883
5962-9154507MYA	J-Leaded Chip Carrier	QPV2500BQL-30KM/883
QPV2500B-15DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500B-15DC
QPV2500B-15KC	J-Leaded Chip Carrier	QPV2500B-15KC
QPV2500B-15DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500B-15DI
QPV2500B-15KI	J-Leaded Chip Carrier	QPV2500B-15KI
QPV2500BL-20DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BL-20DC
QPV2500BL-20KC	J-Leaded Chip Carrier	QPV2500BL-20KC
QPV2500BL-20DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BL-20DI
QPV2500BL-20KI	J-Leaded Chip Carrier	QPV2500BL-20KI
QPV2500BQ-25DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQ-25DC
QPV2500BQ-25KC	J-Leaded Chip Carrier	QPV2500BQ-25KC
QPV2500BQ-25DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQ-25DI
QPV2500BQ-25KI	J-Leaded Chip Carrier	QPV2500BQ-25KI
QPV2500BQL-30DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQL-30DC
QPV2500BQL-30KC	J-Leaded Chip Carrier	QPV2500BQL-30KC
QPV2500BQL-30DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500BQL-30DI
QPV2500BQL-30KI	J-Leaded Chip Carrier	QPV2500BQL-30KI
QPV2500H-35DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-35DC
QPV2500H-35KC	J-Leaded Chip Carrier	QPV2500H-35KC
QPV2500H-35DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-35DI
QPV2500H-35KC	J-Leaded Chip Carrier	QPV2500H-35KC
QPV2500H-25DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-25DC
QPV2500H-25KC	J-Leaded Chip Carrier	QPV2500H-25KC
QPV2500H-25DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500H-25DI
QPV2500H-25KI	J-Leaded Chip Carrier	QPV2500H-25KI
QPV2500L-30DC	DIP -GDIP1-T40 or CDIP2-T40	QPV2500L-30DC
QPV2500L-30KC	J-Leaded Chip Carrier	QPV2500L-30KC
QPV2500L-30DI	DIP -GDIP1-T40 or CDIP2-T40	QPV2500L-30DI
QPV2500L-30KI	J-Leaded Chip Carrier	QPV2500L-30KI

QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

"-MIL" products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com