

# SN54F533, SN74F533 OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

D2932, MARCH 1987—REVISED JANUARY 1989

- 8-Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

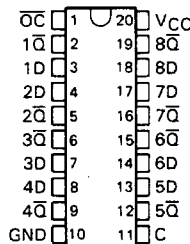
The eight latches of the 'F533 are transparent D-type latches. While the enable (C) is high, the  $\bar{Q}$  outputs will follow the complements of the D inputs. When the enable is taken low, the  $\bar{Q}$  outputs will be latched at the inverses of the levels that were set up at the D inputs. The 'F533 is functionally equivalent to the 'F373 except for having inverted outputs.

A buffered output-control ( $\bar{OC}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

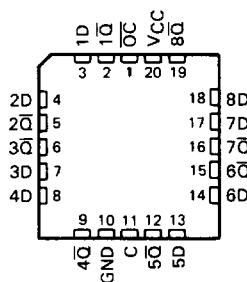
The output control does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54F533 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74F533 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54F533 . . . J PACKAGE  
SN74F533 . . . DW OR N PACKAGE  
(TOP VIEW)



SN54F533 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE (EACH LATCH)

$\bar{OC}$	INPUTS			OUTPUT
	ENABLE C	D		$\bar{Q}$
L	H	H		L
L	H	L		H
L	L	X		$\bar{Q}_0$
H	X	X		Z

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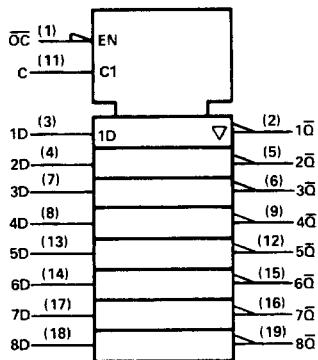


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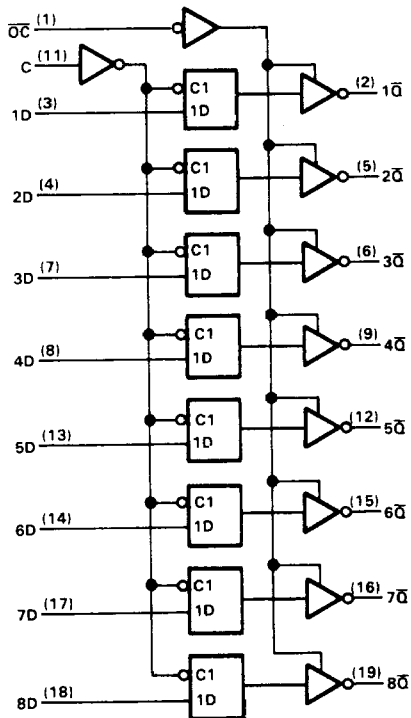
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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## absolute maximum ratings over operating free-air temperature range

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage† .....	-1.2 V to 7 V
Input current .....	-30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state .....	-0.5 V to 5.5 V
Voltage applied to any output in the high state .....	-0.5 to $V_{CC}$
Current into any output in the low state: SN54F533 .....	40 mA
SN74F533 .....	48 mA
Operating free-air temperature range: SN54F533 .....	-55°C to 125°C
SN74F533 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

	SN54F533			SN74F533			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$I_{IK}$ Input clamp current			-18			-18	mA
$I_{OH}$ High-level output current			-3			-3	mA
$I_{OL}$ Low-level output current			20			24	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F533			SN74F533			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V	$I_{OH} = -1$ mA	2.5	3.4	2.5	3.4		V
		$I_{OH} = -3$ mA	2.4	3.3	2.4	3.3		
	Any output $V_{CC} = 4.75$ V	$I_{OH} = -1$ mA to -3 mA			2.7			
$V_{OL}$	$V_{CC} = 4.5$ V	$I_{OL} = 20$ mA	0.3	0.5				V
		$I_{OL} = 24$ mA			0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	μA
$I_{OZL}$	$V_{CC} = 5.5$ V, $V_O = 0.5$ V			-50			-50	μA
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			20	μA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			-0.6			-0.6	mA
$I_{OS}^{\S}$	$V_{CC} = 5.5$ V, $V_O = 0$			-60			-150	mA
$I_{CCZ}$	$V_{CC} = 5.5$ V, See Note 1			41			61	mA

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V,  $T_A = 25$ °C.

<sup>§</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 1:  $I_{CCZ}$  is measured with  $\overline{OC}$  at 4.5 V, all other inputs grounded.

**SN54F533, SN74F533**  
**OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS**

**timing requirements**

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		V <sub>CC</sub> = 4.5 V to 5.5 V, T <sub>A</sub> = MIN to MAX†				UNIT
		'F533		SN54F533		SN74F533		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>su</sub>	Setup time before enable C↓ Data high or low	2		2		2		ns
t <sub>h</sub>	Hold time after enable C↓ Data high or low	3		3		3		ns
t <sub>w</sub>	Pulse duration Enable C high	6		6		6		ns

**switching characteristics (see Note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			'F533			SN54F533		SN74F533		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Any $\bar{Q}$	3.2	6.5	9	3.2	12	3.2	10	ns
t <sub>PHL</sub>			2.2	4.8	7	2.2	9	2.2	8	
t <sub>PLH</sub>	C	Any $\bar{Q}$	4.2	8.1	11	4.2	14	4.2	13	ns
t <sub>PHL</sub>			2.2	5.2	7	2.2	9	2.2	8	
t <sub>PZH</sub>	$\bar{OC}$	Any $\bar{Q}$	1.2	7.3	10	1.2	12.5	1.2	11	ns
t <sub>PZL</sub>			1.2	4.7	6.5	1.2	9	1.2	7.5	
t <sub>PHZ</sub>	$\bar{OC}$	Any $\bar{Q}$	1.2	4.3	6	1.2	8.5	1.2	7	ns
t <sub>PLZ</sub>			1.2	3.7	5.5	1.2	7.5	1.2	6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

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Data Sheets