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Product Specification

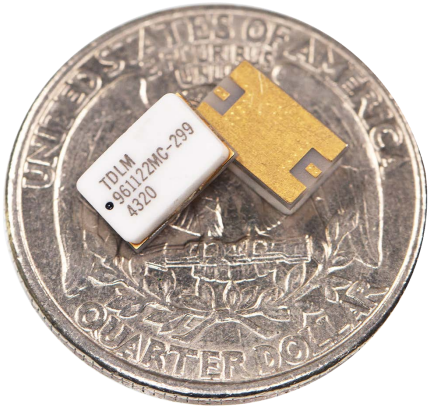
March 2021

TDLM961122MC-299

High Power ARNS/IFF Limiter Module: Ultra Low Flat Leakage & Fast Recovery Time

Features

- SMT Limiter Module: 8 mm x 5 mm x 2.5 mm
- Frequency Range: 960 MHz to 1,215 MHz
- High Average Power Handling: +48 dBm
- High Peak Power Handling: +60 dBm
- Low Insertion Loss: < 0.4 dB
- Return Loss: > 15 dB
- Flat Leakage @ +30 dBm Input: < 12 dBm
- Flat Leakage @ +60 dBm Input: < 14 dBm
- Low Spike Energy Leakage: < 0.5 ergs
- Ultra Fast Recovery Time: < 200 nsec
- dc Blocking Capacitors
- RoHS Compliant



Description

The TDLM961122MC-299 SMT Silicon PIN Diode Limiter Module offers “Always On” High Power CW and Peak protection in the Aeronautical Radio Navigation Service (ARNS)/ Identification Friend or Foe (IFF) frequency range of 960 MHz to 1,215 MHz. This Limiter Module is based on proven hybrid assembly technique utilized extensively in high reliability, mission critical applications for several decades. The TDLM961122MC-299 offers excellent thermal characteristics in a compact, low profile 8 mm x 5 mm x 2.5 mm package. It was designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large signal protection and exceptionally low Flat Leakage for effective receiver protection in the ARNS/IFF frequency range.

The TDLM961122MC-299 Limiter Module provides outstanding passive receiver protection (Always On) which protects against high average power up to +48 dBm @ T_{case}=+85 °C, High Peak Power up to +60 dBm (Peak) Pulse Width = 1 µsec, Pulse Repetition Rate = 1%, T_{case}=+85 °C, while maintaining low flat leakage to less than 14 dBm (typ), and reduces Spike Leakage to less than 0.5 ergs (typ).

ESD and Moisture Sensitivity Rating

The TDLM961122MC-299 Limiter Module carries a Class 1C ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The proprietary design methodology minimizes the thermal resistance from the coarse stage shunt limiter diode junction to base plate. This three stage passive limiter design employs a very sensitive detector circuit which enables ultra-fast turn on of both the intermediate and coarse stages. This circuit topology coupled with the thermal characteristic of the substrate design enables the Limiter Module to reliably handling High Input RF Power up to +48 dBm CW and RF Peak Power levels up to +60 dBm (1 µsec pulse width @ 1.0% duty cycle) with base plate temperature at +85 °C. The TDLM961122MC-299 is based on a substrate designed to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat corrosion.

Absolute Maximum Ratings

@ Z_o = 50 Ω, T_A = +25 °C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65 °C to 125 °C
Storage Temperature		-65 °C to 150 °C
Junction Temperature		175 °C
Assembly Temperature	T = 30 seconds	260 °C
RF Peak Incident Power	T_{CASE} = 85 °C, source and load VSWR < 1.2:1, RF Pulse width = 1 µsec, duty cycle = 1%, derated linearly to 0 W at T_{CASE}=150 °C (note 1)	+60 dBm
RF CW Incident Power	T_{CASE}=+85 °C, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE}=150 °C (note 1)	+48 dBm
RF Input & Output DC Block Capacitor Voltage Breakdown		100 V DC

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

TDLM961122MC-299 Electrical Specifications

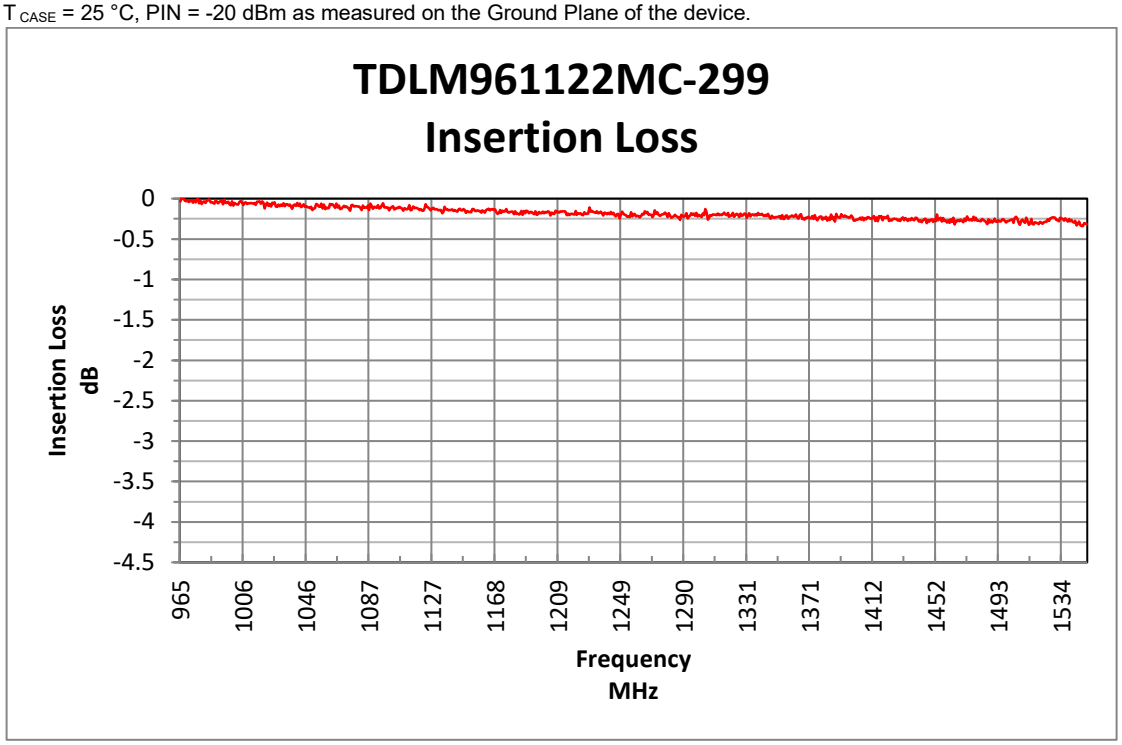
@ Z_o = 50 Ω, TA = +25 °C as measured on the base ground surface of the device.

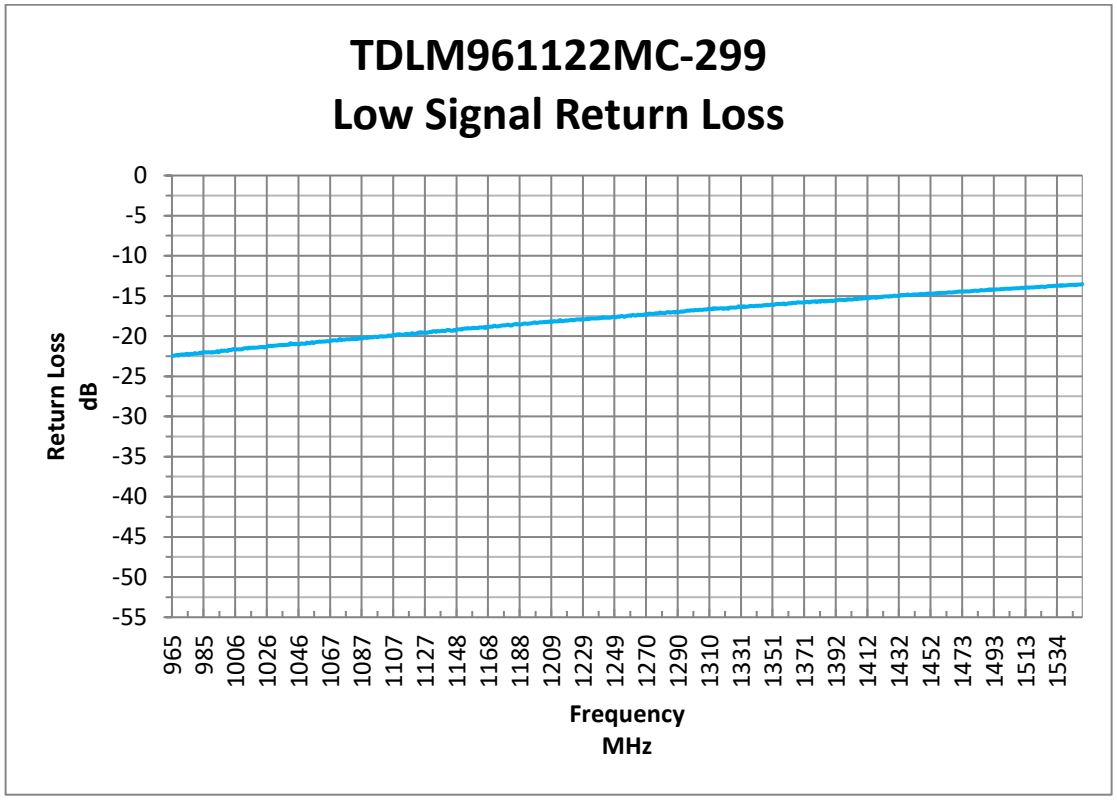
Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	960 MHz ≤ F ≤ 1,215 MHz	960		1,215	MHz
Insertion Loss	IL	960 MHz ≤ F ≤ 1,215 MHz, P_{in}= -10 dBm		0.3	0.4	dB
Insertion Loss	IL	F = 1,090 MHz, P_{in} = -10 dBm		0.3	0.4	dB
IL Rate of Change vs Operating Temperature /1	ΔIL	960 MHz ≤ F ≤ 1,215 MHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	960 MHz ≤ F ≤ 1,215 MHz, Pin = -10 dBm	15			dB
Return Loss	RL	F = 1,090 MHz, Pin = -10dBm	16			dB
Input 1 dB Compression Point	IP_{1dB}	960 MHz ≤ F ≤ 1,215 MHz	0	8	16	dBm
Peak Incident Power /1	$P_{inc\ (PK)}$	RF Pulse = 1 µsec, duty cycle = 1%			+60	dBm
CW Incident Power /1	$P_{inc(CW)}$	960 MHz ≤ F ≤ 1,215 MHz; T_{case} = +85 °C			+48	dBm
Flat Leakage /1	FL	P_{in} = +30 dBm, RF Pulse width = 1 µs, duty cycle = 1%			12	dBm
Flat Leakage /1	FL	P_{in} = +60 dBm, RF Pulse width = 1 µs, duty cycle = 1%			14	dBm
Spike Leakage /1	SL	Pin = +60 dBm, RF Pulse Width = 1 µs, duty cycle = 1%			0.5	erg
Recovery Time /1	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = +60 dBm peak, RF PW = 1 us, duty cycle = 1%		100	200	nsec

Note /1: Guaranteed by characterization.

TDLM961122MC-299 Typical Performance

Z_o = 50 Ω, T_{CASE} = 25 °C, PIN = -20 dBm as measured on the Ground Plane of the device.



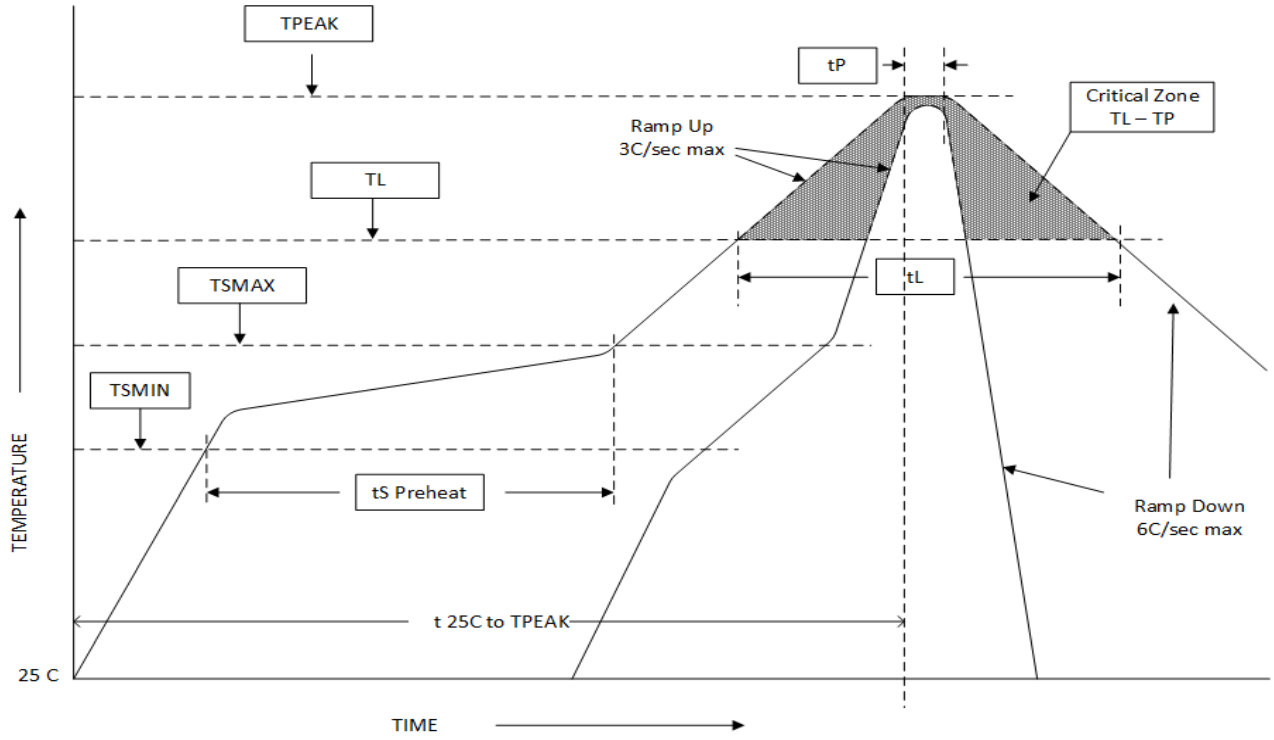


Assembly Instructions

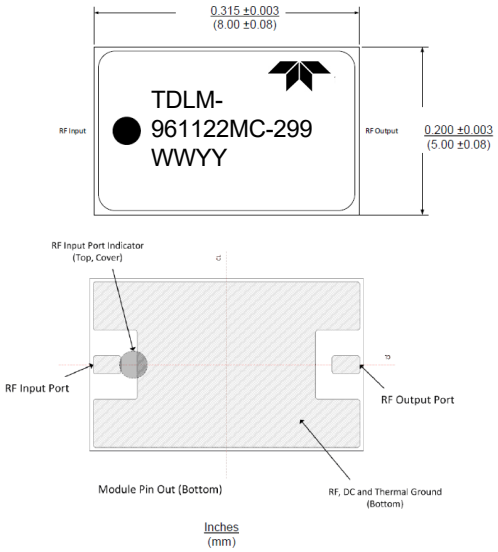
The TDLM961122MC-299 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3 °C/sec (max)	3 °C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100 °C 150 °C 60 – 120 sec	 100 °C 150 °C 60 – 180 sec
T_{smax} to T_L Ramp up Rate	 	 3 °C/sec (max)
Peak Temp (T_P)	225 °C +0°C / -5 °C	260 °C +0 °C / -5 °C
Time within 5 °C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183 °C 60 to 150 sec	 217 °C 60 to 150 sec
Ramp Down Rate	6 °C/sec (max)	6 °C/sec (max)
Time 25 °C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



TDLM961122MC-299 Limiter Module Package Outline Drawing



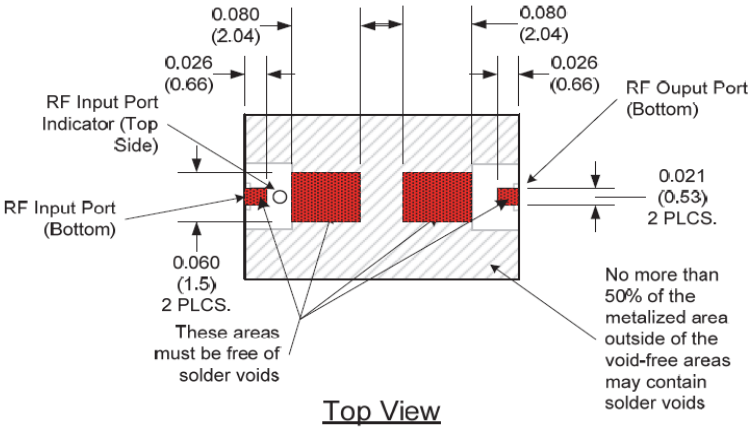
Notes:

1) Plain surface is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).
3) Unit = mils

Thermal Design Considerations:

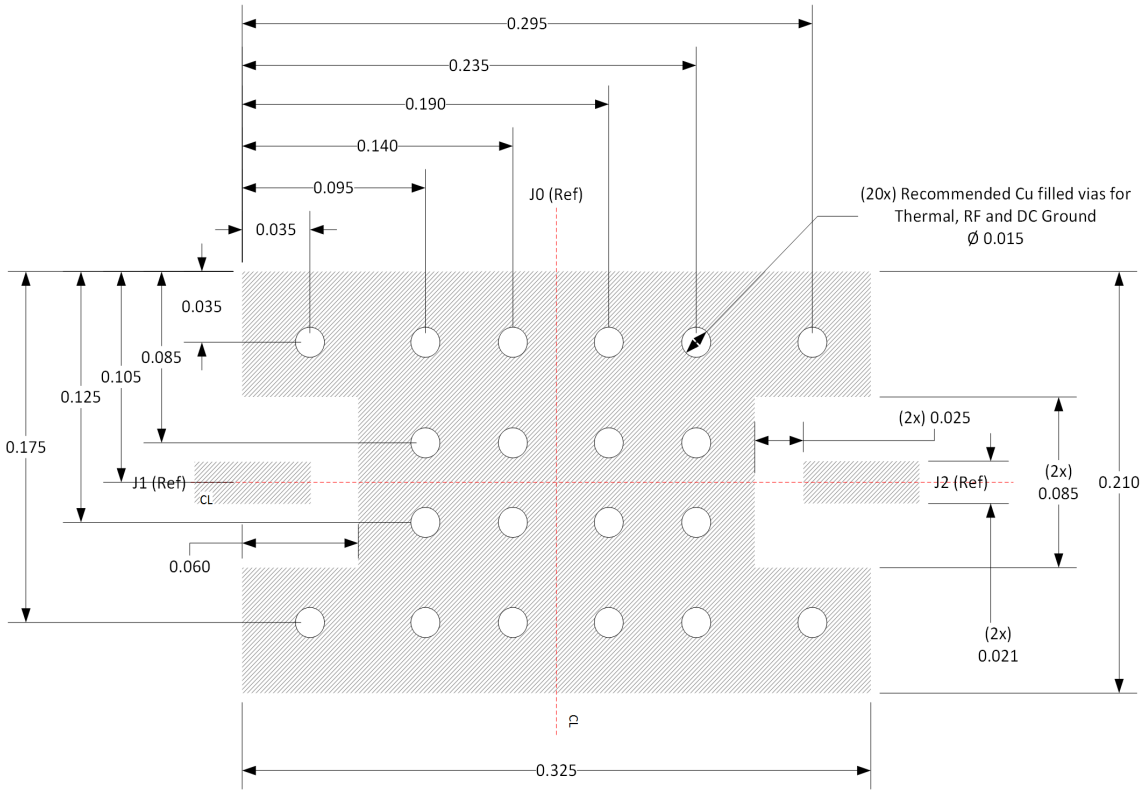
The design of the TDLM961122MC-299 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 85 °C.

There must be a minimal thermal and electrical resistance between the limiter module and ground. Adequate thermal management is required to maintain a Tjc at less than +175 °C and thereby avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.



Dimensions in inches (mm).

Recommended RF Circuit Solder Footprint for the TDLM961122MC-299



Notes:

1) Recommended PCB material is Rogers 4350B, 20 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
2) Plain surface is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.
3) Unit = mils

Part Number Ordering Detail:

The TDLM961122MC-299 Limiter Module is available in the following shipping formats:

Part Number	Description	Packaging
TDLM961122MC-299-EVK	TDLM961122MC-299 Evaluation Kit	1/Box
TDLM961122MC-299	IFF Band Limiter - Input & Output DC Blocking Caps	Gel Packs

Contact Information

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