

# TDLM06100

Document Category: Product Specification

*RF Power Limiter, 10 MHz–6 GHz*

## Features

- Monolithic drop-in solution with no external bias components
- Adjustable low power limiting threshold from +7 dBm to +13 dBm
- High maximum power handling of 50 dBm, 100 W pulsed
- Positive threshold control from +0 V to +0.3 V
- Fast response time of less than 1 ns
- Packaging – 24-pad 4 × 4 × 0.85 mm CLGA
- Qualified for use in harsh environments

## Applications

- Satellite transceivers and antennas
- Sensitive orbital T/R Modules
- Radar

## Product Description

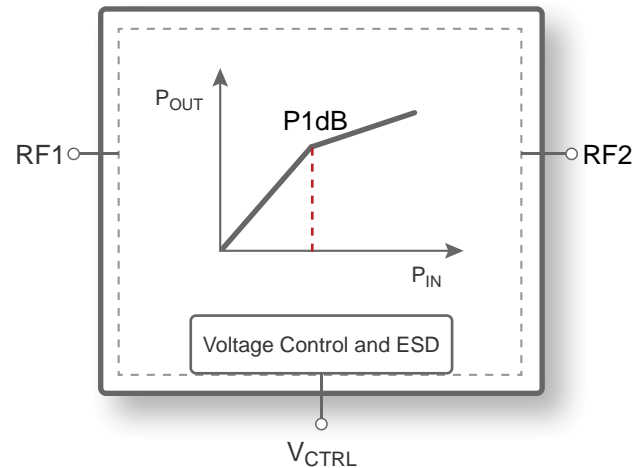
The TDLM06100 is a RF power limiter qualified for operating in harsh environments, including military, space, avionics and medical applications.

Unlike traditional PIN diode solutions, the TDLM06100 achieves an adjustable input 1dB compression point or limiting threshold via a low current control voltage ( $V_{CTRL}$ ), eliminating the need for external bias components such as DC blocking capacitors, RF choke inductors and bias resistors.

It delivers low insertion loss and high linearity under non-limiting power levels and extremely fast response time in a limiting event, ensuring protection of sensitive circuitry. It also offers excellent ESD rating and ESD protection.

The TDLM06100 is a monolithic solution manufactured on a ruggedized process offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1 • TDLM06100 Functional Diagram



## Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

## ESD Precautions

When handling this device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

## Latch-up Immunity

The TDLM06100 is immune to latch-up.

**Table 1 • Absolute Maximum Ratings for TDLM06100**

Parameter/Condition	Min	Max	Unit
Control voltage, $V_{CTRL}$ Power limiting mode	0	3.6	V
RF input power, Pulsed <sup>(1)</sup>		50	dBm
Storage temperature range	-65	+150	°C
ESD voltage HBM, all pins <sup>(2)</sup>		7000	V
ESD voltage CDM, all pins <sup>(3)</sup>		2000	V
<b>Notes:</b> 1) Pulsed, 1.0% duty cycle of 10 $\mu$ s pulse width in 1 ms period, 50 $\Omega$ at +25 °C. 2) Human body model (MIL-STD 883 Method 3015). 3) Charged device model (JEDEC JESD22-C101).			

## Recommended Operating Conditions

**Table 2** lists the recommended operating conditions for the TDLM06100. Devices should not be operated outside the operating conditions listed below.

**Table 2 • Recommended Operating Conditions for TDLM06100**

Parameter	Min	Typ	Max	Unit
Control voltage, $V_{CTRL}$				
Power limiting mode	0		+0.3	V
Power reflecting mode	0		+3.0	V
RF input power, CW(*)			<b>Fig. 2</b>	dBm
Operating temperature range ( $T_{ambient} = T_A$ )	-55	+25	+105	°C
Operating max junction temperature			+150	°C
<b>Note: * See Fig. 2.</b>				

## Electrical Specifications

Table 3 provides the TDLM06100 key electrical specifications at -55 °C to +105 °C ( $Z_S = Z_L = 50\Omega$ ), unless otherwise specified.

Table 3 • TDLM06100 Electrical Specifications

Parameter	Condition	Min	Typ	Max	Unit
Operation frequency		10 MHz		6 GHz	As shown
<b>Power limiting mode</b>					
Insertion loss	10 MHz–3 GHz		0.87	1.10	dB
	3–6 GHz		1.20	1.50	dB
Return loss	10 MHz–3 GHz	$T_A = +25\text{ }^\circ\text{C}$	22		dB
	3–6 GHz		12		dB
P1dB/limiting threshold	Gain compression with $V_{CTRL} = +0V @ 915\text{ MHz}$ , $P_{in} = +12\text{ dBm}$			1.1	dB
	the input conditions $V_{CTRL} = +0.15V @ 915\text{ MHz}$ , $P_{in} = +9\text{ dBm}$			1.1	dB
	shown to the right: $V_{CTRL} = +0.3V @ 915\text{ MHz}$ , $P_{in} = +6\text{ dBm}$			1.1	dB
Leakage power <sup>(1)</sup>	$V_{CTRL} = 0V @ 915\text{ MHz}$		14.6	15.5	dBm
	$V_{CTRL} = +0.15V @ 915\text{ MHz}$		13.6	14.5	dBm
	$V_{CTRL} = +0.3V @ 915\text{ MHz}$		12.1	13.3	dBm
Input IP2	$V_{CTRL} = 0V @ 915\text{ MHz}$	$T_A = +25\text{ }^\circ\text{C}$	88		dBm
	$V_{CTRL} = 0V @ 6\text{ GHz}$		70		dBm
Input IP3	$V_{CTRL} = 0V @ 915\text{ MHz}$	$T_A = +25\text{ }^\circ\text{C}$	37		dBm
	$V_{CTRL} = 0V @ 6\text{ GHz}$		31		dBm
Response time	1 GHz	$T_A = +25\text{ }^\circ\text{C}$	0.6		ns
Recovery time <sup>(4)</sup>	1 GHz, $P_{IN}$ , Pulse = 30 dBm	$T_A = +25\text{ }^\circ\text{C}$	1.0		ns
<b>Power reflecting mode<sup>(2)</sup></b>					
Leakage power <sup>(1)</sup>	$V_{CTRL} = +3.0V @ 915\text{ MHz}$		-36.6	-24.0	dBm
Switching time <sup>(3)</sup>	State change to 10% RF	$T_A = +25\text{ }^\circ\text{C}$	2.7		$\mu\text{s}$
<b>Notes:</b>					
1) Measured with +30 dBm CW applied at input.					
2) This mode requires the control voltage to toggle between +3.0V and 0V. At +3.0V, the limiter equivalent circuit is a low impedance to ground, reflecting most of the incident power back to the source.					
3) State change is $V_{CTRL}$ toggle from 0V to +3.0V.					
4) Pulsed, 1% duty cycle of 10 $\mu\text{s}$ pulse width in 1 ms period, 50 $\Omega$ @ +25 °C.					

## Thermal Data

Psi-JT ( $\Psi_{JT}$ ), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

where

$\Psi_{JT}$  = junction-to-top of package characterization parameter, °C/W

$T_J$  = die junction temperature, °C

$T_T$  = package temperature (top surface, in the center), °C

$P$  = power dissipated by device, Watts

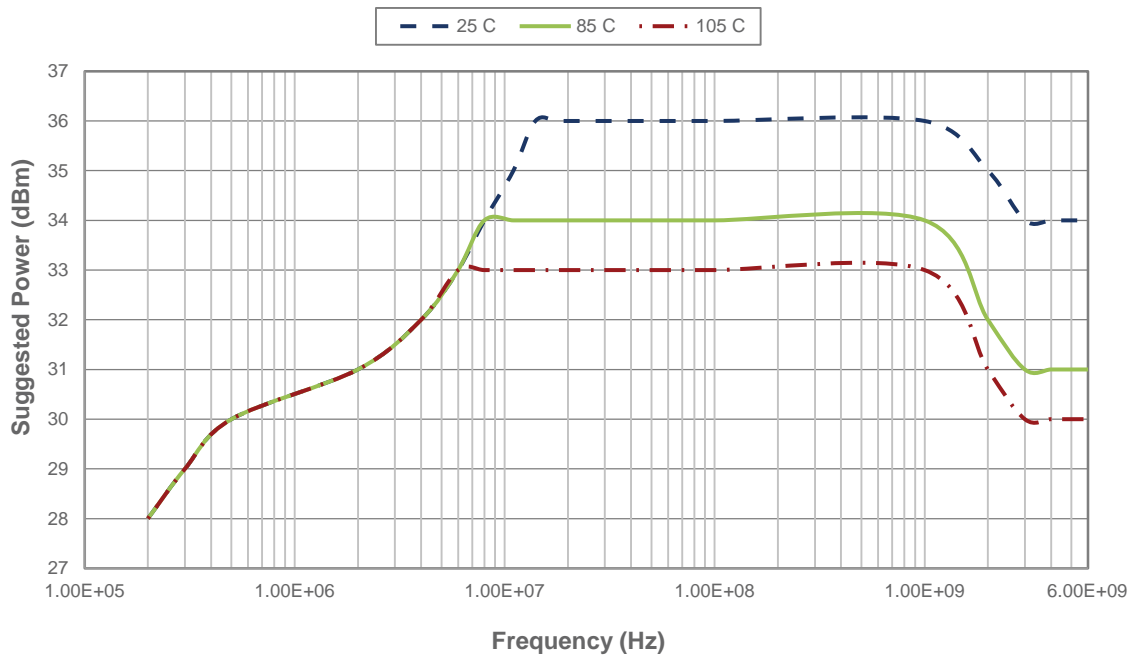
Table 4 • Thermal Data for TDLM06100

Parameter	Typ	Unit
$\Psi_{JT}$	35	°C/W
$\Theta_{JA}$ , junction-to-ambient thermal resistance	73	°C/W

## Power De-rating Curve

Figure 2 shows the power de-rating curve indicating maximum allowable operating RF input power (CW) up to the part's maximum operating ambient temperature of +105 °C. This RF input power maintains the maximum operating junction temperature requirement of +150 °C.

Figure 2 • Power De-rating Curve, 10 MHz–6 GHz, +25 °C to +105 °C Ambient, CW, 50Ω<sup>(\*)</sup>



Note: \* High frequency CW power handling can be improved with 0.30pF capacitive matching on input and output RF ports.

## Dual Mode Operation

### Power Limiting Mode

The TDLM06100 performs as a linear power limiter with adjustable P1dB/limiting threshold. The P1dB/limiting threshold can be adjusted by changing the control voltage between 0V and +0.3V. If unbiased, or if  $V_{CTRL} = 0V$ , the TDLM06100 still offers power limiting protection.

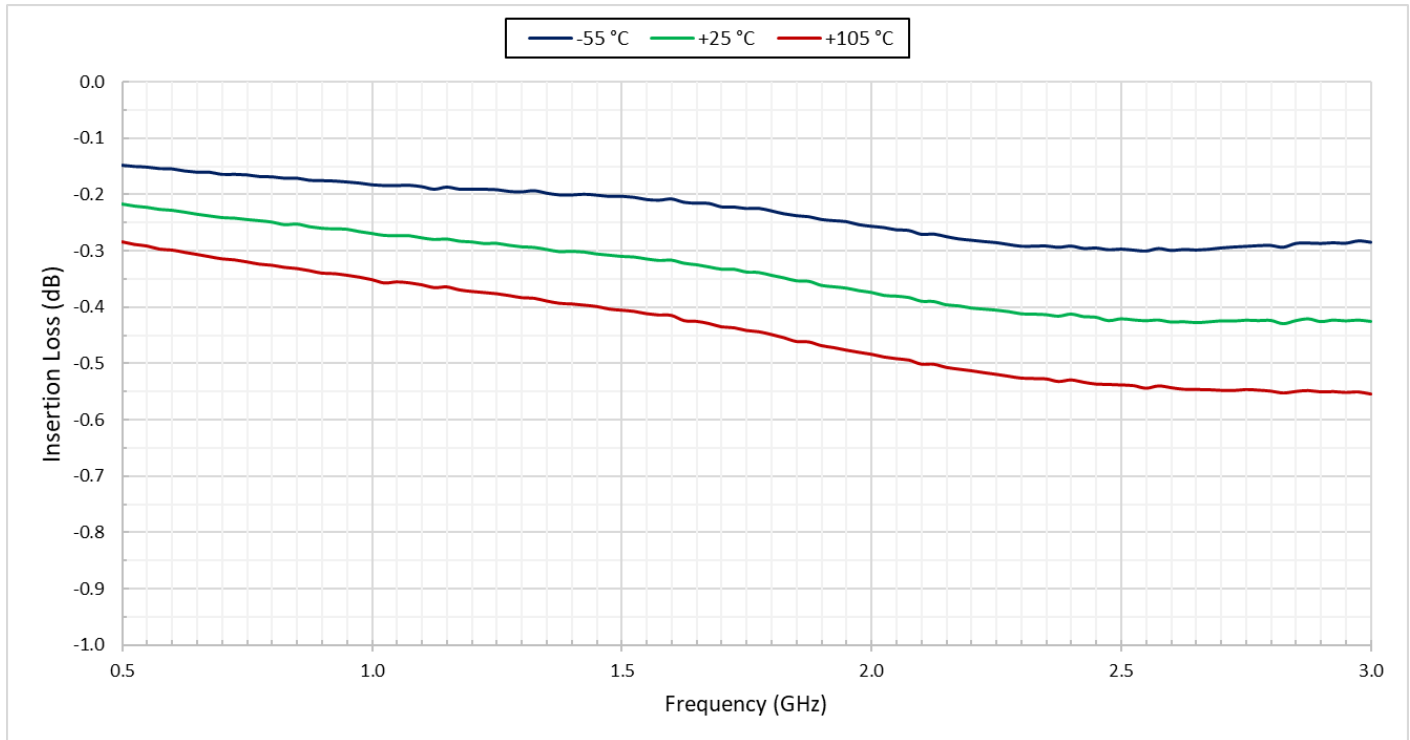
### Power Reflecting Mode

Power reflecting mode requires a power detector to sample the RF input power and a microcontroller to toggle the limiter control voltage between +3.0V and 0V based on the system protection requirements. At +3.0V, the limiter impedance to ground is less than  $1\Omega$  and most of the incident power will be reflected back to the source. At 0V, the device operates as in power limiting mode.

## Typical Performance Data

Fig. 3–Figure 16 show the typical performance data at +25 °C ( $Z_S = Z_L = 50 \Omega$ ), unless otherwise specified.

Figure 3 • *Insertion Loss vs Temp (Soldered 24L CLGA Package)*



**Note:** Figures 4-17 were taken using a 12L, 3x3 mm Plastic QFN Package

Figure 4 • *Input Return Loss vs Temp*

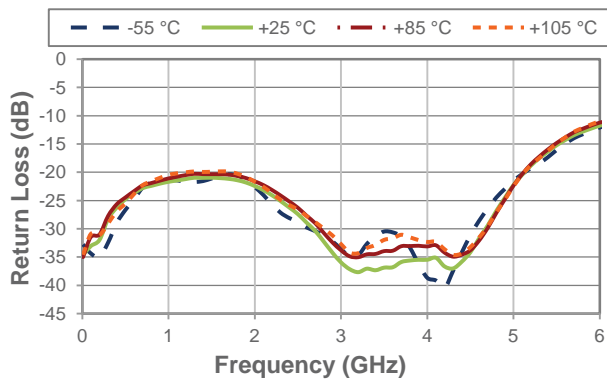
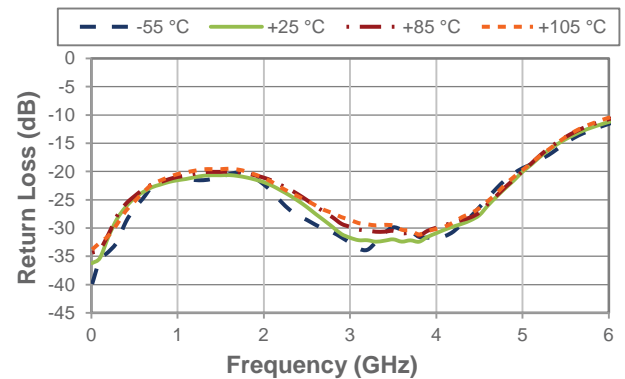
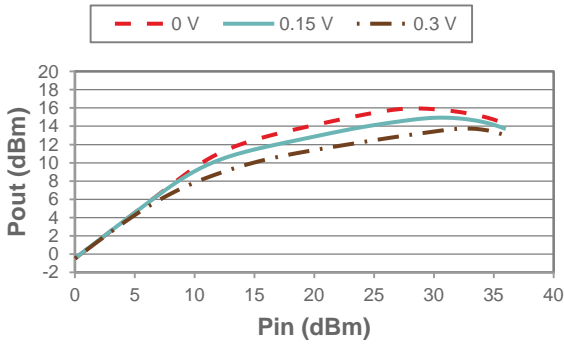


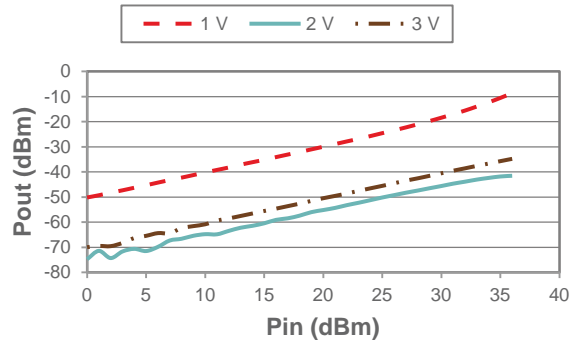
Figure 5 • *Output Return Loss vs Temp*



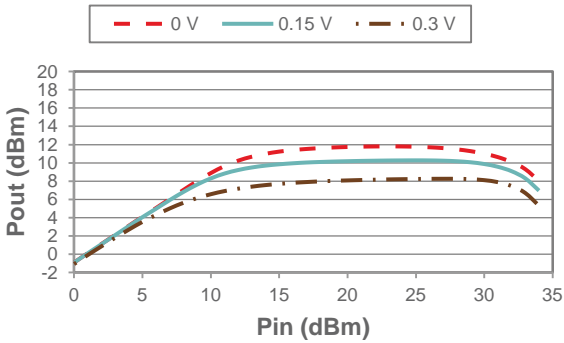
**Figure 6 •  $P_{OUT}$  vs  $P_{IN}$  Over  $V_{CTRL}$  (Limiting Mode @ 915 MHz)**



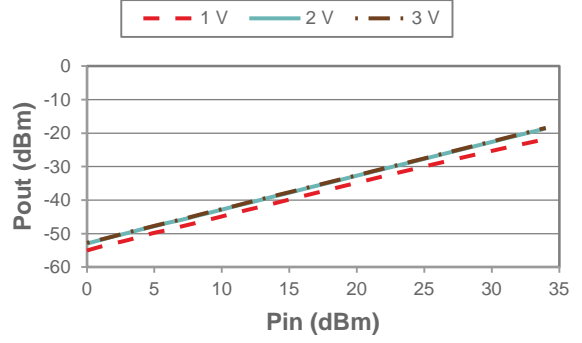
**Figure 9 •  $P_{OUT}$  vs  $P_{IN}$  Over  $V_{CTRL}$  (Reflecting Mode @ 915 MHz)**



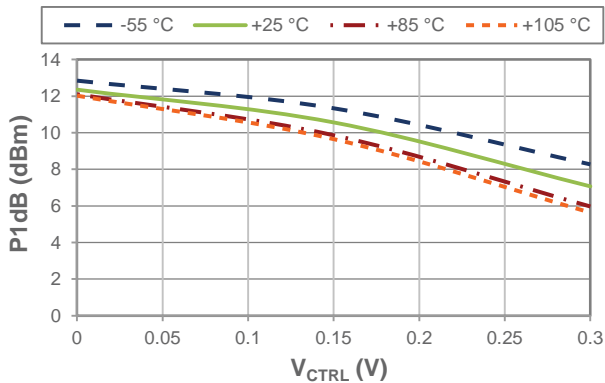
**Figure 7 •  $P_{OUT}$  vs  $P_{IN}$  Over  $V_{CTRL}$  (Limiting Mode @ 6 GHz)**



**Figure 10 •  $P_{OUT}$  vs  $P_{IN}$  Over  $V_{CTRL}$  (Reflecting Mode @ 6 GHz)**



**Figure 8 •  $P1dB$  vs  $V_{CTRL}$  Over Temp @ 915 MHz**



**Figure 11 •  $P1dB$  vs  $V_{CTRL}$  Over Temp @ 6 GHz**

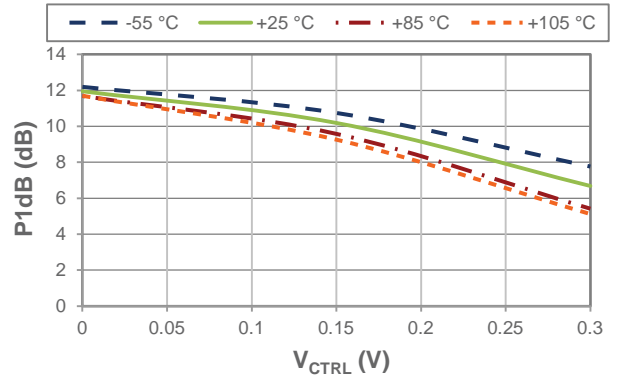




Figure 12 • Leakage Power @  $P_{MAX}$  vs  $V_{CTRL}$  Over Temp @ 915 MHz

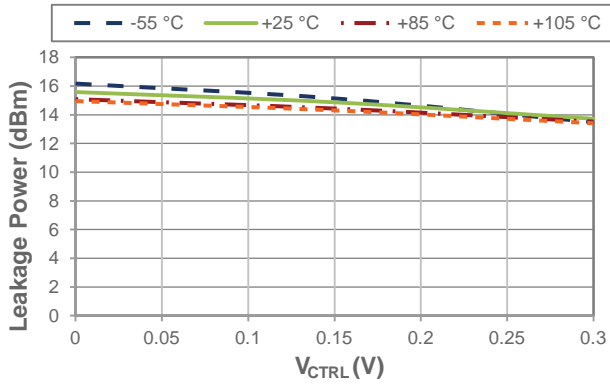


Figure 15 • Leakage Power @  $P_{MAX}$  vs  $V_{CTRL}$  Over Temp @ 6 GHz

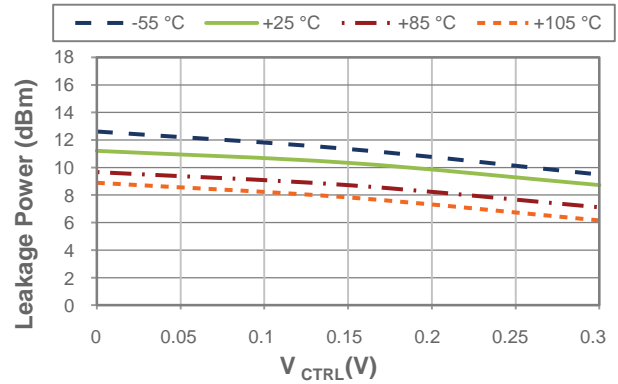


Figure 13 • IIP2/IIP3 vs  $P_{IN}$  Over  $V_{CTRL}$  @ 915 MHz

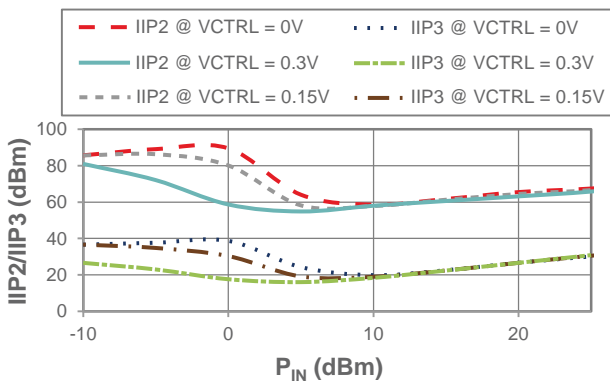


Figure 16 • IIP2/IIP3 vs  $P_{IN}$  Over  $V_{CTRL}$  @ 6 GHz

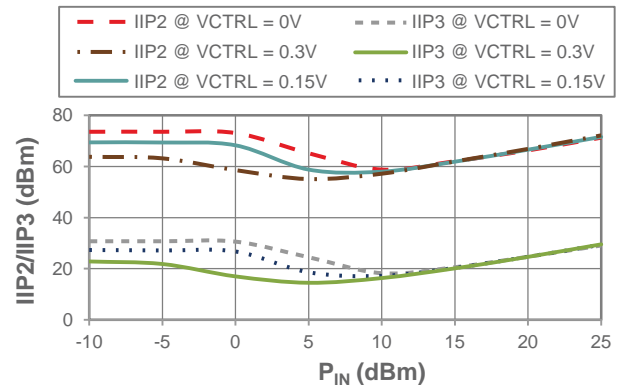


Figure 14 • IIP2/IIP3 vs  $V_{CTRL}$  Over  $P_{IN}$  @ 915 MHz

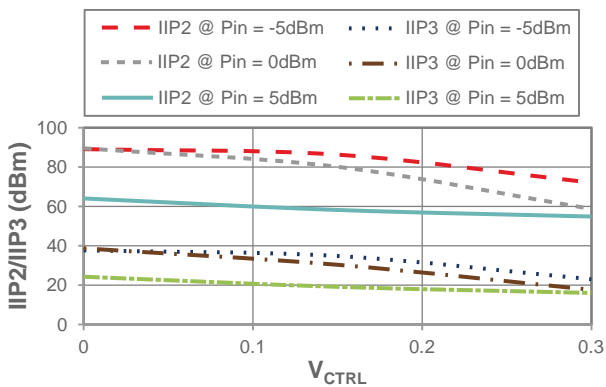
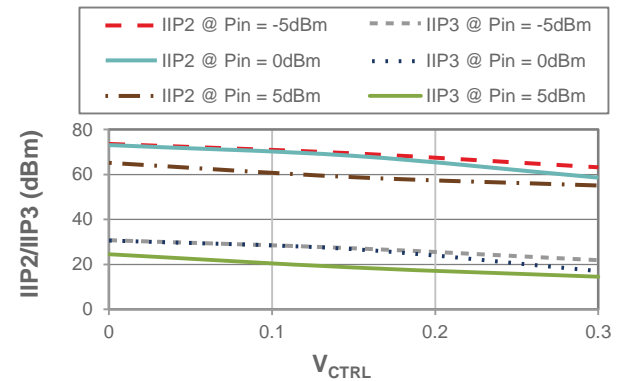


Figure 17 • IIP2/IIP3 vs  $V_{CTRL}$  Over  $P_{IN}$  @ 6 GHz

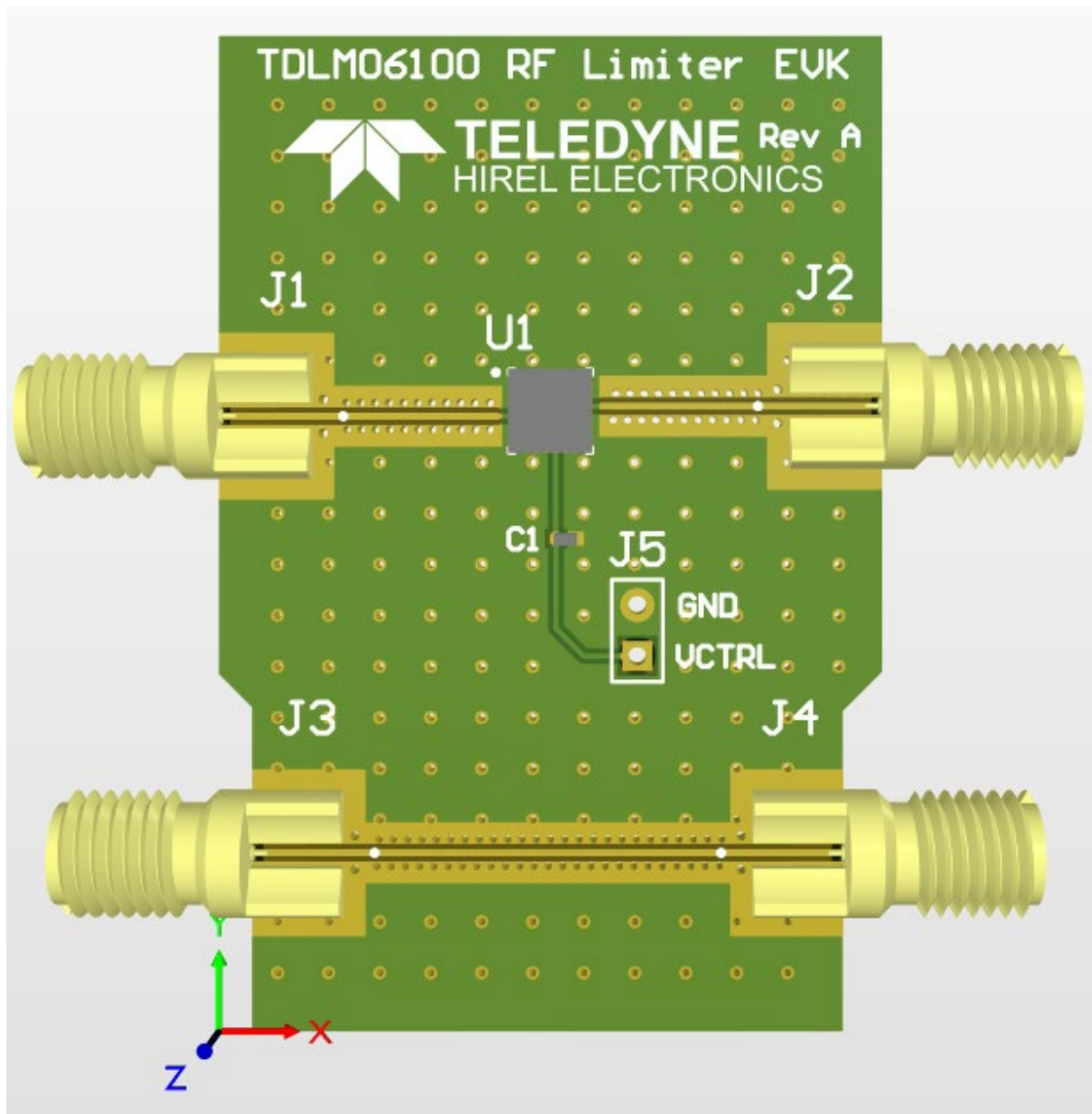


## Evaluation Kit

The power limiter evaluation kit board (EVB) was designed to ease customer evaluation of Peregrine's TDLM06100. The uni-directional RF input and output are connected to the RF1 and RF2 port through a 50Ω transmission line via SMA connectors J2 and J3. A through 50Ω transmission line is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated. The 2-pin connector J4 is connected to the external bias  $V_{CTRL}$ .

The board is constructed of a four metal layer material with a total thickness of 62 mils. The top RF layer is Rogers RO4350B material with a 6.6 mil RF core and  $\epsilon_R = 3.66$ . The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 13.5 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

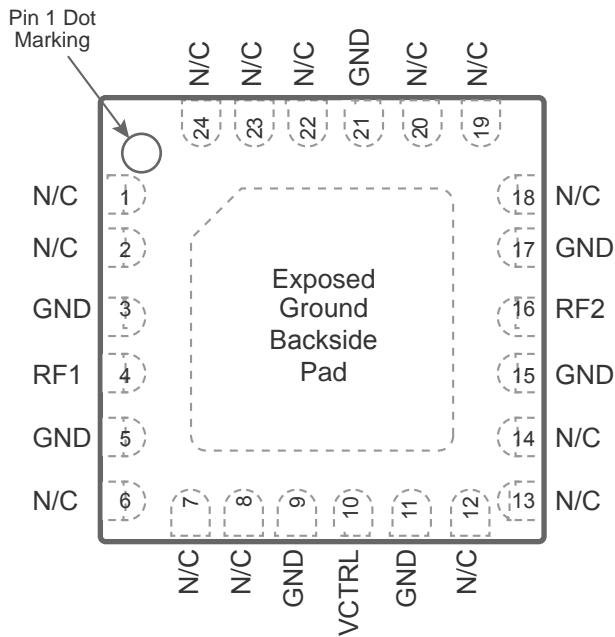
**Figure 18 • Evaluation Kit Layout for TDLM06100**



## Pin Information

This section provides pinout information for the TDLM06100. **Figure 19** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

**Figure 19 • Pin Configuration (Top View)**



**Table 5 • Pin Descriptions for TDLM06100**

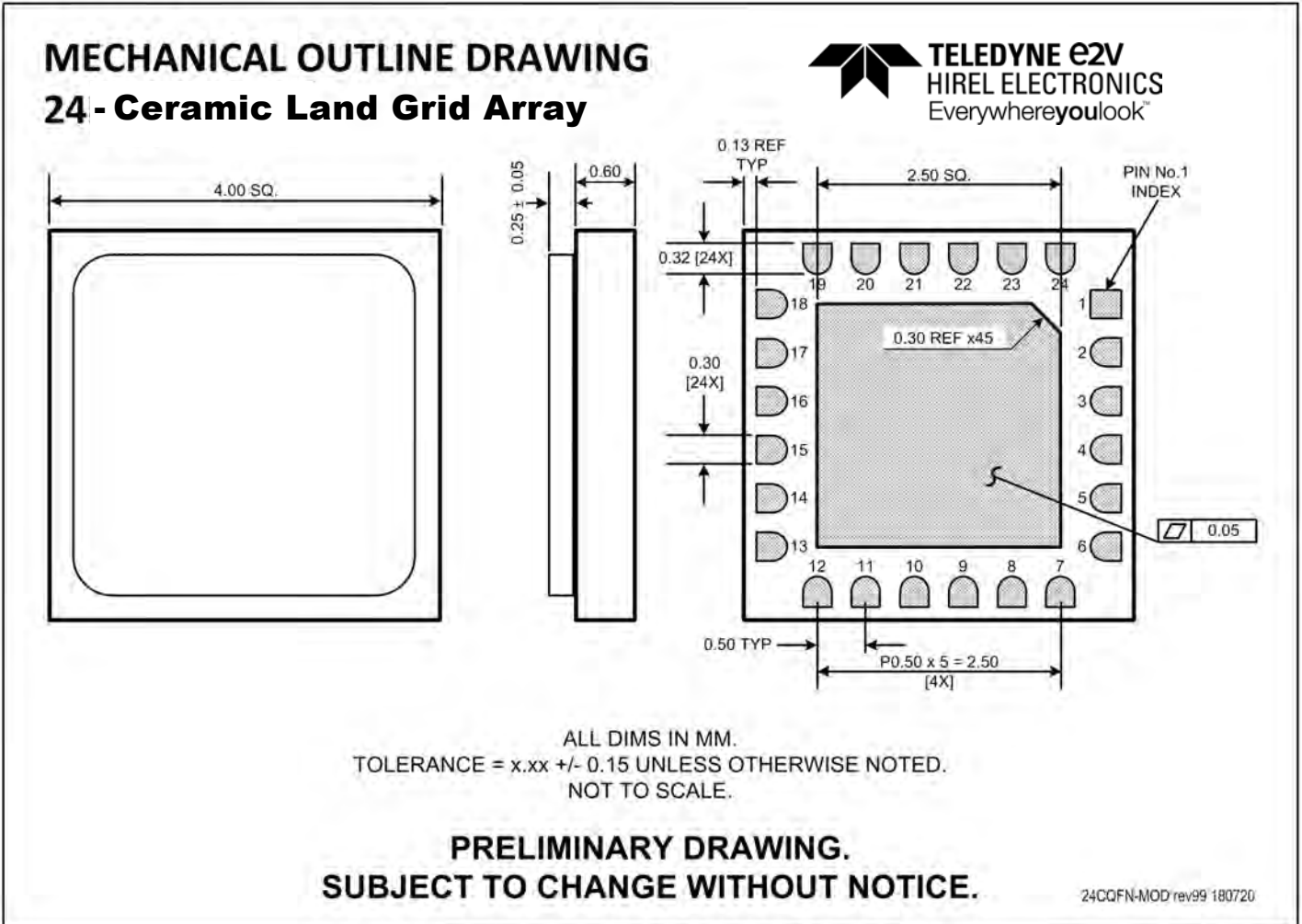
Pin No.	Pin Name	Description
3, 5, 9, 11, 15, 17, 21	GND	Ground
4	RF1 <sup>(1)(3)</sup>	RF port 1
10	V <sub>CTRL</sub>	Control voltage
16	RF2 <sup>(1)(3)</sup>	RF port 2
1, 2, 6-8, 12-14, 18-20, 22-24	N/C <sup>(2)</sup>	No connect
Pad	GND	Exposed backside pad: <b>ground</b> for proper operation
<b>Notes:</b>		
1) RF pins 4 and 16 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.		
2) N/C pins can be grounded, if deemed necessary by the customer.		
3) The limiter is not bi-directional. RF1 is the RF input and RF2 is the RF output.		

**Packaging Information**

This section provides packaging data

**Package Drawing**

Figure 20 • Package Mechanical Drawing for 24-lead 4 × 4 Ceramic QFN



## Ordering Information

Table 6 lists the available ordering codes for the TDLM06100 as well as available shipping methods.

Table 6 • Order Codes for TDLM06100

Order Codes	Description	Packaging	Shipping Method
TDLM06100-00	TDLM06100 Evaluation Kit	Evaluation kit	1/box
TDLM06100-01	TDLM06100 EM Units	24-lead 4 × 4 Ceramic LGA	Trays
TDLM06100-11	TDLM06100 Flight Units	24-lead 4 × 4 Ceramic LGA	Trays

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## Document Categories

### Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

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