DAC-08
8-Bit High Speed Multiplying D/A Converter

Description

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33 mW power consumption attainable at ±5.0V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. Devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1.0 µs A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

Features

- Fast settling output current — 85 ns
- Full scale current pre-matched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% max. over temperature range
- High output impedance and compliance — -10V to +18V
- Differential current outputs
- Wide range multiplying capability — 1.0 MHz bandwidth
- Low FS current drift — ±10 ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33 mW @ ±5.0V
- Low cost

Ordering Information

Part Number	Package	Operating Temperature Range	Non-linearity
DAC-08EN	N	0°C to +70°C	±0.19%
DAC-08CN	N	0°C to +70°C	±0.39%
DAC-08AD	D	-55°C to +125°C	±0.1%
DAC-08D	D	-55°C to +125°C	±0.19%
DAC-08D/883B	D	-55°C to +125°C	±0.19%
DAC-08AD/883B	D	-55°C to +125°C	±0.1%

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
N = 16-lead plastic DIP
D = 16- lead ceramic DIP

Absolute Maximum Ratings

(T_A = +25°C unless otherwise noted)

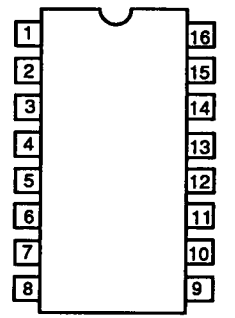
Supply Voltage (between $+V_S$ and $-V_S$) 36V
Logic Inputs ..... $-V_S$ to ($-V_S$ plus 36V)
Analog Current Outputs ..... 4 mA
Reference Inputs (V_{14} to V_{15}) ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) ..... 5.0 mA
Operating Temperature Range
DAC-08AD, D ..... -55°C to +125°C
DAC-08EN, CN ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Thermal Characteristics

	16-Lead Ceramic DIP	16-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	1042 mW	555 mW
Therm. Res θ_{JC}	60°C/W	—
Therm. Res. θ_{JA}	120°C/W	135°C/W
For T_A >50°C Derate at	8.38 mW/°C	7.41 mW/°C

Connection Information

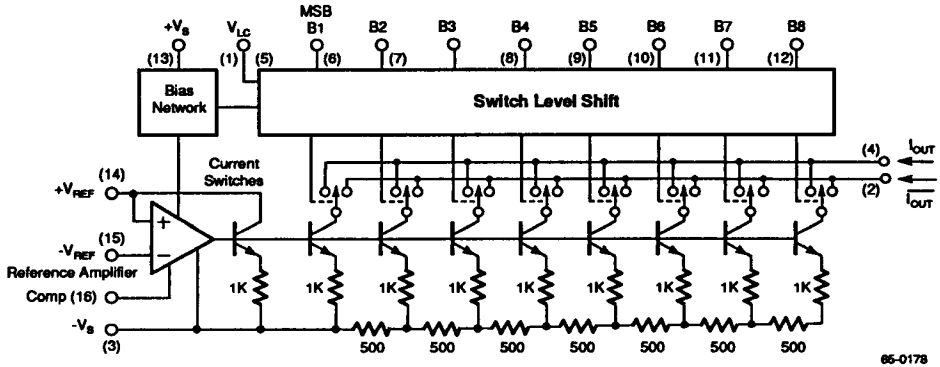
16-Lead
Dual-In-Line
(Top View)



65-0177

Pin	Function	Pin	Function
1	VLC Threshold Control	9	B5
2	I_{OUT}	10	B6
3	$-V_S$	11	B7
4	I_{OUT}	12	B8 (LSB)
5	B1 (MSB)	13	$+V_S$
6	B2	14	V_{REF} (+)
7	B3	15	V_{REF} (-)
8	B4	16	Compensation

Functional Block Diagram



Electrical Characteristics

(V_S = ±15V, I_{REF} = 2.0 mA, T_A = -55°C to +125°C for DAC-08 and DAC-08A; T_A = 0°C to +70°C for DAC-08C and DAC-08E unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameters	Test Conditions	DAC-08A			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.1			+0.19	%FS
Settling Time	To +1/2LSB, All Bits Switched ON or OFF T_A = +25°C[1]		85	135		85	150	ns
Propagation Delay								
Each Bit	T_A = +25°C[1]		35	60		35	60	ns
All Bits Switched			35	60		35	60	
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		±0.5	±4.0		±1.0	±8.0	µA
Zero Scale Current			0.1	1.0		0.2	2.0	
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = 12V	4.2			4.2			
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	µA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range[1]	V_S = ±15V	-10		+13.5	-10		+13.5	
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	µA
Reference Input Slew Rate[1]		4.0	8.0		4.0	8.0		mA/µs

Note:

1. Guaranteed by design, but not tested.

Electrical Characteristics (continued)

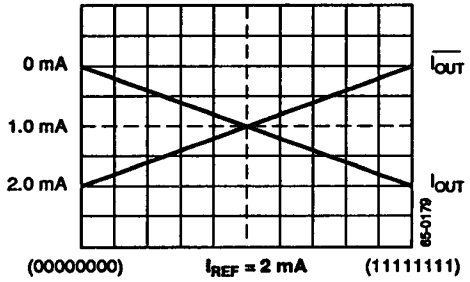
Parameters	Test Conditions	DAC-08A Min	DAC-08A Typ	DAC-08A Max	DAC-08 Min	DAC-08 Typ	DAC-08 Max	Units
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V,							%ΔFS
Positive	$-V_S$ = -4.5V to -18V,		±0.0003	±0.01		±0.0003	±0.01	%ΔV
Negative	I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01	%/%
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0 mA		-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V I_{REF} = 1.0 mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0 mA		108	136		108	136	
	V_S = ±15V I_{REF} = 2.0 mA		135	174		135	174	

Parameters	Test Conditions	DAC-08E Min	DAC-08E Typ	DAC-08E Max	DAC-08C Min	DAC-08C Typ	DAC-08C Max	Units
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.19			+0.39	%FS
Settling Time	To +1/2LSB, All Bits Switched ON or OFF T_A = +25°C[1]		85	150		85	150	ns
Propagation Delay								
Each Bit	T_A = +25°C[1]		35	60		35	60	ns
All Bits Switched			35	60		35	60	
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < 1/2 LSB R_{OUT} > 20 MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FS4}-I_{FS2}		±1.0	±8.0		±2.0	±16.0	µA

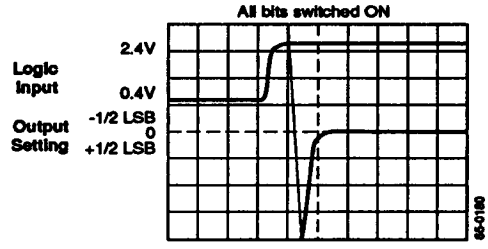
Electrical Characteristics (continued)

Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Scale Current			0.2	2.0		0.2	4.0	µA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5,000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	µA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range[1]	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	µA
Reference Input Slew Rate[1]		4.0	8.0		4.0	8.0		mA/µs
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V							
Positive	$-V_S$ = -4.5V to -18V		±0.0003	±0.01		±0.0003	±0.01	%ΔFS
Negative	I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01	%ΔV
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0 mA		-4.3	-5.8		-4.3	-5.8	
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.4	-7.8		-6.4	-7.8	
Positive	V_S = ±15V		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0 mA		-6.5	-7.8		-6.5	-7.8	
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0 mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0 mA		103	136		108	136	mW
	V_S = ±15V, I_{REF} = 2.0 mA		135	174		135	174	mW

Typical Performance Characteristics

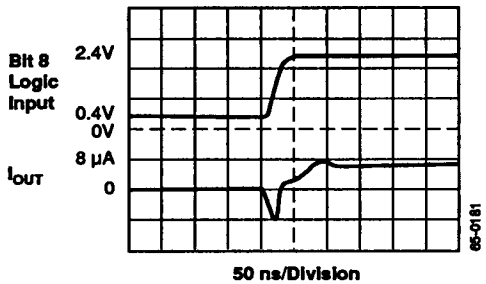


True and Complementary Output Operation



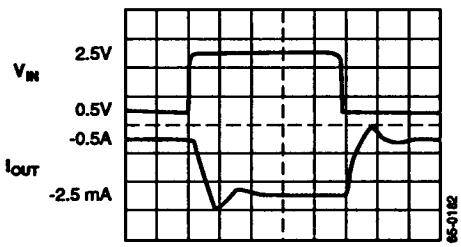
50 ns/Division
I_{FS} = 2 mA
R_L = 1 kΩ
1/2 LSB = 4 µA

Full Scale Settling Time



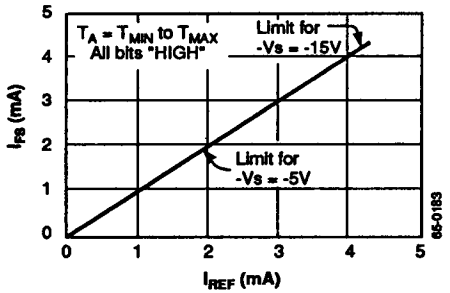
50 ns/Division

LSB Switching

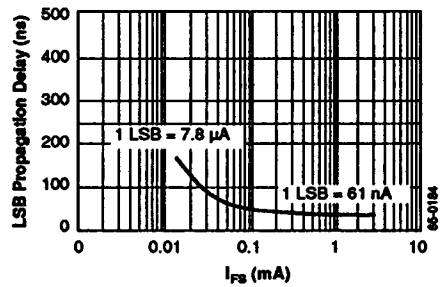


200 ns/Division
R_{EQ} (Input) = 200Ω
R_L = 100Ω
C_C = 0
R_{IN} = 5K
$+V_{IN}$ = 10V

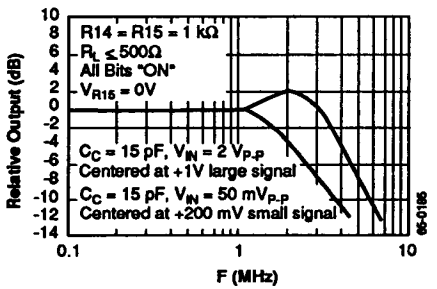
Fast Pulsed Reference Operation



Full Scale Output Current vs. Reference Current



LSB Propagation Delay vs. Full Scale Output Current



Reference Input Frequency Response

Applications Information

Reference Amplifier Set-up

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or vary from nearly zero to +4.0 mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to VREF(-) at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (normally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: $V_{CM^-} = -V_S$ plus (I_{REF} x 1 kΩ) plus 2.5V. The positive common mode range is $+V_S$ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1 µF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2 mA to +4.0 mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to $-V_S$. For fixed reference operation, a 0.01 µF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

Multiplying Operation

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0 µA to 4.0 mA. Monotonic operation is maintained over a typical range of I_{REF} from 100 µA to 4.0 mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to $-V_S$. The value of this capacitor depends on the impedance presented to pin 14; for R_{14} values of 1.0, 2.5, and 5.0 kΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0 kΩ and C_C = 15 pF, the reference amplifier slews at 4.0 mA/µs enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0 mA) occurs in 120 ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16 mA/µs which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0 µA logic input current and completely adjustable logic threshold voltage. For $-V_S$ = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +5V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: $-V_S$ plus (I_{REF} x 1.0 kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range

by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). V_{TH} is nominally 1.4V above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL an I_{REF} = 1.0 mA is recommended. For general setup of the logic control circuit, it should be noted that pin 1 will source or sink 100 µA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0 kΩ divider, for example, it should be bypassed to ground by a 0.01 µF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided where $I_{OUT} + \overline{I_{OUT}} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_{OUT}}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above $-V_S$ and is independent of the positive supply. Negative compliance is given by $-V_S$ plus (I_{REF} x 1.0 kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection, and other balanced applications such as driving center-tapping coils and transformers.

Power Supplies

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5.0V or less, $I_{REF} \leq 1.0$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required. However, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows: $Pd = (I+)(+V_S) + (I-)(-V_S) + (2\ I_{REF})(-V_S)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power bypass capacitors.

Temperature Performance

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is typically ±10 ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at -55°C; at +125°C an increase of about 15% is typical.

Typical Applications

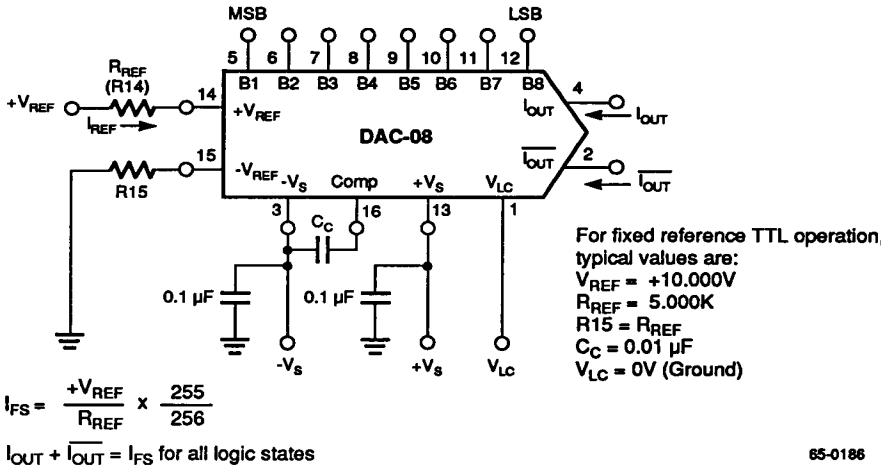


Figure 1. Basic Positive Reference Operation

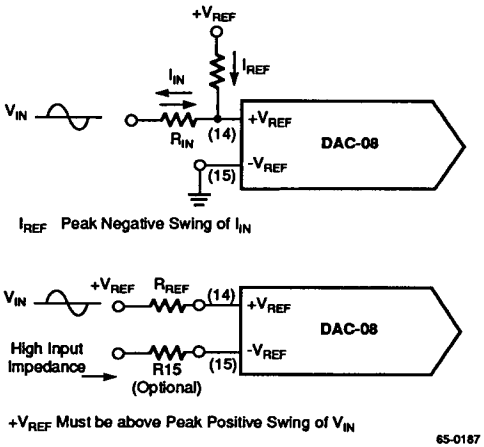


Figure 2. Accommodating Bipolar References

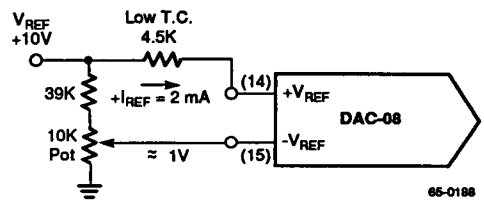


Figure 3. Recommended Full Scale Adjustment Circuit

Typical Applications (Continued)

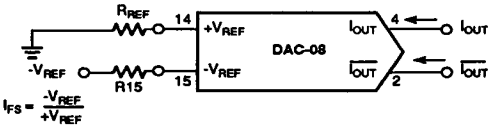
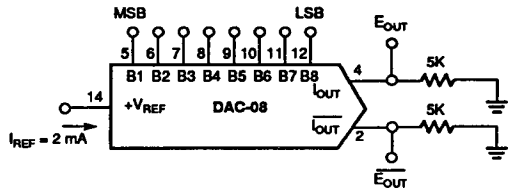


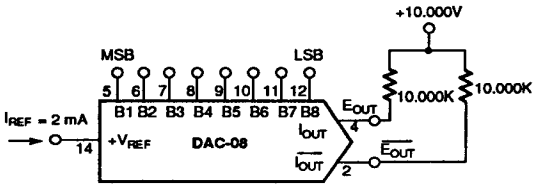
Figure 4. Basic Negative Reference Operation



Scale	B1	B2	B3	B4	B5	B6	B7	B8	I_{OUT}mA	$\overline{I_{OUT}}$mA	E_{OUT}	$\overline{E_{OUT}}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.008	-9.660	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

65-0190

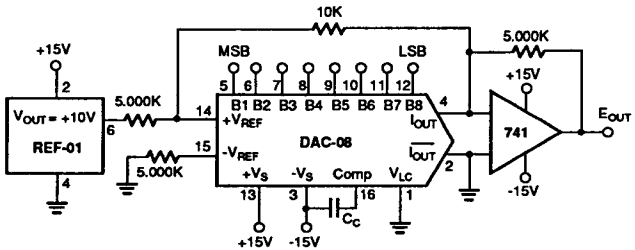
Figure 5. Basic Unipolar Negative Operation



Scale	B1	B2	B3	B4	B5	B6	B7	B8	E_{OUT}	$\overline{E_{OUT}}$
Pos Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos Full Scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

65-0191

Figure 6. Basic Bipolar Output Operation

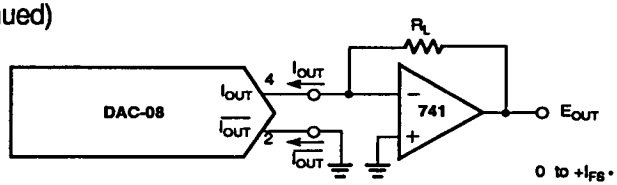


Scale	B1	B2	B3	B4	B5	B6	B7	B8	E_{OUT}
Pos Full Scale	1	1	1	1	1	1	1	1	+4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale + 1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

65-0192

Figure 7. Offset Binary Operation

Typical Applications (Continued)



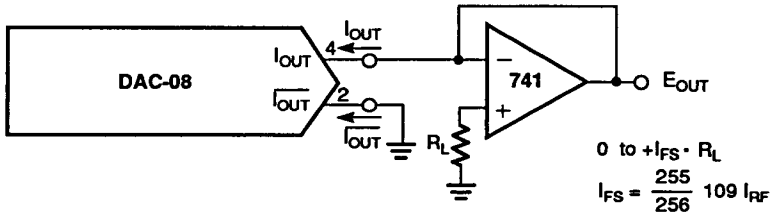
For complementary output (operation as a negative logic (DAC) connect inverting input of op amp to $\overline{I_{OUT}}$ (pin 2) ; connect I_{OUT} (pin 4) to ground.

$0 \text{ to } +I_{FS} \cdot R_L$

$I_{FS} = \frac{255}{256} I_{REF}$

65-0193

Figure 8. Positive Low Impedance Output Operation



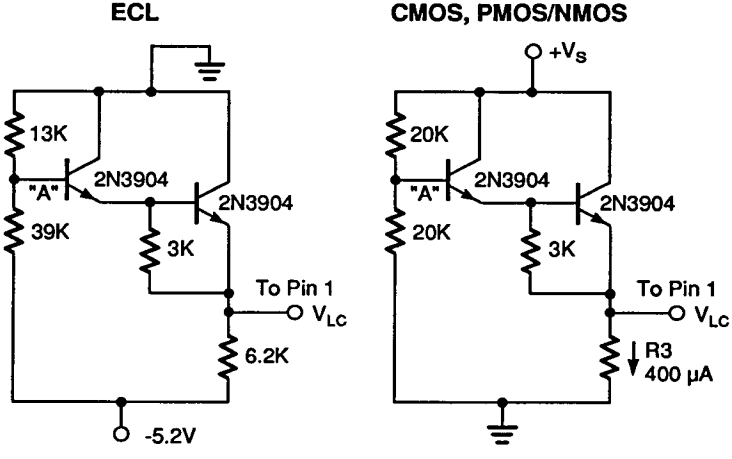
For complementary output (operation as a negative logic (DAC) connect inverting input of op amp to $\overline{I_{OUT}}$ (pin 2) ; connect I_{OUT} (pin 4) to ground.

$0 \text{ to } +I_{FS} \cdot R_L$

$I_{FS} = \frac{255}{256} 109\ I_{RF}$

65-0194

Figure 9. Negative Low Impedance Output Operation



Temperature Compensating V_{LC} Circuits

65-0195

Figure 10. Interfacing With Various Logic Families

Settling Time

The DAC-08 is capable of extremely fast settling times, typically 85 ns at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within 1/2 LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 85 ns. Settling to 6-bit accuracy requires about 65 to 70 ns. The output capacitance of the DAC-08 including the package is approximately 15 pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output R_C time constant.

Measurement of settling time requires the ability to accurately resolve ±4.0 µA, therefore a 1.0 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture uses a cascade design to permit driving a 1.0 kΩ load with less than 5.0 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}..

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic state: 0.1 µF capacitors at the supply pins provide full transient protection.

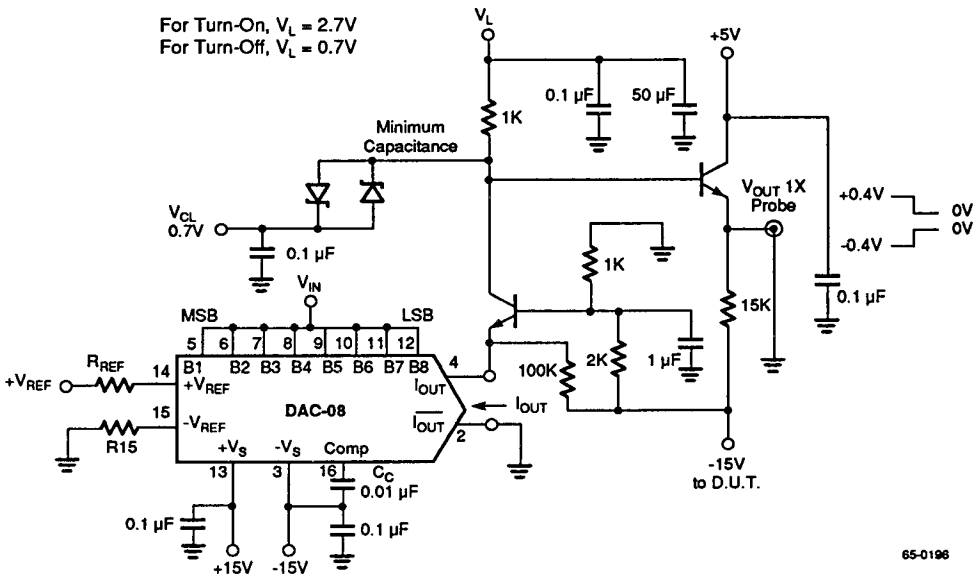


Figure 11. Settling Time Test Fixture