QP27C128

April 7, 2009

QP27C128 – 128 Kilobit (16K x 8) CMOS EPROM

General Description

The QP27C128 is a 16Kx8 (128-Kbit), UV erasable programmable read-only memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The QP27C128 meets the same specification requirements and utilizes the same programming methodology as the AMD 27C128 that it replaces.

Products are available in windowed and non-windowed (OTP) ceramic hermetic packages, as well as plastic one time programmable (OTP) packages.

Data is typically accessed in less than 45 ns, allowing high-performance microprocessors to operate without any WAIT states. The device offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) pins, eliminating bus contention in a multiple bus system.

Typical power consumption is only 80 mW in active mode, and 100 µW in standby mode.

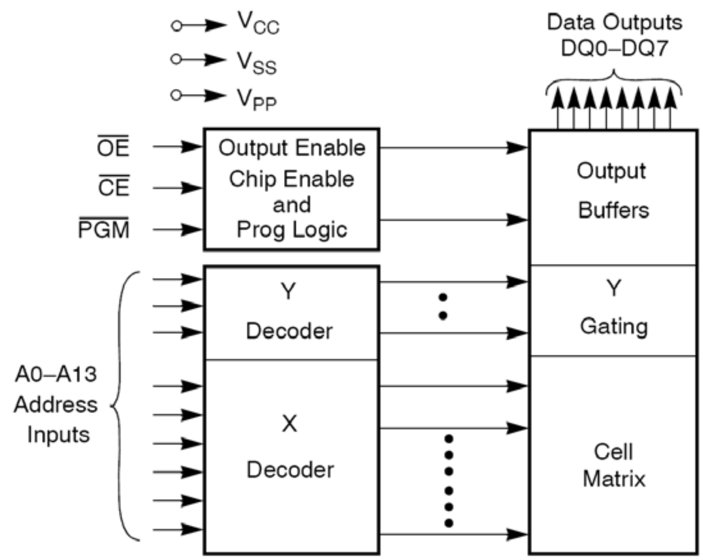
All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The device is programmed identically to the AMD27C128 device that it replaces, using the same programming algorithm (100 us pulses).

The QP27C128 features:

- Same programming algorithm as the AMD27C128, allowing it to be programmed using the same equipment, data and algorithm. When programming this device select AMD as the manufacturer and 27C128 as the devicetype.
- Speed options as fast as 45ns
- JEDEC Pinout
- Single +5V power supply
- CMOS and TTL input/output compatibility
- Two line control functions

The device/family is constructed using an advanced UV CMOS wafer fabrication process.

Block Diagram

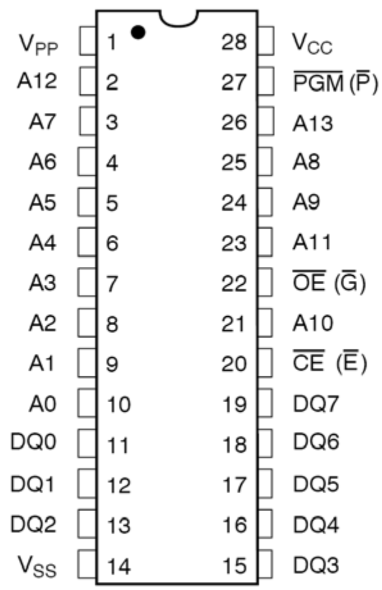


Pin Name	Function
$A_0 - A_{13}$	Address Inputs
$\overline{CE}$ ($\overline{E}$)	Chip Enable Input
$D_{Q0} - D_{Q7}$	Data Input/Output
$\overline{OE}$ ($\overline{G}$)	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	Program Enable Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Voltage Input

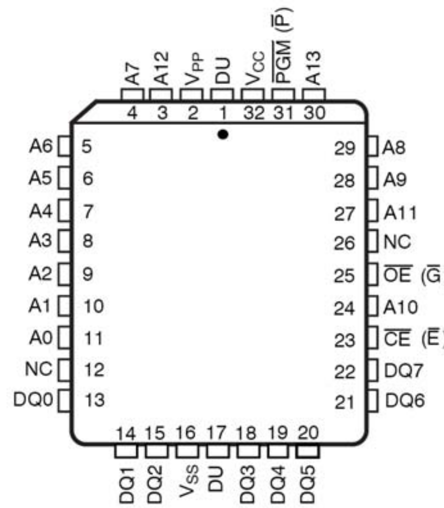
Connection Diagrams

Device Type

CERDIP / CERPACK / PDIP



LCC / PLCC



Functional Description

Device Erasure

In order to clear all locations of their programmed contents, the device must be exposed to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase the device. This dosage can be obtained by exposure to an ultraviolet lamp with a wavelength of 2537Å and an intensity of 12,000 μW/cm^2 for 15 to 20 minutes. The device should be directly under and about one inch from the source, and all filters should be removed from the UV light source prior to erasure.

Note that all UV erasable devices will erase with light sources having wavelengths shorter than 4000Å, such as fluorescent light and sunlight. Although the erasure process happens over a much longer time period, exposure to any light source should be prevented for maximum system reliability. Simply cover the package window with an opaque label or substance.

Device Programming

Upon delivery, or after each erasure, the device has all of its bits in the “ONE”, or HIGH state. “ZEROs” are loaded into the device through the programming procedure.

The device enters the programming mode when 12.75V ± 0.25V is applied to the V_{PP} pin, and both $\overline{CE}$ & $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data pins.

The programming algorithm uses a 100 μs programming pulse and gives each address only as many pulses as needed to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum pulses allowed is reached. This process is repeated while sequencing through each address of the device. This part of the algorithm is done with V_{CC} = 6.25 V to assure that each bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming different data to multiple devices in parallel is easily accomplished. Except for $\overline{CE}$, all like inputs of the devices may be common. A TTL low-level program pulse applied to one device's $\overline{CE}$ input with V_{PP} = 12.75 V ± 0.25 V and $\overline{PGM}$ LOW will program that particular device. A high-level $\overline{CE}$ input inhibits the other devices from being programmed.

Program Verify

Verification should be performed on the programmed bits to determine that they were correctly programmed. Verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Autoselect Mode

The autoselect mode provides manufacturer and device identification through identifier codes on DQ0–DQ7. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the device. To activate this mode, the programming equipment must force V_H on address line A9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} (that is, changing the address from 00h to 01h). All other address lines must be held at V_{IL} during the autoselect mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. Both codes have odd parity, with DQ7 as the parity bit.

Read Mode

To obtain data at the device outputs, Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be driven low. $\overline{CE}$ controls the power to the device and is typically used to select the device. $\overline{OE}$ enables the device to output data, independent of device selection. Addresses must be stable for at least t_{ACC}–t_{OE}.

Standby Mode

The device enters the CMOS standby mode when $\overline{CE}$ is at V_{CC} ± 0.3 V. Maximum V_{CC} current is reduced to 100 µA. The device enters the TTL-standby mode when $\overline{CE}$ is at V_{IH}. Maximum VCC current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR Connection

To accommodate multiple memory connections, a two-line control function provides:

- Low memory power dissipation
- Assurance that output bus contention will not occur.

$\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. As a minimum, a 0.1µF ceramic capacitor (high frequency, low inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE Select Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs	Notes
Read	V_{IL}	V_{IL}	X	X	X	X	D_{OUT}	\1
Output Disable	X	V_{IH}	X	X	X	X	High Z	\1
Standby (TTL)	V_{IH}	X	X	X	X	X	High Z	\1
Standby (CMOS)	$V_{CC}\pm0.3V$	X	X	X	X	X	High Z	\1
Program	V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}	\1
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}	\1
Program Inhibit	V_{IH}	X	X	X	X	V_{PP}	High Z	\1
Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01h	\1 \2 \3 \4
Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	16h	\1 \2 \3 \4

Notes:

\1 X = Either V_{IH} or V_{IL}

\2 V_H = 12.0V ± 0.5V

\3 A_1-A_8 & A_{10}-A_{12} = V_{IL}

\4 Device Manufacture Code and Device ID match original AMD device for programming compatibility

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Power Supply (V_{CC})	-0.6 to +6.25	Volts DC	
Voltage with Respect to V_{SS}			
All pins except A_9, V_{PP}, V_{CC}	-0.6 to +6.25	Volts	\5 \9
A_9	-0.6 to +13.5	Volts	\6 \9
V_{PP}	-0.6 to +14	Volts	\6 \9
Storage Temperature Range	-65 to +150	ºC	\7
Lead Temperature (soldering, 10 seconds)	+300	ºC	
Junction Temperature (T_J)	+150	ºC	\7
Maximum Operating Temperature			
Commercial Devices	0 to 70	ºC	\7 \8
Industrial Devices	-40 to 85	ºC	\7 \8
Military Temperature Range	-55 to 125	ºC	\7 \8
Data Retention	10	Years, minimum	
Device must not be removed from or inserted into a socket when V_{CC} or V_{PP} is applied.			

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range (V_{CC})	4.5 to 5.5	Volts DC	
Input or Output Voltage Range	0.0 to V_{CC}	Volts DC	\5 \6
Minimum High-Level Input Voltage ($V_{IH\ TTL}$)	2.0	Volts DC	
Minimum High-Level Input Voltage ($V_{IH\ CMOS}$)	$V_{CC}\pm0.2$	Volts DC	
Maximum Low-Level Input Voltage ($V_{IL\ TTL}$)	0.8	Volts DC	
Maximum Low-Level Input Voltage ($V_{IL\ CMOS}$)	GND ± 0.2	Volts DC	
Case Operating Range (T_c)			
Commercial Devices	0 to 70	ºC	\7 \8
Industrial Devices	-40 to 85	ºC	\7 \8

Military Temperature Range	-55 to 125 °C	\7 \8

\5 – Minimum DC Input Voltage on input or I/O pins –0.5V. During voltage transitions, the input may overshoot VSS to –2.0V for periods of up to 20ns. Maximum DC voltage on input and I/O pins is VCC+0.5V. During transitions, input and I/O pins may overshoot to VCC +2.0V for periods up to 20ns.
\6 – Minimum DC Input Voltage on A9 is –0.5V. During voltage transitions, A9 and VPP may overshoot VSS to –2.0V for periods of up to 20ns. A9 and VPP must not exceed +13.5V at any time.
\7 – Do not exceed 125ºC TC or TJ for plastic package devices.
\8 – Maximum PD, Maximum TJ Are Not to Be Exceeded.
\9 – During transitions, the inputs may undershoot to –2.0 V dc for periods less than 20 ns.
\10 – V_{PP} may be connected directly to V_{CC} except during programming.
\11 – Qualification Only.
\12 – If not tested, shall be guaranteed to the limits specified.
\13 – For all switching characteristics and timing measurements, input pulse levels are 0.4V and 2.4V and VPP = 12.5 ± 0.5V during programming.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

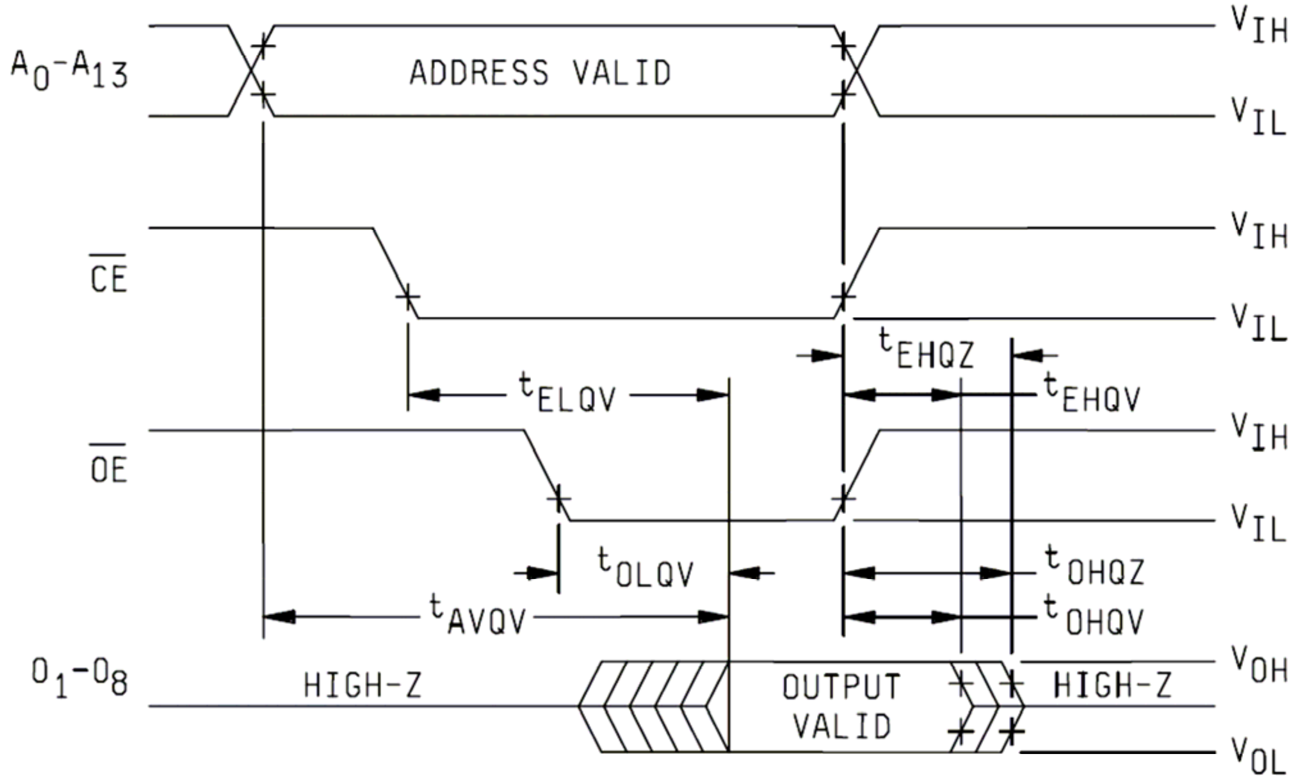
Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified	Min	Max	Unit
Output High Voltage	V_{OH}	V_{IL}=0.8V,V_{IH}=2.0V I_{OL}= -400 µA	2.4		V
Output Low Voltage	V_{OL}	V_{IL}=0.8V,V_{IH}=2.0V I_{OL}= 2.1mA		0.45	V
Input Current (Leakage)	I_I	V_I = 5.5V or 0.0V All other inputs at either V_{CC} or GND	-10.0	+10.0	µA
Output Current (Leakage)	I_O	V_O = 5.5V or 0.0V	-10.0	+10.0	µA
V_{PP} Supply Current	I_{PP1}	V_{PP} = V_{CC} = 5.5V		100	µA
V_{PP} Supply Current (during program pulse) \12	I_{PP2}	V_{PP} = 13V All but 70ns		50	mA
		70ns		60	mA
Operating Current (active)	I_{CC1}	V_{CC} = 5.5V 70ns		85	mA
		$\overline{CE}$ ($\overline{E}$) = V_{IL} 90ns		70	mA
		f = 1/t_{AVQV} 120ns		60	mA
		O_0-O_7 = 0 mA 150ns		25	mA
		170ns		25	mA
		200ns		25	mA
		250ns		25	mA
		300ns		25	mA

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified		Min	Max	Unit
Standby Current, TTL	I_{CC2}	V_{CC} = 5.5V	70ns		200	mA
		$\overline{CE}$ ($\overline{E}$) =2.0Vdc	90ns		3.0	mA
		f = 0hz	120ns		3.0	mA
			150ns		3.0	mA
			170ns		3.0	mA
			200ns		3.0	mA
			250ns		3.0	mA
			300ns		3.0	mA
Standby Current, CMOS	I_{CC3}	V_{CC} = 5.5V	70ns		300	µA
		$\overline{CE}$ ($\overline{E}$) = V_{CC}	90ns		300	µA
		f = 0Hz	120ns		300	µA
			150ns		300	µA
			170ns		300	µA
			200ns		300	µA
			250ns		300	µA
			300ns		500	µA
Input Capacitance \11	C_{IN}	V_{IN} = 0V, f = 1 MHz			10	pF
Output Capacitance \11	C_{OUT}	V_{OUT} = 0V, f = 1 MHz			14	pF
Address to Output Delay \13	T_{AVQV}		70ns		70	ns
			90ns		90	ns
			120ns		120	ns
			150ns		150	ns
			170ns		170	ns
			200ns		200	ns
			250ns		250	ns
			300ns		300	ns

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions -55ºC ≤TA≤+125ºC Unless Otherwise Specified	Min	Max	Unit
Chip enable access time \13	T_{ELQV}	70ns		70	ns
		90ns		90	ns
		120ns		120	ns
		150ns		150	ns
		170ns		170	ns
		200ns		200	ns
		250ns		250	ns
		300ns		300	ns
Output enable access time \13	T_{OLQV}	70ns		25	ns
		90ns		50	ns
		120ns		50	ns
		150ns		70	ns
		170ns		70	ns
		200ns		75	ns
		250ns		100	ns
		300ns		120	ns
$\overline{CE}$ or $\overline{OE}$ disable to output in high Z \12	T_{EHQZ}, T_{OHQZ}	70ns		25	ns
		90ns		50	ns
		120ns		50	ns
		150ns		50	ns
		170ns		50	ns
		200ns		60	ns
		250ns		60	ns
		300ns		105	ns
$\overline{CE}$ or $\overline{OE}$ enable to output valid \12	T_{EHQV}, T_{OHQV}	70ns		0	ns
		90ns		0	ns
		120ns		0	ns
		150ns		0	ns
		170ns		0	ns
		200ns		0	ns
		250ns		0	ns
		300ns		0	ns



Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
5962-8766101XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-90/XA
5962-8766101YA	CQCC1-N32 (LCC)	QP27C128-90/YA
5962-8766101YC	CQCC1-N32 (LCC)	QP27C128-90/YC
5962-8766102XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-120/XA
5962-8766102YA	CQCC1-N32 (LCC)	QP27C128-120/YA
5962-8766102YC	CQCC1-N32 (LCC)	QP27C128-120/YC
5962-8766103XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-150/XA
5962-8766103YA	CQCC1-N32 (LCC)	QP27C128-150/YA
5962-8766103YC	CQCC1-N32 (LCC)	QP27C128-150/YC
5962-8766104XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-170/XA
5962-8766104YA	CQCC1-N32 (LCC)	QP27C128-170/YA
5962-8766104YC	CQCC1-N32 (LCC)	QP27C128-170/YC
5962-8766105XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-200/XA
5962-8766105YA	CQCC1-N32 (LCC)	QP27C128-200/YA
5962-8766105YC	CQCC1-N32 (LCC)	QP27C128-200/YC
5962-8766106XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-250/XA
5962-8766106YA	CQCC1-N32 (LCC)	QP27C128-250/YA
5962-8766106YC	CQCC1-N32 (LCC)	QP27C128-250/YC
5962-8766107XA	GDIP1-T28 CDIP2-T28 (DIP)	QP27C128-300/XA
5962-8766107YA	CQCC1-N32 (LCC)	QP27C128-300/YA
5962-8766107YC	CQCC1-N32 (LCC)	QP27C128-300/YC
5962-8766108YA	CQCC1-N32 (LCC)	QP27C128-70/YA

QP Semiconductor supports Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

"-MIL" products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B devices. This datasheet defines the electrical test requirements for the device(s).

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com