QP SEMICONDUCTOR

October 9, 2007

QP111 Voltage Comparator / QP2111 Dual Voltage Comparator

General Description

The QP2111 dual voltage comparator is a single monolithic die with two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in closer thermal tracking, lower weight, reduced insertion cost and smaller size than two individual die. The QP Semiconductor product is improved over other manufacturer's devices of the same device type because thermal tracking is improved again over their products that are based on using two separate die in a single package.

The QP2111/QP111 are industry standard LM111 voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages. The devices operate from standard ±15V op amp supplies down to the single 5V supply used for IC logic.

Their outputs are compatible with RTL, DTL and TTL as well as CMOS/MOS circuits. And, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the QP2111/QP111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. The family is also much less prone to spurious oscillations than either the LM106 or LM710.

The QP111 has the same pin configuration as the LM111, LM106 and LM710. The QP2111 has the same pin configuration as the LH2111/LM2111.

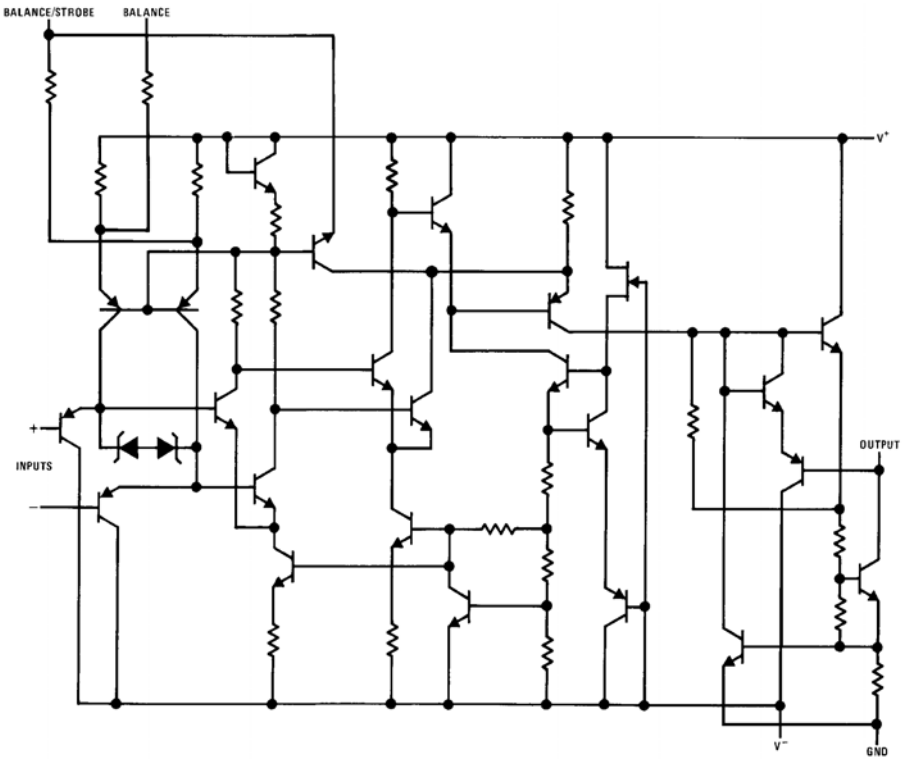
The QP2111/QP111 are specified for operation over the -55°C to +125°C military temperature range.

The QP2111/QP111 feature:

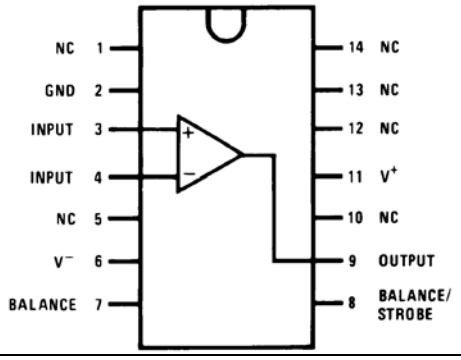
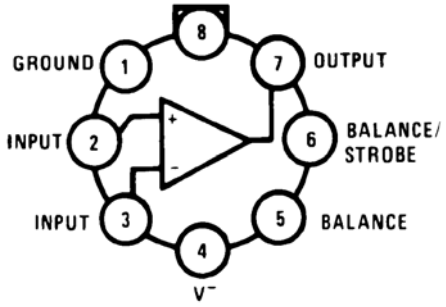
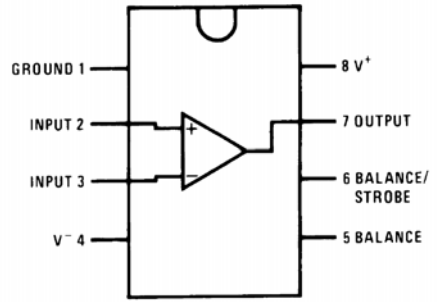
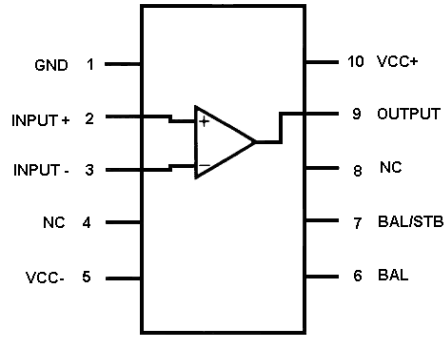
- Wide operating supply range: ±15V to a single +5V
- Input current: 150 nA maximum over temperature
- Offset current: 20 nA maximum over temperature
- Wide Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V
- High output drive: 50 mA, 50V

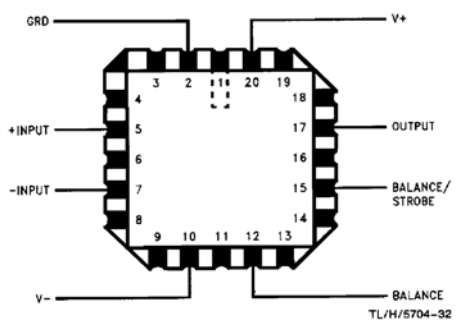
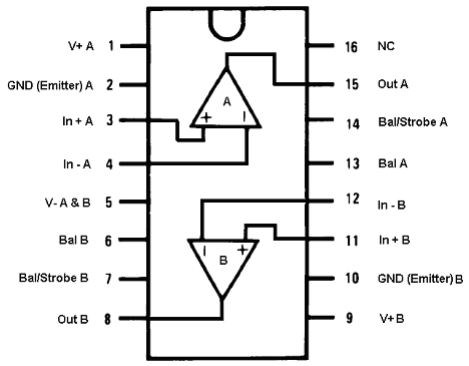
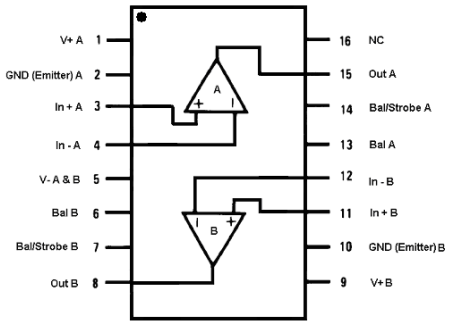
The family is constructed using an advanced bipolar process.

Equivalent Schematic Diagram



Connection Diagrams

	CerDIP/Cerpack 14 Lead	Metal Can
QP111		
	CerDIP/DIP 8 Lead	**CerPACK/Flatpack 10 Lead**
QP111		

	LLCC 20 Lead	
QP111		
	CerDIP/DIP 16 Lead	CerPACK/Flatpack 16 Lead
QP2111		

Absolute Maximum Ratings

Stresses above the AMR may cause permanent damage, extended operation at AMR may degrade performance and affect reliability

Condition		Units	Notes
Total Supply Voltage	36	Volts	
Positive Supply Voltage	+30	Volts	
Negative Supply Voltage	-30	Volts	
Output to Negative Supply Voltage	50	Volts	
Ground to Negative Supply Voltage	30	Volts	
Differential Input Voltage	±30	Volts	
Input Voltage	±15	Volts	/1
Output Sink Current	50	mA	
Output Short Circuit Duration	10	Seconds	
Maximum Strobe Current	10	mA	
Voltage at Strobe Pin	V+ −5	Volts	
Storage Temperature Range	-65 to +150	ºC	
Lead Temperature (soldering, 10 seconds)	+260	ºC	
Junction Temperature (T_J)	+175	ºC	/2

Recommended Operating Conditions

Condition		Units	Notes
Supply Voltage Range	4.5 to 30	Volts DC	/3
Case Operating Range (T_c)	-55C to +125	ºC	/2

Notes:

Apply to Absolute Maximum, Recommended Operating Conditions and Electrical Performance Characteristics.

/1 – This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage, or 30V below the positive supply, whichever is less.

/2 – Maximum T_J is not to be exceeded.

/3 – Absolute Maximum Conditions are not to be exceeded relative to total supply voltage and input limitations.

/4 – These specifications apply for $+V_{CC}/-V_{CC}$= ±15V and Ground pin at ground, and −55°C≥T_A≤+125°C, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

/5 – The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. These parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

/6 – The response time specified is for a 100 mV input step with 5 mV overdrive.

/7 – This specification gives the range of current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

/8 – V_{IC} is achieved by algebraically subtracting the common mode voltage from each supply voltage ($+V_{CC}$ and $-V_{CC}$) and algebraically adding it to V_{IN}. V_{IC} can be calculated by using the following formula:

$$V_{IC} = -\left[\frac{(+V_{CC})+(-V_{CC})}{2}\right] - V_{IN}$$

/9 – Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to $+V_{CC}$.

/10 - Unless otherwise specified, V_{IC} = 0V, $\pm V_{CC}$ = ±15V. Limits apply QP111 and to each half of QP2111.

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /10 -55ºC ≤T_A≤+125ºC Unless Otherwise Specified	Min	Max	Unit
Input Offset Voltage	V_{IO}	R_S=50Ω, V_{IC}=0V, V_{supply} 13V & -14.5V T_A=25ºC	-3.0	+3.0	mV
		/8 T_A= –55ºC or 125ºC	-4.0	+4.0	mV
		R_S=50Ω, V_{IC}=0V, V_{supply} 2.5V & -2.5V T_A=25ºC	-3.0	+3.0	mV
		/8 T_A= –55ºC or 125ºC	-4.0	+4.0	mV
Raised Input Offset Voltage /9	$V_{IO(R)}$	R_S=50Ω, V_{IC}=0V, V_{supply} 13V & -14.5V T_A=25ºC	-3.0	+3.0	mV
		/8 V_{BAL}=$V_{BAL/STB}$=$+V_{CC}$ T_A= –55ºC or 125ºC	-4.5	+4.5	mV

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /10 -55ºC ≤T_A≤+125ºC Unless Otherwise Specified	Min	Max	Unit
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$	R_S=50Ω	-25.0	+25.0	µV/ºC
Input Offset Current	I_{IO}	R_S=50KΩ, V_{IC}=0V, V_{supply} 13V & -14.5V T_A=25ºC & 125ºC	-10.0	+10.0	nA
		/8 T_A= –55ºC	-20.0	+20.0	nA
Raised Input Offset Current /9	$I_{IO(R)}$	R_S=50KΩ, V_{IC}=0V, V_{supply} 13V & -14.5V T_A=25ºC & 125ºC	-25.0	+25.0	nA
		/8 V_{BAL}=$V_{BAL/STB}$=+V_{CC} T_A= –55ºC	-50.0	+50.0	nA
Input Offset Voltage Temperature Coefficient	$\Delta I_{IO}/\Delta T$	R_S=50Ω T_A=25 / 125ºC	-100.0	+100.0	pA/ºC
		T_A=25 / -55ºC	-200.0	+200.0	pA/ºC
Input Bias Current	$+I_{IB}$	R_S=50KΩ, V_{IC}=0V T_A=25ºC & 125ºC	-100.0	+0.1	nA
		T_A= –55ºC	-150.0	+0.1	nA
		R_S=50KΩ, V_{IC}= 13V & -14.5V T_A=25ºC & 125ºC	-150.0	+0.1	nA
		T_A= –55ºC	-200.0	+0.1	nA
Input Bias Current	$-I_{IB}$	R_S=50KΩ, V_{IC}=0V T_A=25ºC & 125ºC	-100.0	+0.1	nA
		T_A= –55ºC	-150.0	+0.1	nA
		R_S=50KΩ, V_{IC}= 13V & -14.5V T_A=25ºC & 125ºC	-150.0	+0.1	nA
		T_A= –55ºC	-200.0	+0.1	nA
Collector Output Voltage (Strobed)	$V_{O(STB)}$	R_S=50Ω, I_{STB}= -3.0mA	+14.0		V
Common Mode Rejection Ratio	CMRR	R_S=50Ω, V_{IC}= 13V & -14.5V	+80.0		dB
Output Leakage Current	I_{CEX}	±V_{CC}= ±18V T_A=25ºC	-1.0	+10.0	nA
		V_{OUT}= 32V T_A=125ºC	-1.0	+500.0	nA
Input Leakage Current	I_{I1}	±V_{CC}= ±18V V_{ID}= +29V	-5.0	+500.0	nA
	I_{I2}	±V_{CC}= ±18V V_{ID}= -29V	-5.0	+500.0	nA

TABLE I – ELECTRICAL PERFORMANCE CHARACTERISTICS

Test	Symbol	Conditions /10 $-55^oC \le T_A \le +125^oC$ Unless Otherwise Specified	Min	Max	Unit
Positive Supply Current	$+I_{CC}$	T_A= -55ºC		+7.0	mA
(Limit is for one comparator.)		T_A= 25ºC		+6.0	mA
		T_A= 125ºC		+6.0	mA
Negative Supply Current	$-I_{CC}$	T_A= -55ºC	-6.0		mA
(Limit is for one comparator.)		T_A= 25ºC	-5.0		mA
		T_A= 125ºC	-5.0		mA
Short Circuit Current	I_{OS}	T_A= -55ºC		-250	mA
Duration not to exceed 10ms, one output at a time		T_A= 25ºC		-200	mA
		T_A= 125ºC		-150	mA
Adjustment for	$V_{IO(ADJ)+}$	R_S=50Ω, T_A= 25ºC	+5.0		mV
Input Offset Voltage	$V_{IO(ADJ)-}$	R_S=50Ω, T_A= 25ºC		-5.0	mV
Low Level Output Voltage	V_{OL1} V_{OL2}	$+V_{CC}$=+4.5V, $-V_{CC}$=0V, V_{IC}= -1.75V, +0.75V, V_{ID}=-6.0mV, I_O= 8mA		0.4 0.4	V V
	V_{OL3} V_{OL4}	$\pm V_{CC}$= ±15V, V_{IC}= 13V, -14V, V_{ID}=-5.0mV, I_O= 50mA		1.5 1.5	V V
Voltage Gain	$\pm A_{VE}$	R_L= 600Ω, T_A= 25ºC	+10.0		V/mV
(emitter follower output)		T_A= -55ºC, +125ºC	+8.0		V/mV
Response Time, Low to High Level Collector Output	t_{RLHC}	T_A= 25ºC, -55ºC V_{0D}= -5mV, C_L=50pF, V_{IN}=100mV		300	ns
		T_A=125ºC		640	ns
Response Time, High to Low Level Collector Output	t_{RHLC}	T_A= 25ºC, -55ºC V_{0D}= +5mV, C_L=50pF, V_{IN}=100mV		300	ns
		T_A=125ºC		500	ns

Ordering Information

Part Number	Package (Mil-Std-1835)	Generic
5962-86877012A	CQCC1-N20 (LLCC)	QP111
5962-86877012C *	CQCC1-N20 (LLCC)	QP111
5962-8687701GA	MACY1-X8 (Metal CAN)	QP111
5962-8687701PA	CDIP2-T8 (CERDIP)	QP111
5962-8687701PC *	GDIP1-T8 (Dual-in-Line)	QP111
5962-8687701Q2A	CQCC1-N20 (LLCC)	QP111
5962-8687701Q2C *	CQCC1-N20 (LLCC)	QP111
5962-8687701QGA	MACY1-X8 (Metal CAN)	QP111

Part Number		Package (Mil-Std-1835)	Generic
5962-8687701QPA		CDIP2-T8 (CERDIP)	QP111
5962-8687701QPC	*	GDIP1-T8 (Dual-in-Line)	QP111
5962-8687701QZA		GDFP1-G10 (Gull Wing Flatpack)	QP111
5962-8687701QZC	*	GDFP1-G10 (Gull Wing Flatpack)	QP111
JM38510-10304B2A		CQCC1-N20 (LLCC)	QP111
JM38510-10304B2C	*	CQCC1-N20 (LLCC)	QP111
JM38510-10304BAA		CDFP6-F14 (FLATPACK)	QP111
JM38510-10304BAC	*	GDFP5-F14 (FLATPACK)	QP111
JM38510-10304BCA		CDIP2-T14 (CERDIP)	QP111
JM38510-10304BCC	*	GDIP1-T14 (Dual-in-Line)	QP111
JM38510-10304BGA		MACY1-X8 (Metal CAN)	QP111
JM38510-10304BHA		CDFP2-F10 (FLATPACK)	QP111
JM38510-10304BHC	*	GDFP1-F10 (FLATPACK)	QP111
JM38510-10304BPA		CDIP2-T8 (CERDIP)	QP111
JM38510-10304BPC	*	GDIP1-T8 (Dual-in-Line)	QP111
JM38510-10305BEA		CDIP2-T16 (CERDIP)	QP2111
JM38510-10305BEC	*	GDIP1-T16 (Dual-in-Line)	QP2111
JM38510-10305BFA		CDFP3-F16 (CERPACK)	QP2111
JM38510-10305BFC	*	GDFP2-F16 (FLATPACK)	QP2111

* denotes Lead Free Lead Finish

In addition to those products listed above, QP Semiconductor supports Industrial Temperature Range, Source Control Drawing (SCD), and custom package development for this product family.

Notes:

Package outline information and specifications are defined by Mil-Std-1835 package dimension requirements.

Products manufactured by QP Semiconductor are compliant to the assembly, burn-in, test and quality conformance requirements of Test Methods 5004 & 5005 of Mil-Std-883 for Class B or Q devices as appropriate. The appropriate DSCC Detail Specifications define the electrical test requirements for each device.

The listed drawings, Mil-PRF-38535, Mil-Std-883 and Mil-Std-1835 are available online at http://www.dscc.dla.mil/

Additional information is available at our website http://www.qpsemi.com

Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the QP111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs and also away from Balance and Balance/Strobe pins. However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the QP111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 1 below.

1. The trim pins (Balance and Balance/Strobe) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between Balance and Balance/Strobe will minimize the susceptibility to AC coupling. A smaller capacitor is used if Balance is used for positive feedback as in Figure 1.

2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.

3. When the signal source is applied through a resistive network, RS, it is usually advantageous to choose an RS' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.

4. When comparator circuits use input resistors (e.g. Summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if RS=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the QP111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If Balance and Balance/Strobe are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the QP111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Balance/Strobe and the Output. The power supply bypass capacitors should be located within a couple inches of the QP111. It is better if the power-supply bypass capacitors are located immediately adjacent to the comparator.

6. It is standard procedure to use Hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of Figure 2, the feedback from the output to the positive input will cause about 3 mV of Hysteresis. However, if RS is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of Figure 3 could be used, but it is rather awkward. See the notes in paragraph 7 below.

7. When both inputs of the QP111 are connected to active signals, or if a high-impedance signal is driving the positive input of the QP111 so that positive feedback would be disruptive, the circuit of Figure 1 is ideal. The positive feedback is to Balance pin (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV Hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82W resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at the Balance pin, so this feedback does not add to the VOS of the comparator. As much as 8 mV of VOS can be trimmed out, using a 5 kΩ pot and 3 kΩ resistor as shown.

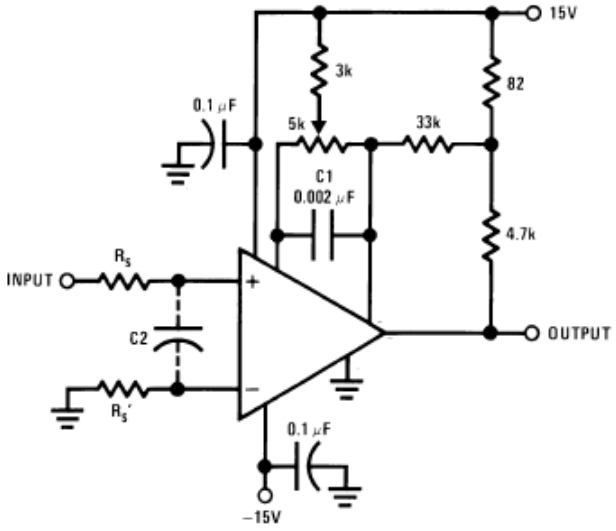


FIGURE 1. Improved Positive Feedback

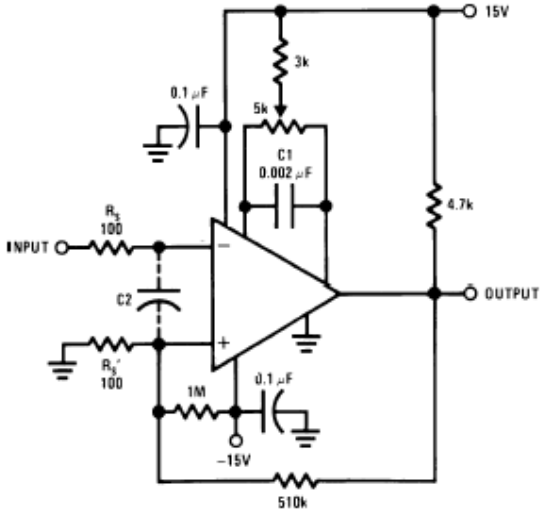


FIGURE 2. Conventional Positive Feedback

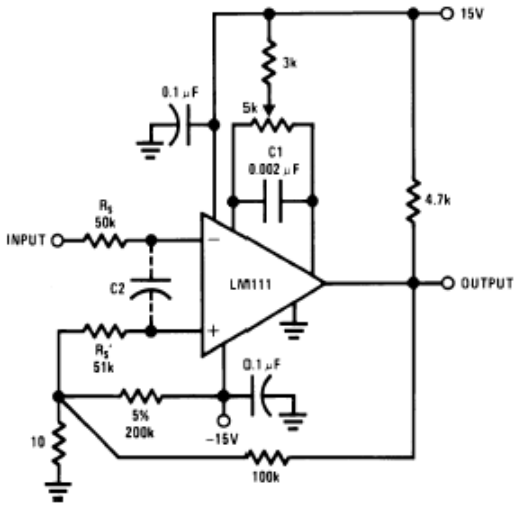


FIGURE 3. Positive Feedback with High Source Resistance