

# High-speed dual-differential comparator/sense amp

NE/SE521

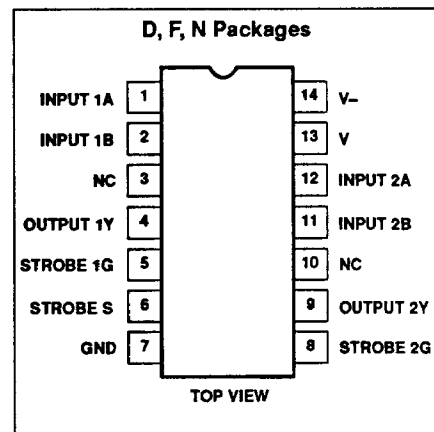
## FEATURES

- 12ns maximum guaranteed propagation delay
- 20µA maximum input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

## APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

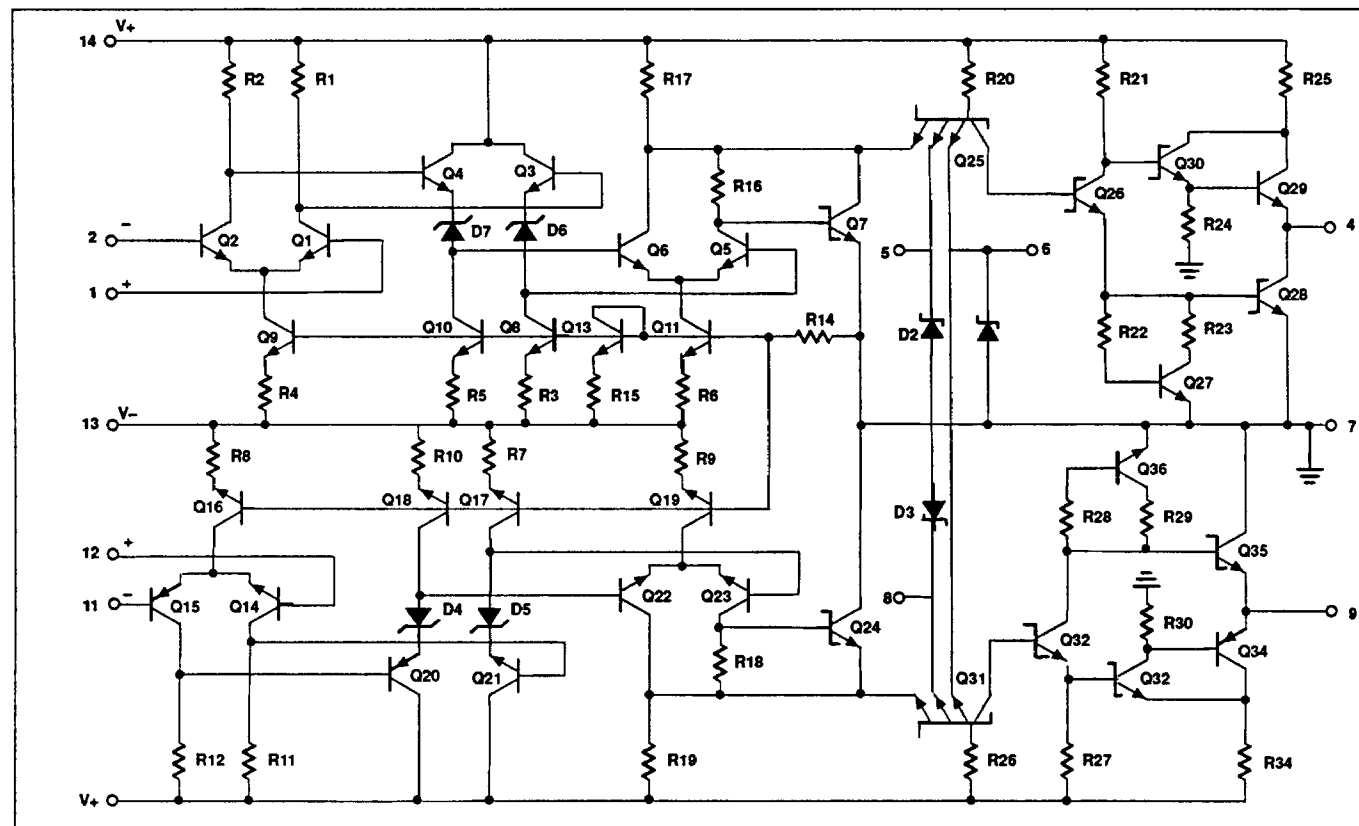
## PIN CONFIGURATION



## ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE521N
14-Pin SO Package	0 to +70°C	NE521D
14-Pin Cerdip	0 to +70°C	NE521F
14-Pin Cerdip	-55°C to +125°C	SE521F

## EQUIVALENT SCHEMATIC



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## LOGIC FUNCTIONS

$V_{ID}$ A+, B-	STROBE S	STROBE G	OUTPUT (Y)
$V_{ID} \leq V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geq V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

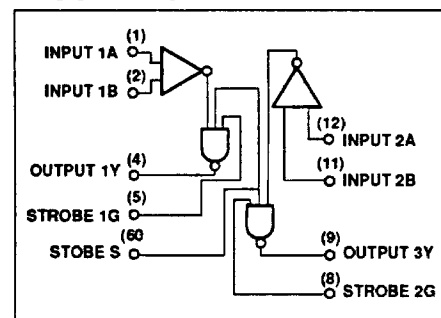
## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage		
	Positive	+7	V
V-	Negative	-7	V
$V_{IDR}$	Differential input voltage	$\pm 6$	V
$V_{IN}$	Input voltage		
	Common mode	$\pm 5$	V
	Strobe/gate	+5.25	V
$P_D$	Maximum power dissipation <sup>1</sup>		
	$T_A = 25^\circ\text{C}$ (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
$T_A$	Operating temperature range		
	NE521	0 to 70	$^\circ\text{C}$
	SE521	-55 to +125	$^\circ\text{C}$
$T_{STG}$	Storage temperature range	-65 to +150	$^\circ\text{C}$
$T_{SOLD}$	Lead soldering temperature (10 sec. max)	+300	$^\circ\text{C}$

### NOTES:

- Derate above  $25^\circ\text{C}$  at the following rates:  
 F package at  $9.5\text{mW}/^\circ\text{C}$   
 N package at  $11.4\text{mW}/^\circ\text{C}$   
 D package at  $8.3\text{mW}/^\circ\text{C}$

## BLOCK DIAGRAM



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**DC ELECTRICAL CHARACTERISTICS (SE521)**V<sub>+</sub>=+5V, V<sub>-</sub>=-5V, T<sub>A</sub>=-55°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V <sub>OS</sub>	Input offset voltage At 25°C Over temperature range	V <sub>+</sub> =+4.5V, V <sub>-</sub> =-4.5V		6	7.5 15	mV
I <sub>BIAS</sub>	Input bias current At 25°C Over temperature range	V <sub>+</sub> =+5.5V, V <sub>-</sub> =-5.5V		7.5	20 40	μA
I <sub>OS</sub>	Input offset current At 25°C Over temperature range	V <sub>+</sub> =+5.5V, V <sub>-</sub> =-5.5V		1.0	5 12	μA
V <sub>CM</sub>	Common-mode voltage range	V <sub>+</sub> =+4.5V, V <sub>-</sub> =-4.5V	-3		+3	V
V <sub>IL</sub>	Low level input voltage At 25°C Over temperature				0.8 0.7	V
V <sub>IH</sub>	High level input voltage		2.0			V
I <sub>IH</sub>	Input current High	V <sub>+</sub> =+5.5V, V <sub>-</sub> =-5.5V V <sub>IH</sub> =2.7V 1G or 2G strobe Common strobe S			50 100	μA μA
I <sub>IL</sub>	Input Current Low	V <sub>IL</sub> =0.5V 1G or 2G strobe Common strobe S			-2.0 -4.0	mA mA
V <sub>OH</sub>	Output voltage High	V <sub>(S)</sub> =2.0V V <sub>+</sub> =+4.5V, V <sub>-</sub> =-4.5V, I <sub>LOAD</sub> =1mA	2.5	3.4		V
V <sub>OL</sub>	Low	V <sub>+</sub> =+4.5V, V <sub>-</sub> =-4.5V, I <sub>LOAD</sub> =10mA T <sub>A</sub> =25°C, I <sub>LOAD</sub> =20mA			0.5 0.5	
V <sub>+</sub> V <sub>-</sub>	Supply voltage Positive Negative		4.5 -4.5	5.0 -5.0	5.5 -5.5	V
I <sub>CC+</sub> I <sub>CC-</sub>	Supply current Positive Negative	V <sub>+</sub> =5.5V, V <sub>-</sub> =-5.5V, T <sub>A</sub> =25°C		27 -15	35 -28	mA
I <sub>SC</sub>	Short-circuit output current		-35		-115	mA

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**DC ELECTRICAL CHARACTERISTICS(NE521)**V<sub>+</sub>=+5V, V<sub>-</sub>=-5V, T<sub>A</sub>=0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V <sub>OS</sub>	Input offset voltage At 25°C Over temperature range	V <sub>+</sub> =+4.75V, V <sub>-</sub> =-4.75V		6	7.5 10	mV
I <sub>BIAS</sub>	Input bias current At 25°C Over temperature range	V <sub>+</sub> =+5.25V, V <sub>-</sub> =-5.25V		7.5	20 40	μA
I <sub>OS</sub>	Input offset current At 25°C Over temperature range	V <sub>+</sub> =+5.25V, V <sub>-</sub> =-5.25V		1.0	5 12	μA
V <sub>CM</sub>	Common-mode voltage range	V <sub>+</sub> =+4.75V, V <sub>-</sub> =-4.75V	-3		+3	V
I <sub>IH</sub>	Input current High	V <sub>+</sub> =+5.25V, V <sub>-</sub> =-5.25V V <sub>IH</sub> =2.7V 1G or 2G strobe Common strobe S			50 100	μA μA
I <sub>IL</sub>	Input Current Low	V <sub>IL</sub> =0.5V 1G or 2G strobe Common strobe S			-2.0 -4.0	mA mA
V <sub>OH</sub> V <sub>OL</sub>	Output voltage High Low	V <sub>(KS)</sub> =2.0V V <sub>+</sub> =+4.75V, V <sub>-</sub> =-4.75V, I <sub>LOAD</sub> =-1mA V <sub>+</sub> =+5.25V, V <sub>-</sub> =-5.25V, I <sub>LOAD</sub> =20mA	2.7	3.4	0.5	V
V <sub>+</sub> V <sub>-</sub>	Supply voltage Positive Negative		4.75 -4.75	5.0 -5.0	5.25 -5.25	V
I <sub>CC+</sub> I <sub>CC-</sub>	Supply current Positive Negative	V <sub>+</sub> =5.25V, V <sub>-</sub> =-5.25V, T <sub>A</sub> =25°C		27 -15	35 -28	mA
I <sub>SC</sub>	Short-circuit output current		-40		-100	mA

**AC ELECTRICAL CHARACTERISTICS**T<sub>A</sub>=25°C, R<sub>L</sub>=280Ω C<sub>L</sub>=15pF V<sub>+</sub>=5V V<sub>-</sub>=-5V.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
<b>Large-signal switching speed</b>							
t <sub>PLH(D)</sub>	Propagation delay Low to high <sup>1</sup>	Amp	Output		8	12	ns
t <sub>PHL(D)</sub>	High to low <sup>1</sup>	Amp	Output		6	9	
t <sub>PLH(S)</sub>	Low to high <sup>2</sup>	Strobe	Output		4.5	10	
t <sub>PHL(S)</sub>	High to low <sup>2</sup>	Strobe	Output		3.0	6	
f <sub>MAX</sub>	Max. operating frequency			40	55		

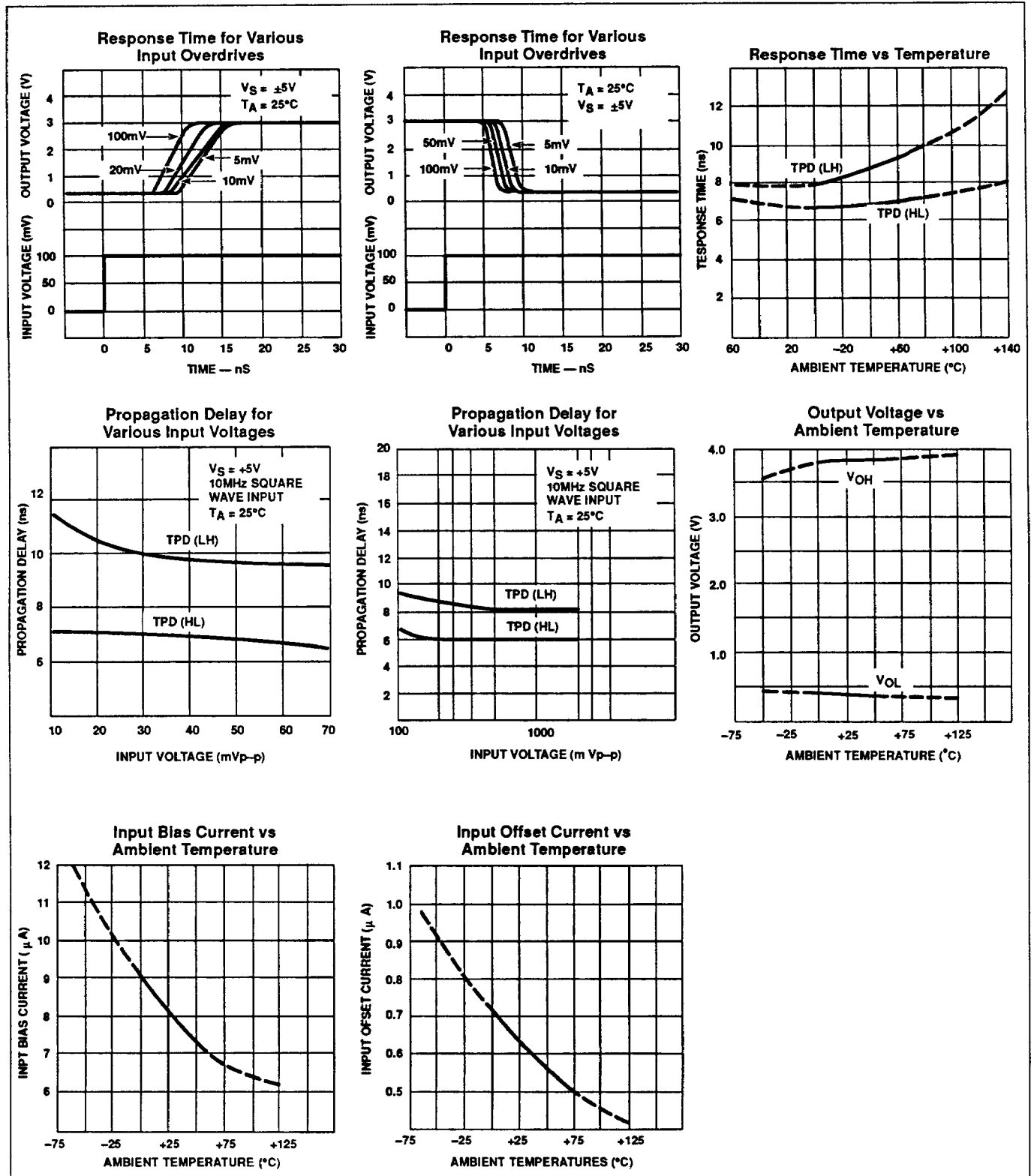
**NOTES:**

- Response time measured from 0V point of ±100mV<sub>p-p</sub> 10MHz square wave to the 1.5V point of the output.
- Response time measured from 1.5V point of input to 1.5V point of the output.

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## TYPICAL PERFORMANCE CHARACTERISTICS



# Signetics

# Packaging Information

T.90-20

## Military Products

### SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-In-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.

- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt <sup>4</sup>
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X <sup>2</sup>	28
24DIP6	D-3	J	28
28DIP6	D-10	X <sup>2</sup>	28
40DIP6	D-5	Q	28
48DIP6	D-14 <sup>1</sup>	X <sup>2</sup>	28
50DIP9	D-12 <sup>1</sup>	X <sup>2</sup>	28
64DIP9	D-13 <sup>1</sup>	X <sup>2</sup>	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y <sup>2</sup>	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y <sup>2</sup>	22
52FLAT	Y-1 <sup>1</sup>	Y <sup>2</sup>	22
18LLCC	C-9	U <sup>2</sup>	20
20LLCC	C-2 <sup>3</sup>	2	20
28LLCC	C-4 <sup>3</sup>	3	20
32LLCC	C-12	U <sup>2</sup>	20
44LLCC	C-5	U <sup>2</sup>	20
68LLCC	C-7	U <sup>2</sup>	20
68PGA	P-AB	Z <sup>2</sup>	20
84PGA	P-AB	Z <sup>2</sup>	20

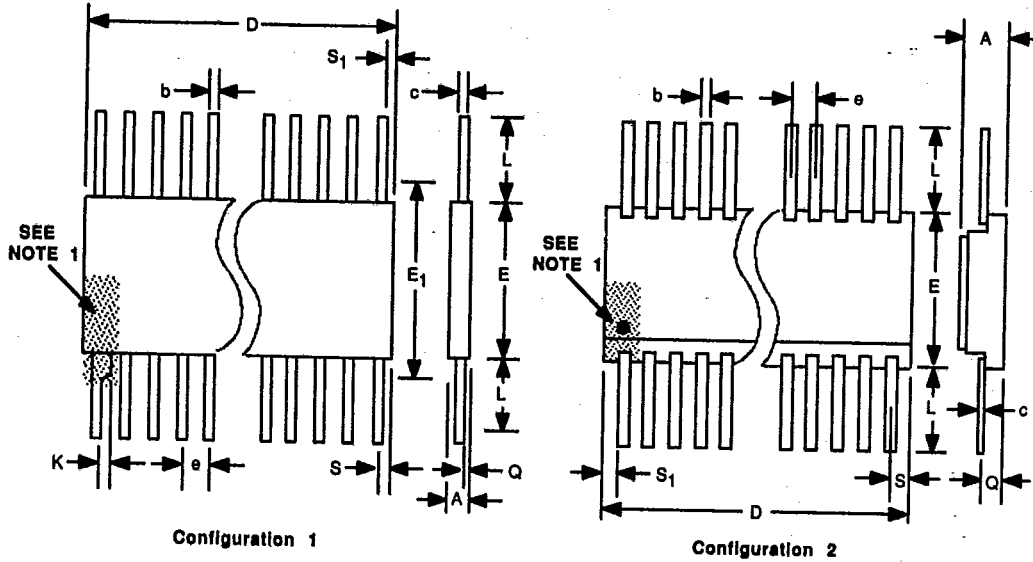
**NOTES:**

1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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CASE OUTLINES Y (FLAT PACKAGES)



NOTES:

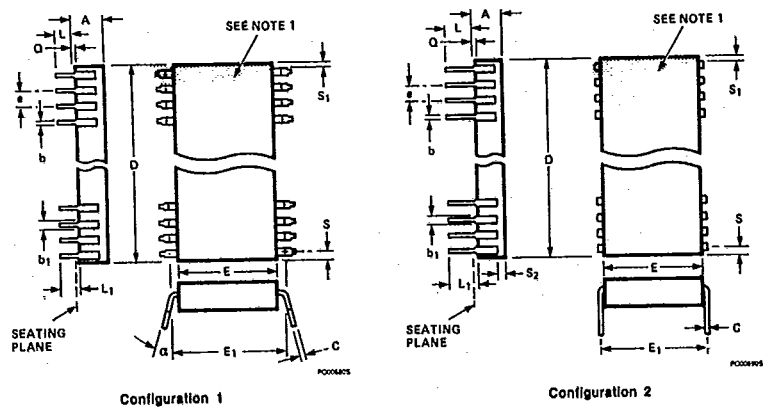
1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within  $\pm 0.005$  of its longitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	6
b	0.015	0.026	
c	0.008	0.015	
D	-	1.330	2
E	0.620	0.660	3
e	0.050 BSC		
L	0.250	0.370	4
Q	0.054	0.0666	
S	-	0.045	5
S1	0.005	-	5

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**Packaging Information**

**CASE OUTLINES X (DUAL IN-LINE PACKAGES)**



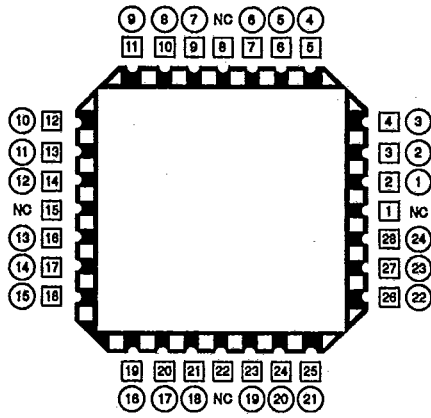
1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within  $\pm 0.010$  of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.



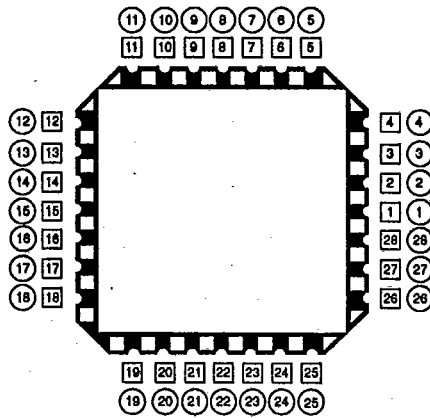
Packaging Information

T-90-20

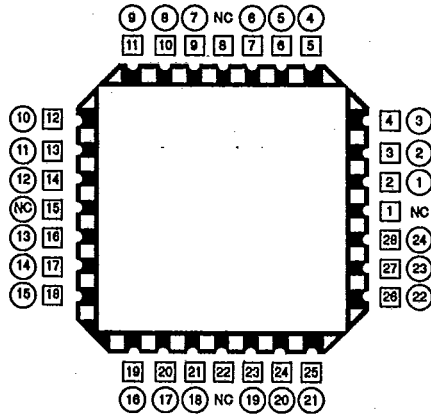
LEADLESS CHIP CARRIER (LLCC) PINOUTS



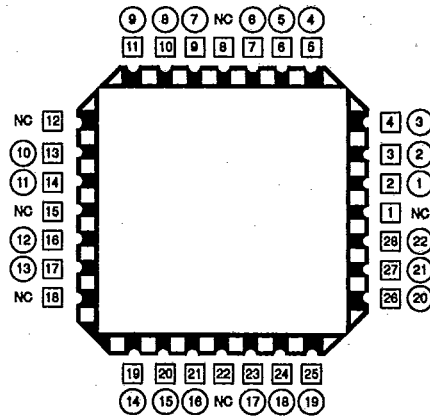
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number  
 ○ = Dual In-Line Lead Number  
 NC = No Connect