National Semiconductor

74F269
8-Bit Bidirectional Binary Counter

General Description

The 'F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

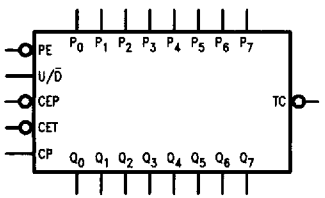
- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 100 MHz
- Supply current 113 mA typ
- 300 mil slimline package

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F269SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F269SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbols



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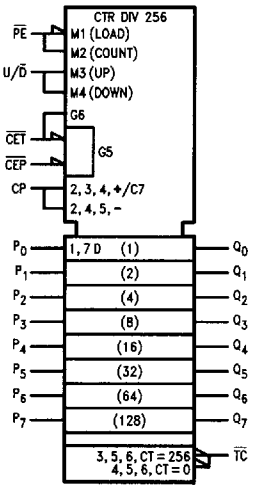
IEEE/IEC



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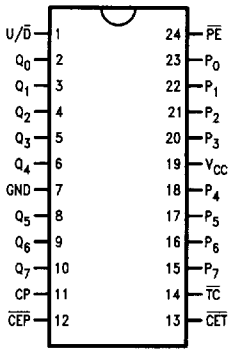
Connection Diagram

Pin Assignment for DIP and SOIC



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Function Table

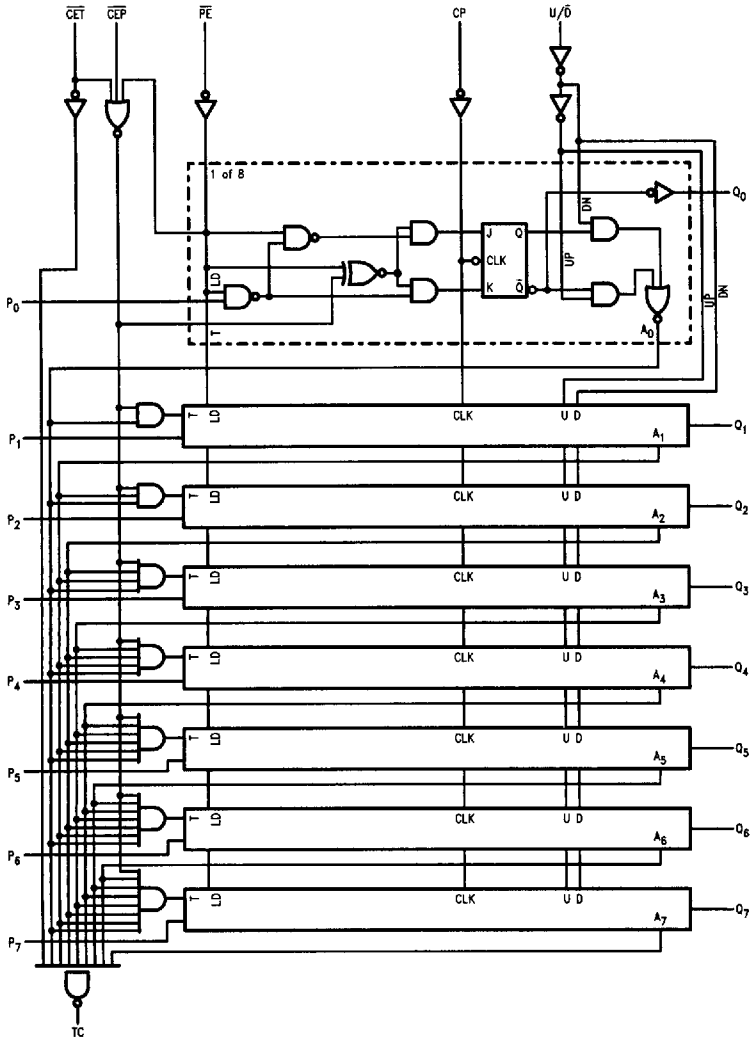
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ($\overline{TC}$ Held HIGH)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = Transition LOW-to-HIGH

Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0–P_7	Parallel Data Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$U/\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 μA/−0.6 mA
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
CP	Clock Input	1.0/1.0	20 μA/−0.6 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	5.0/33.3	−1 mA/20 mA
Q_0–Q_7	Flip-Flop Outputs	50/33.3	−1 mA/20 mA

Logic Diagram



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			104	125	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			113	135	mA	Max	V_O = LOW

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100			85		MHz	2-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Count-Up)	3.5 4.5		8.0 10.5	3.5 4.5	7.0 11.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.5 4.5		7.5 7.5	3.5 4.5	10.0 11.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.5 3.0		7.0 10.5	3.5 3.0	10.5 11.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	4.5 5.0		10.0 10.0	4.5 4.5	10.5 10.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Count-Down)	3.5 4.5		10.5 10.5	3.5 4.5	11.0 11.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load)	3.5 4.0		7.0 7.0	3.5 4.0	10.0 7.0	ns	2-3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		74F T_A, V_{CC} = Com		Units	Fig. No.
		Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Data to CP	3.5 3.0		4.0 3.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Data to CP	1.0 1.0		2.0 1.0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.5 5.5		6.5 6.5		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0		0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	6.0 8.0		6.5 9.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CET}$ or $\overline{CEP}$ to CP	0 0		0 0			
$t_w(H)$ $t_w(L)$	Clock Pulse Width, HIGH or LOW	3.5 3.5		3.5 4.0		ns	2-4
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	8.0 6.0		9.5 7.0		ns	2-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0.0 0.0		0.0 0.0		ns	2-6