

## 54ACT534 Octal D Flip-Flop with TRI-STATE® Outputs

### General Description

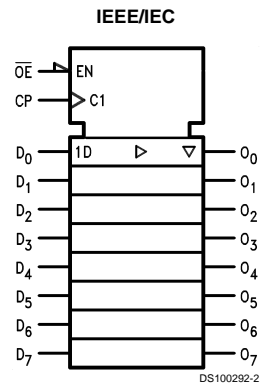
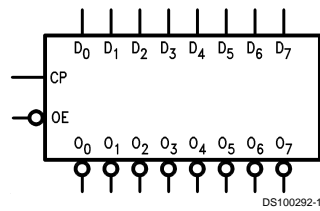
The 'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374
- Standard Microcircuit Drawing (SMD) 5962-8965801

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%

### Logic Symbols

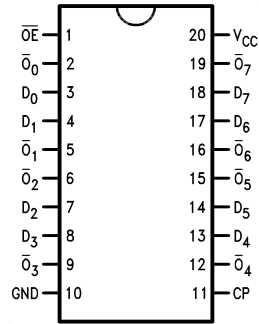


Pin Names	Description
$D_0$ – $D_7$	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$ – $\overline{O}_7$	Complementary TRI-STATE Outputs

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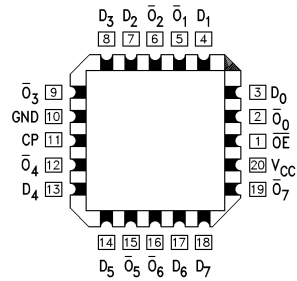
## Connection Diagrams

Pin Assignment  
for DIP and Flatpak



DS100292-3

Pin Assignment  
for LCC



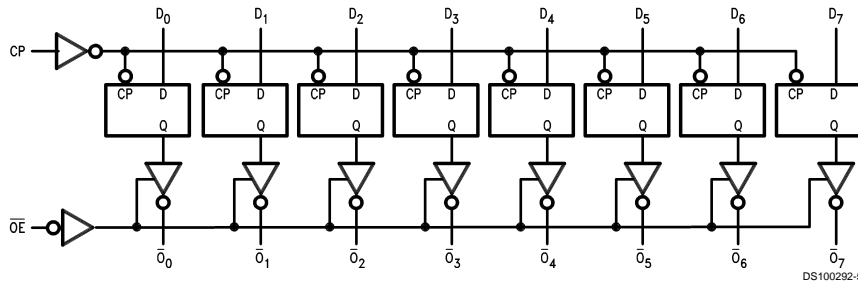
DS100292-4

## Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold

times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Logic Diagram



DS100292-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
↗	L	H	L
↗	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Clock Transition  
 Z = High Impedance  
 $\overline{O}_0$  = Value stored from previous clock cycle

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

Junction Temperature ( $T_J$ )

CDIP

175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## DC Characteristics for 'ACT Family Devices

Symbol	Parameter	$V_{CC}$ (V)	54ACT		Units	Conditions	
			$T_A =$ -55°C to +125°C				
			Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	2.0				
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8		V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	0.8				
$V_{OH}$	Minimum High Level Output Voltage	4.5	4.4		V	$I_{OUT} = -50 \mu A$	
		5.5	5.4				
			4.5	3.70		V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
			5.5	4.70			
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1		V	$I_{OUT} = 50 \mu A$	
		5.5	0.1				
			4.5	0.50		V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$
			5.5	0.50			
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0		µA	$V_I = V_{CC}, GND$	
$I_{OZ}$	Maximum TRI-STATE Current	5.5	±5.0		µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$	
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6		mA	$V_I = V_{CC} - 2.1V$	
$I_{OLD}$	Minimum Dynamic	5.5	50		mA	$V_{OLD} = 1.65V$ Max	
$I_{OHD}$	Output Current (Note 3)	5.5	-50		mA	$V_{OHD} = 3.85V$ Min	
$I_{CC}$	Maximum Quiescent Supply Current	5.5	80.0		µA	$V_{IN} = V_{CC}$ or GND	

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:**  $I_{CC}$  for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	5.0	85		MHz	
t <sub>PLH</sub>	Propagation Delay CP to $\overline{Q}_n$	5.0	1.5	14.0	ns	
t <sub>PHL</sub>	Propagation Delay CP to $\overline{Q}_n$	5.0	1.5	13.0	ns	
t <sub>PZH</sub>	Output Enable Time	5.0	1.5	14.0	ns	
t <sub>PZL</sub>	Output Enable Time	5.0	1.5	13.0	ns	
t <sub>PHZ</sub>	Output Disable Time	5.0	1.5	14.5	ns	
t <sub>PLZ</sub>	Output Disable Time	5.0	1.5	11.5	ns	

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

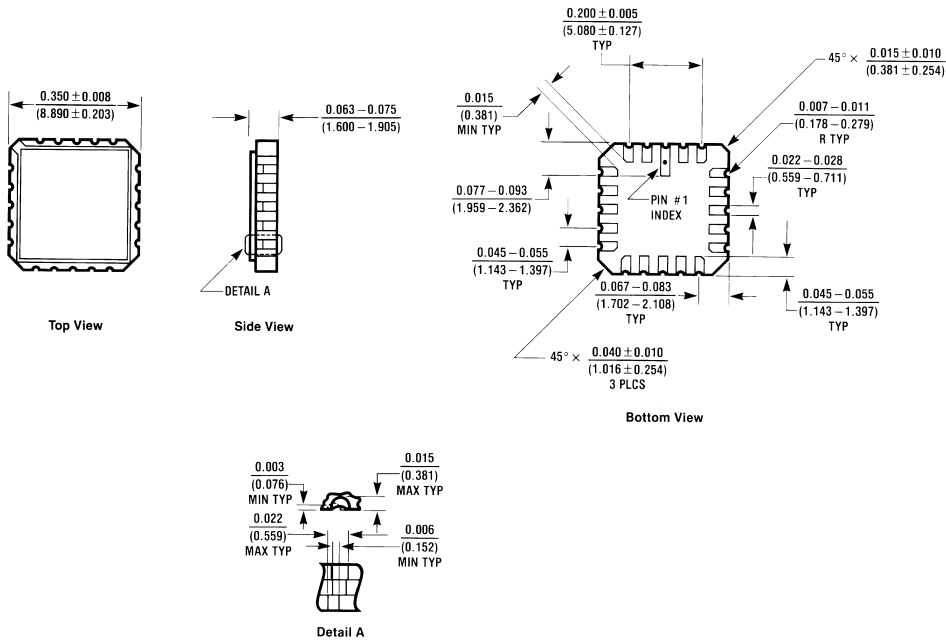
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	54ACT		Units	Fig. No.
			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF			
			Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D <sub>n</sub> to CP	5.0	5.0		ns	
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	3.0		ns	
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	5.0		ns	

Note 6: Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

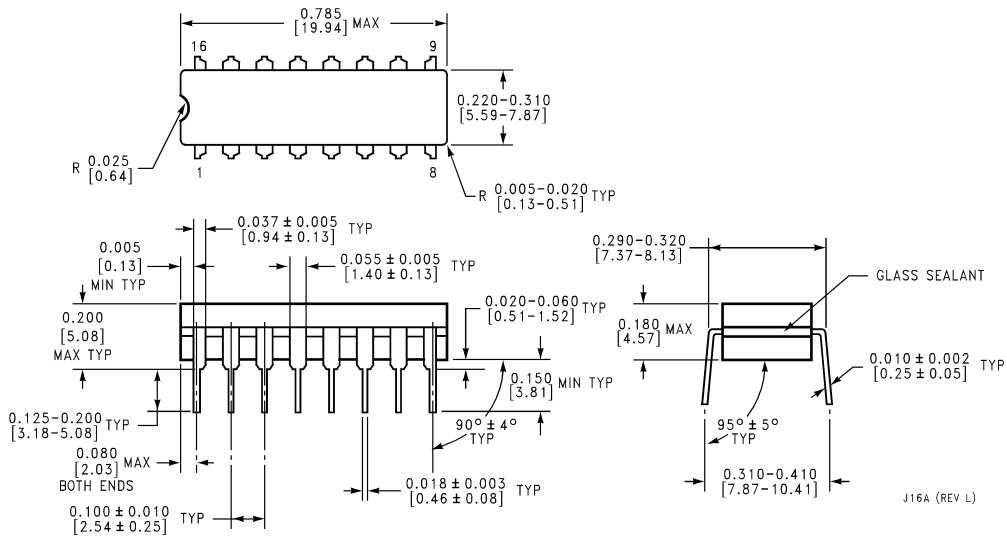
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	40.0	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20 Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E20A

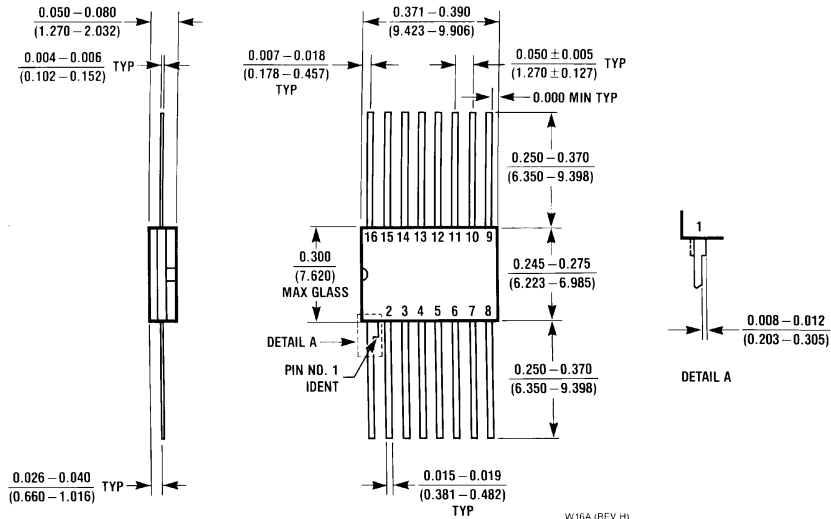
E20A (REV D)



**16 Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J16A

J16A (REV L)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16 Lead Ceramic Flatpak (F)  
NS Package Number W16A**

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**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

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