National Semiconductor

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54ABT240
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

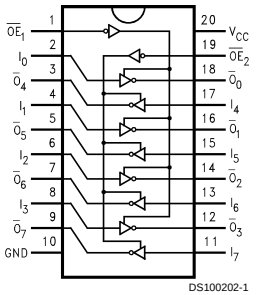
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) — 5962-9318801

Ordering Code

Military	Package Number	Package Description
54ABT240J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT240W-QML	W20A	20-Lead Cerpack
54ABT240E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

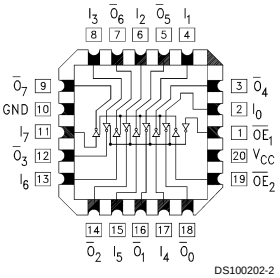
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100202-1

Pin Assignment for LCC



DS100202-2

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

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Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	−150 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT240 Min	ABT240 Typ	ABT240 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	μA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	μA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}_n$ = V_{CC};
								All Others at V_{CC} or Ground
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			1.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			1.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			50	μA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or Ground
I_{CCD}	Dynamic I_{CC}	No Load				mA/	Max	Outputs Open
	(Note 4)				0.1	MHz		$\overline{OE}_n$ = GND, (Note 3)
								One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

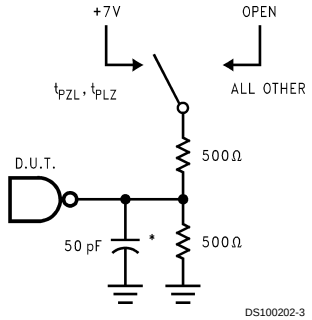
Symbol	Parameter	54ABT $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF		Units	Fig. No.
		Min	Max		
t_{PLH}	Propagation Delay	0.8	5.5	ns	*Figure 5*
t_{PHL}	Data to Outputs	1.0	5.5		
t_{PZH}	Output Enable	0.8	7.5	ns	*Figure 4*
t_{PZL}	Time	0.8	7.7		
t_{PHZ}	Output Disable	1.0	7.5	ns	*Figure 4*
t_{PLZ}	Time	1.0	7.2		

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ C$
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	V_{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

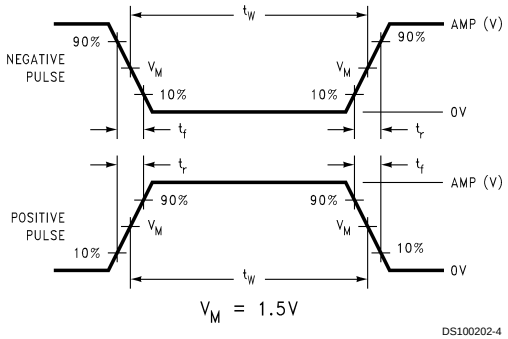


FIGURE 2. Test Input Signal Levels

AC Waveforms

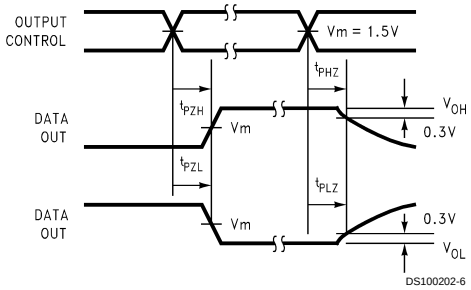


FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

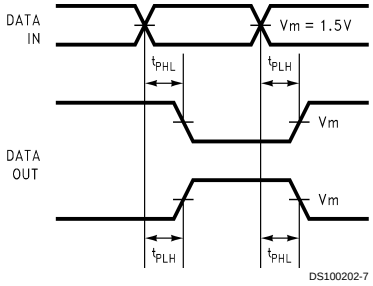
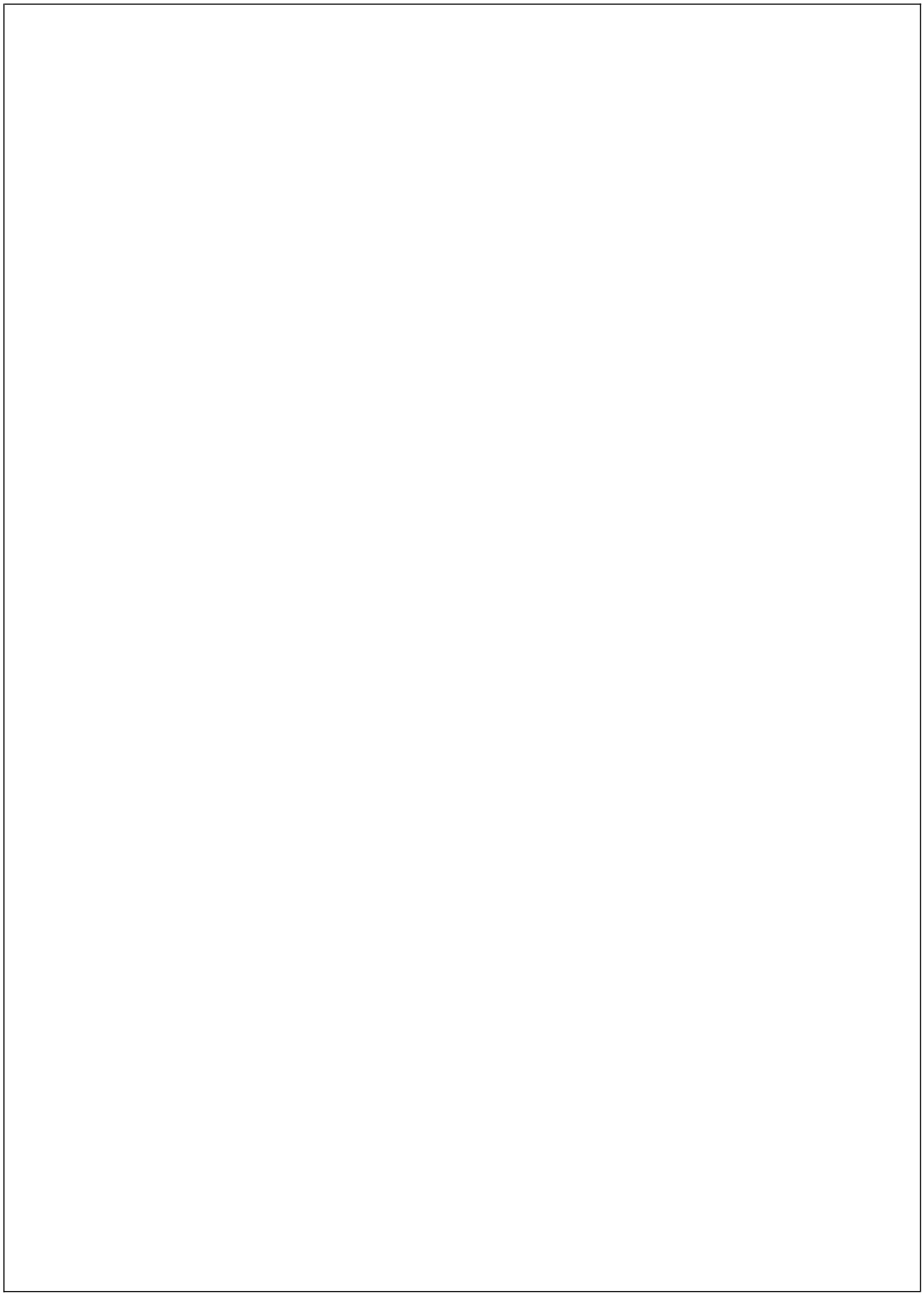
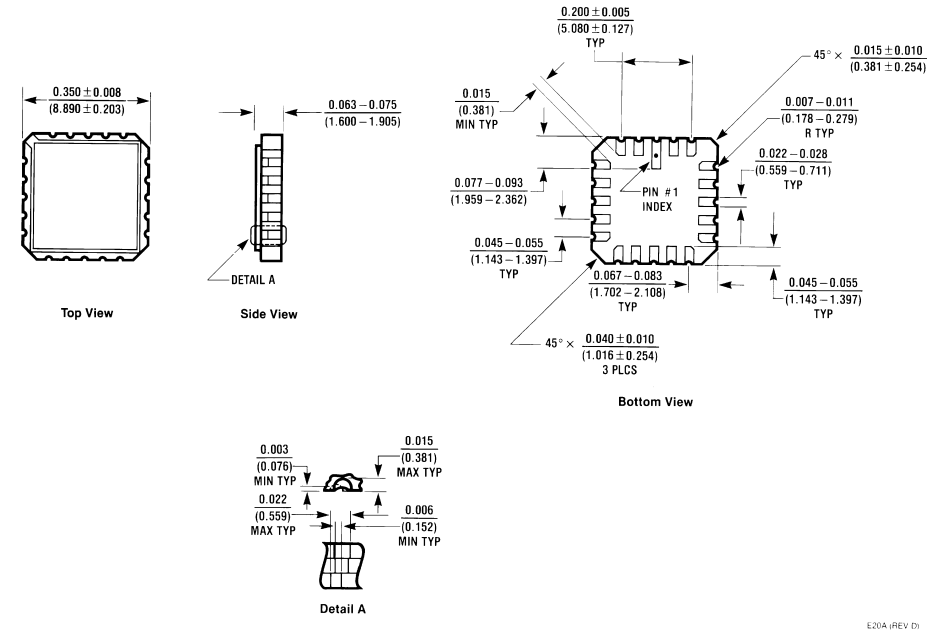


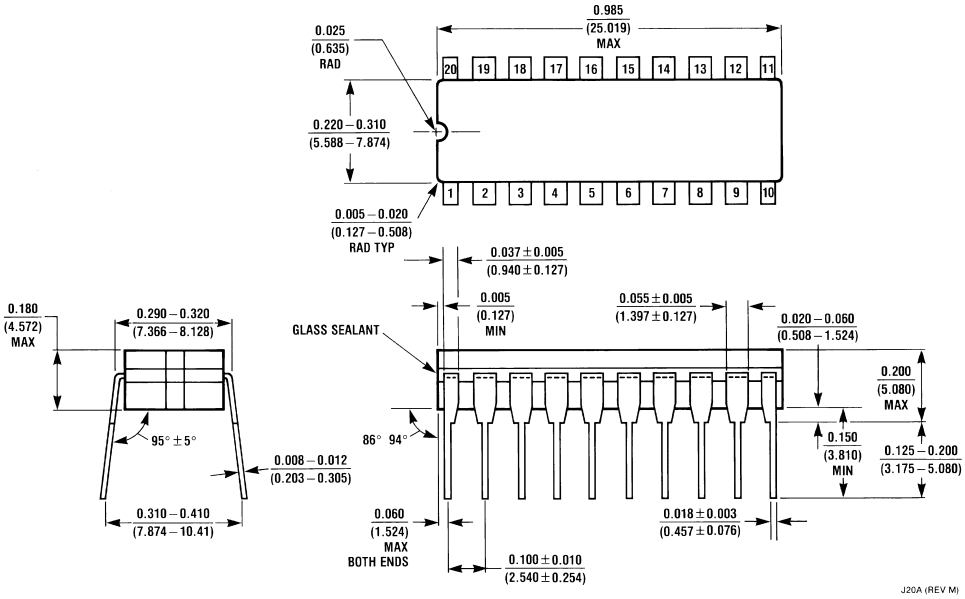
FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



Physical Dimensions inches (millimeters) unless otherwise noted

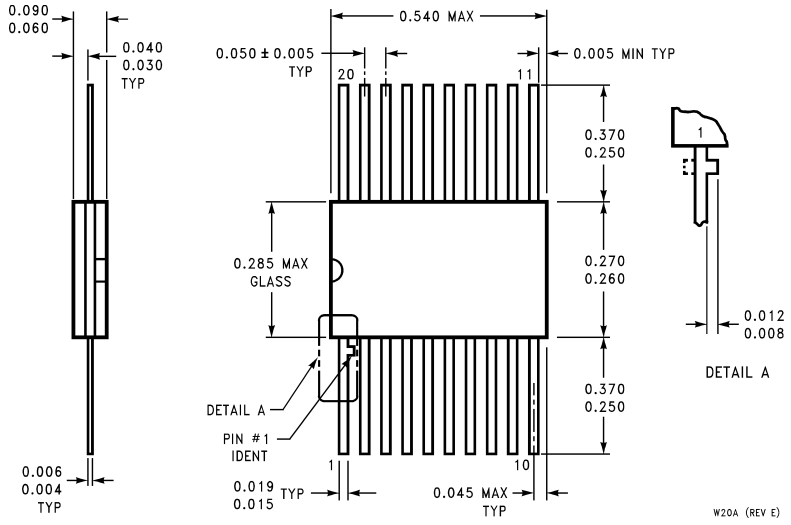


20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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