National Semiconductor

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100341
Low Power 8-Bit Shift Register

General Description

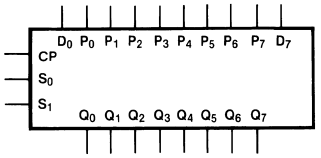
The 100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Features

- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/function compatible with 100141
- Voltage compensated operating range = −4.2V to −5.7V
- Standard Microcircuit Drawing (SMD) 5962-9459101

Logic Symbol

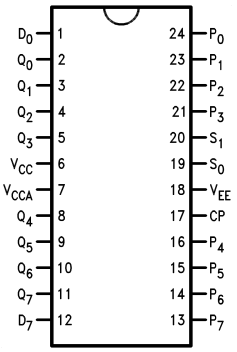


DS100315-1

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

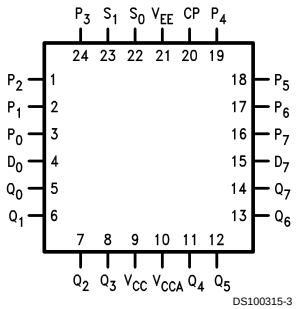
Connection Diagrams

24-Pin DIP



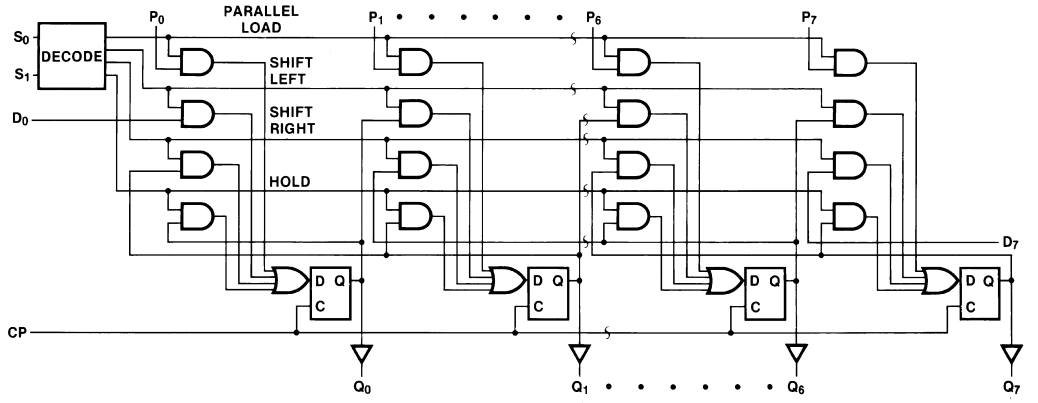
DS100315-2

24-Pin Quad Cerpak



DS100315-3

Logic Diagram



Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	⌐	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	⌐	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	⌐	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = V_{IH} (Max) or V_{IL}(Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = V_{IH} (Min) or V_{IL}(Max)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs		(Notes 3, 4, 5, 6)
V_{IL}	Input LOW Current	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs		(Notes 3, 4, 5, 6)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		(Notes 3, 4, 5, 6)
I_{IH}	Input High Current		240	µA	0˚C to +125˚C	V_{EE} = −5.7V		(Notes 3, 4, 5)
			340	µA	−55˚C	V_{IN} = V_{IH} (Max)		
I_{EE}	Power Supply Current					Inputs Open		(Notes 3, 4, 5)
		−168	−55	mA	−55˚C to +125˚C	V_{EE} = −4.2V to −4.8V		
		−178	−55	mA		V_{EE} = −4.2V to −5.7V		

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at −55˚C, +25˚C and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{max}	Max Clock Frequency	400		400		300		MHz	*Figures 2, 3*	4
t_{PLH}	Propagation Delay	0.50	2.50	0.50	2.30	0.50	2.80	ns		(Notes 7, 8, 9, 11)
t_{PHL}	CP to Output								*Figures 1, 3*	
t_{TLH}	Transition Time	0.30	1.30	0.30	1.30	0.30	1.30	ns		
t_{THL}	20% to 80%, 80% to 20%									

AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_s	Setup Time									
	D_n, P_n	0.60		0.60		0.60		ns		
	S_n	1.70		1.60		2.40			*Figure 4*	(Note 10)
t_h	Hold Time									
	D_n, P_n	0.90		0.90		0.90		ns		
	S_n	0.50		0.50		0.50				
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*	

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

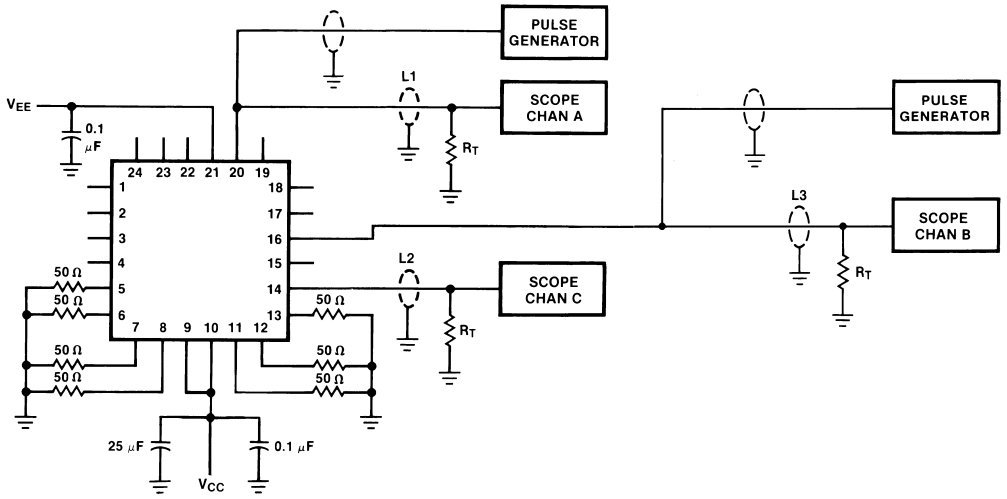
Note 8: Screen tested 100% on each device at +25˚C temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at +25˚C, Subgroup A9, and at +125˚C and −55˚C temperatures, Subgroups A10 and A11.

Note 10: Not tested at +25˚C, +125˚C and −55˚C temperature (design characterization data).

Note 11: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

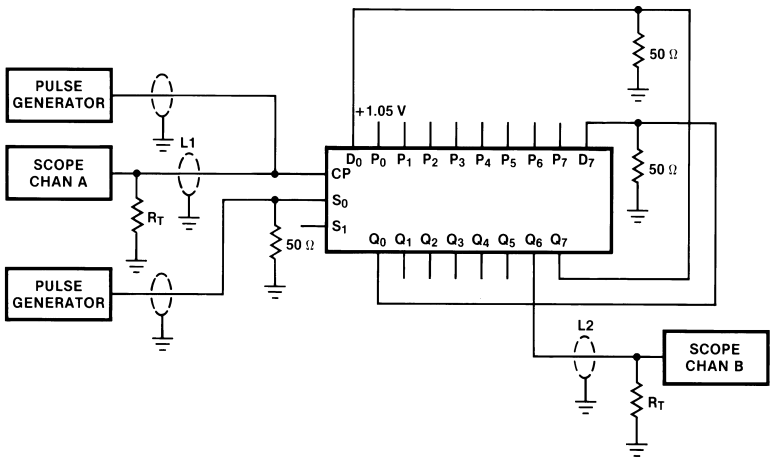
Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for Flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Test Circuitry (Continued)



Notes:
For shift right mode pulse generator connected to S_0 is moved to S_1.
Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms

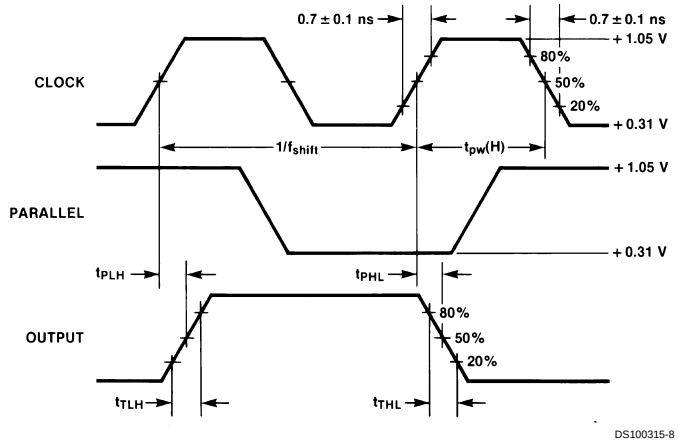
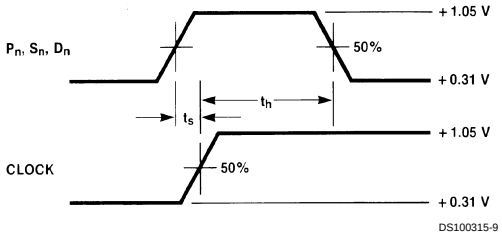


FIGURE 3. Propagation Delay and Transition Times

Switching Waveforms (Continued)

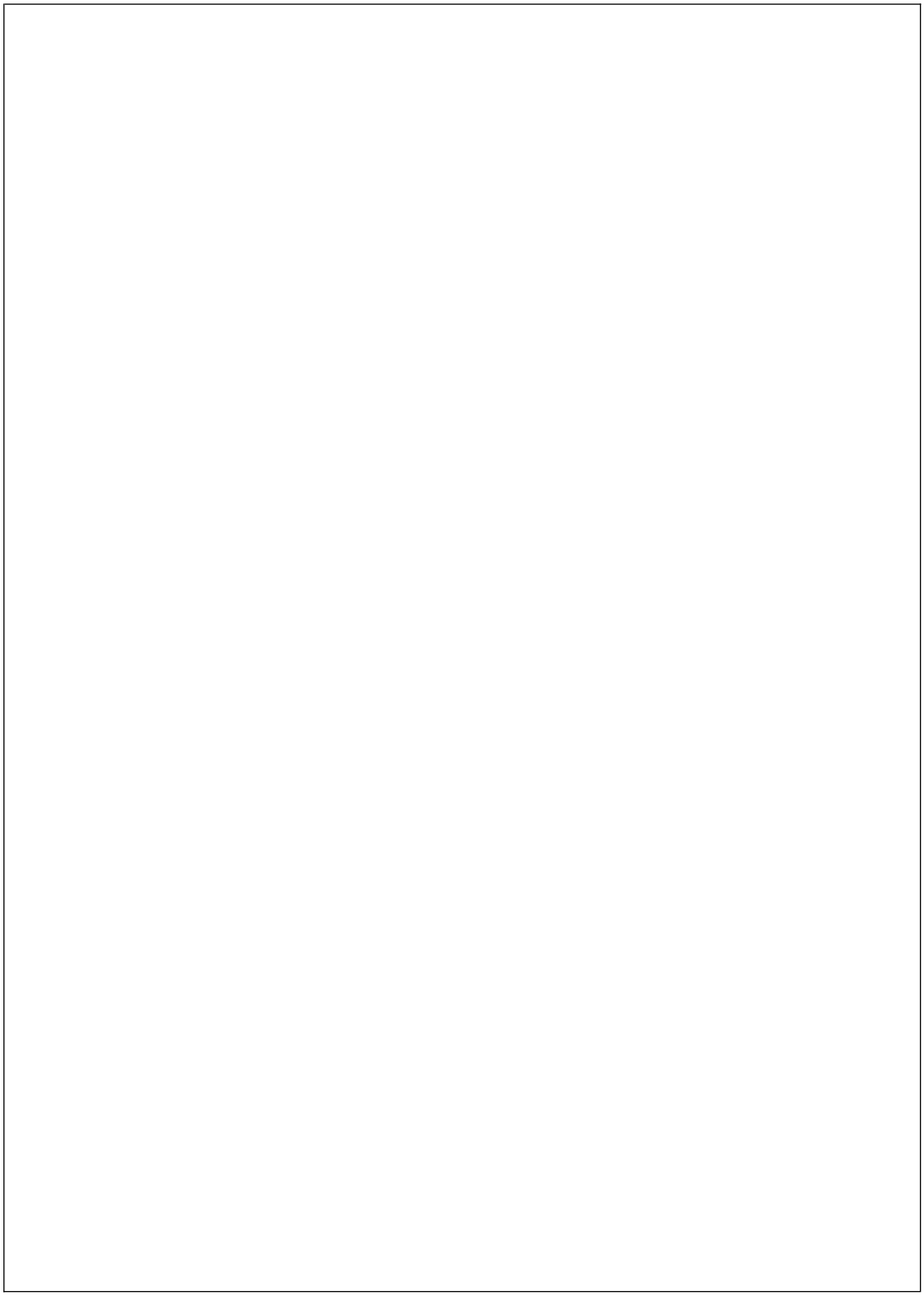


Notes:

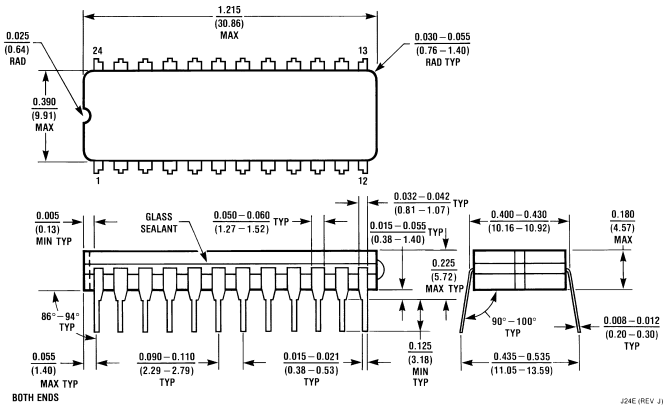
t_S is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

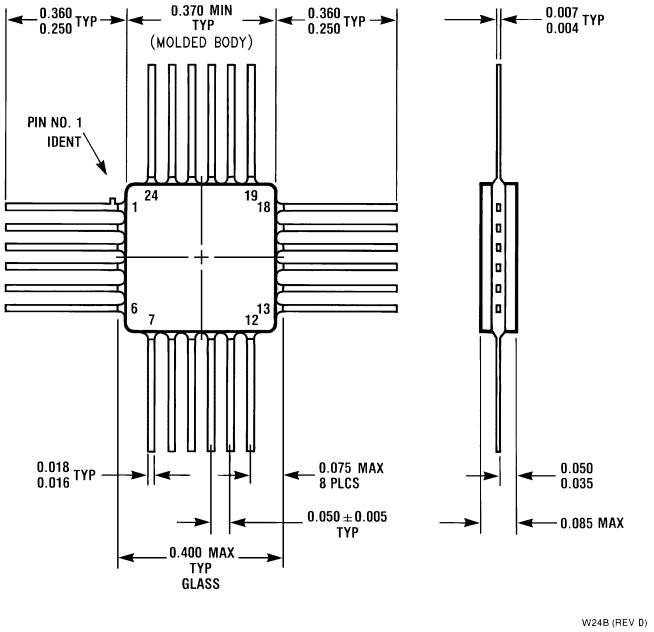
FIGURE 4. Setup and Hold Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

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