MOTOROLA

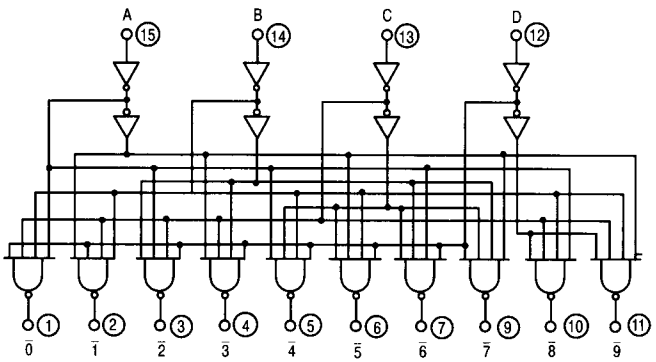
1-of-10 Decoder

ELECTRICALLY TESTED PER:
MIL-M-38510/30703

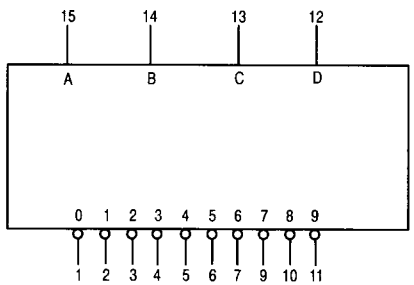
The LSTTL/MSI 54LS42A is a multipurpose decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42A is fabricated with the Schottky barrier diode process for high-speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Demultiplexing Capability
- Mutually Exclusive Outputs
- Input Clamp Diodes Limit High-Speed Termination Effect

LOGIC DIAGRAM



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS42A decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol or diagram. The active LOW outputs facilitate addressing over MSI units with LOW input enables.

The logic design of the LS42A ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input D produces a useful inhibit function when the LS42A is used as a one-of-eight decoder. The D input can also be used as the Data input in an 8-output demultiplexer application.

Military 54LS42A

MPO

AVAILABLE AS:

1) JAN: JM38510/30703BXA
2) SMD: N/A
3) 883: 54LS42A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
0	1	1	2	V_{CC}
1	2	2	3	V_{CC}
2	3	3	4	V_{CC}
3	4	4	5	V_{CC}
4	5	5	7	V_{CC}
5	6	6	8	V_{CC}
6	7	7	9	V_{CC}
GND	8	8	10	GND
7	9	9	12	V_{CC}
8	10	10	13	V_{CC}
9	11	11	14	V_{CC}
D	12	12	15	V_{CC}
C	13	13	17	V_{CC}
B	14	14	18	V_{CC}
A	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

Pin Names		Loading (Note a)	
		HIGH	LOW
A-D 0 to 9	Address Inputs Active Low Outputs (Note b)	0.5 U.L. 10 U.L.	0.25 U.L. 5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 µA HIGH/ 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

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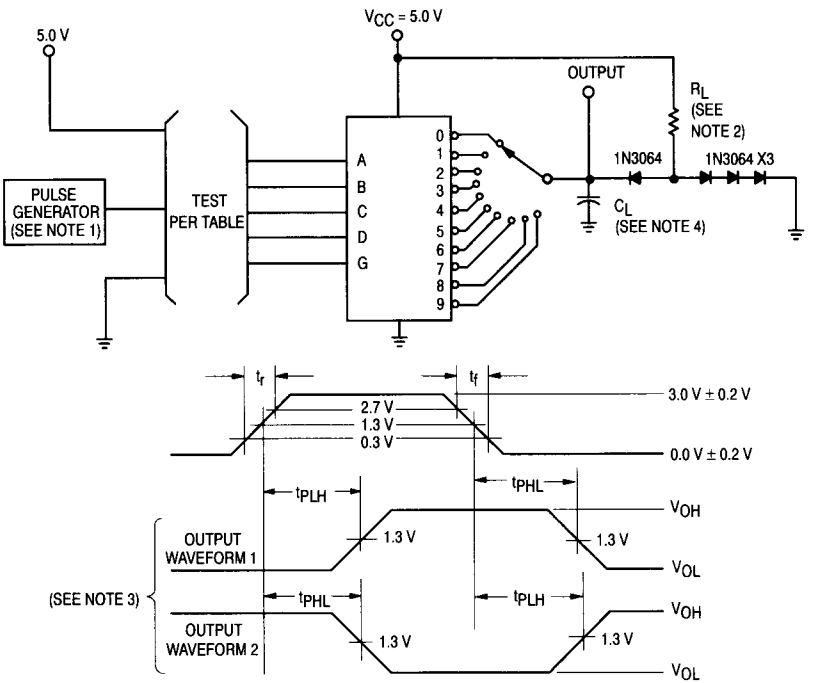
TRUTH TABLE														
Inputs				Outputs										
A	B	C	D	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Levels
L = LOW Voltage Levels

TEST CIRCUIT AND WAVEFORM



NOTES:

1. The input pulse generator has the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, PRR ≤ 1.0 MHz, and minimum duty cycle = 50%.
2. $R_L = 2.0\ k\Omega \pm 10\%$.
3. Input-output waveform combination in accordance with truth table.
4. $C_L = 50$ pF ± 10%, including scope probe, wiring and stray capacitance.
5. Voltage measurements are to be made with respect to network ground terminal.
6. All diodes are 1N3064 or equivalent.
7. The limits specified for $C_L = 15$ pF are guaranteed but not tested.
8. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = – 0.4 mA, V_{IH} = 2.0 V (all inputs).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IN} = 0.7 V or 2.0 V per Truth Table.
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are GND.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 4.5 V.
I_{IL}	Logical "0" Input Current	– 0.12	– 0.36	– 0.12	– 0.36	– 0.12	– 0.36	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), V_{OUT} = GND.
I_{CC}	Power Supply Current Off		13		13		13	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
VIL	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output High-Low	5.0 —	30 25	5.0 —	45 40	5.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Low-High	5.0 —	30 25	5.0 —	45 40	5.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4} t_{PHL4}	Propagation Delay /Data-Output High-Low	5.0 —	35 30	5.0 —	53 48	5.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay /Data-Output Low-High	5.0 —	35 30	5.0 —	53 48	5.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

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