MOTOROLA

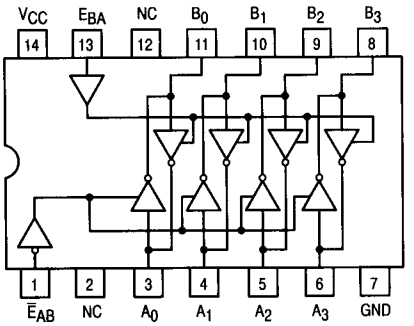
Quad Non-Inverting Bus Transceivers With 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/34801

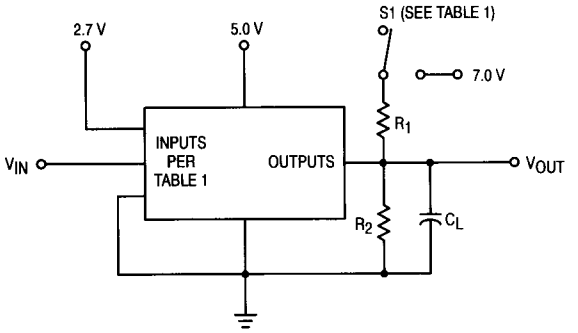
The 54F242 is a Quad Bus Transmitter/Receivers designed for 4-line asynchronous 2-way data communications between data buses.

- 2-Way Asynchronous Data Bus Communication
- Input Clamp Diodes Limit High Speed Termination Effects

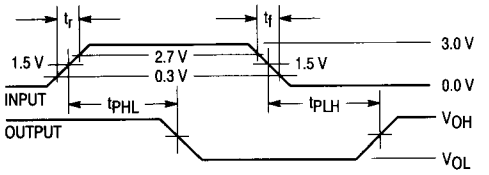
LOGIC DIAGRAM



AC TEST CIRCUIT



PROPAGATION DELAY TIMES



Military 54F242

AVAILABLE AS:

1) JAN: JM38510/34801BXA
2) SMD: N/A
3) 883: 54F242/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}_{AB}$	1	1	2	V_{CC}
NC	2	2	3	V_{CC}
A_0	3	3	4	OPEN
A_1	4	4	6	OPEN
A_2	5	5	8	OPEN
A_3	6	6	9	OPEN
GND	7	7	10	GND
B_3	8	8	12	OPEN
B_2	9	9	13	OPEN
B_1	10	10	14	OPEN
B_0	11	11	16	OPEN
NC	12	12	18	V_{CC}
E_{BA}	13	13	19	V_{CC}
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output	Inputs		Output
$\overline{E}_{AB}$	D		E_{BA}	D	
L	L	H	L	X	(Z)
L	H	L	L	X	(Z)
H	X	(Z)	H	L	H
H	X	(Z)	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

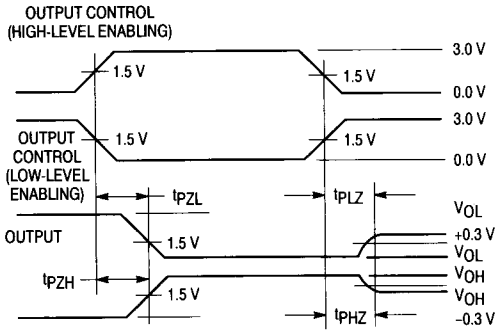


Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IN} = 2.0 V or 0.8 V per Truth Table.
V_{OH1}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = −12 mA, V_{IN} = 2.0 V or 0.8 V per Truth Table.
V_{OL}	Logical "0" Output Voltage		0.55		0.55		0.55	V	V_{CC} = 4.5 V, I_{OL} = 48 mA, V_{IN} = 2.0 V, $E_{AB,\ BA}$ = 2.0 V or 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, $E_{AB,\ BA}$ = 5.5 V or 0 V, other inputs are open.
I_{IH}	Logical 1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V ($E_{AB,\ BA}$), other inputs are open.
I_{IH2}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IN} = 7.0 V ($E_{AB,\ BA}$), other inputs are open.
I_{IH3}	Logical "1" Input Current		1.0		1.0		1.0	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, $E_{AB,\ BA}$ = 0 V or (5.5 V).
I_{IL}	Logical "0" Input Current	−0.03	−1.0	−0.03	−1.0	−0.03	−1.0	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V ($E_{AB,\ BA}$), other inputs are open.
I_{OS}	Output Short Circuit Current	−100	−325	−100	−325	−100	−325	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, other inputs are open, $E_{AB,\ BA}$ = 0 V or 5.5 V, V_{OUT} = 0 V.
I_{IOZH}	Output Off Current High		70		70		70	µA	V_{CC} = 5.5 V, V_{IN} = 2.7 V, other inputs are open, V_{OUT} = 5.5 V, E_{AB} = 2.0 V, E_{BA} = 0.8 V.
I_{IOZL}	Output Off Current Low	−0.06	−1.6	−0.06	−1.6	−0.06	−1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open, V_{OUT} = 0 V, E_{AB} = 2.0 V, E_{BA} = 0.8 V.
I_{CCH}	Power Supply Current		60		60		60	mA	V_{CC} = 5.5 V, V_{IN} = 0 V, $E_{AB,\ BA}$ = 5.5 V or 0 V.
I_{CCL}	Power Supply Current		90		90		90	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, $E_{AB,\ BA}$ = 5.5 V or 0 V.
I_{CCZ}	Power Supply Current Off		90		90		90	mA	V_{CC} = 5.5 V, E_{AB} = 5.5 V, E_{BA} = 0 V, other inputs are open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	− 55°C		
		Subgroup 7	Subgroup 8A	Subgroup 8B		
	Functional Tests					per Truth Table with V_{CC} = 4.5 V, **(Repeat at)**, V_{CC} = 5.5 V, V_{INL} = 0.5 V, V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output B to A	1.5	5.2	1.0	8.5	1.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output B to A	1.5	5.2	1.0	6.5	1.0	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHL2}	Propagation Delay /Data-Output A to B	1.5	5.2	1.0	8.5	1.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLH2}	Propagation Delay /Data-Output A to B	1.5	5.2	1.0	6.5	1.0	6.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLZ1}	Propagation Delay /Data-Output B to A	2.5	6.0	2.0	8.5	2.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHZ1}	Propagation Delay /Data-Output B to A	2.5	6.0	2.0	7.5	2.0	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZL1}	Propagation Delay /Data-Output B to A	2.5	8.5	2.0	10.5	2.0	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZH1}	Propagation Delay /Data-Output B to A	2.5	5.7	2.0	8.0	2.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLZ2}	Propagation Delay /Data-Output A to B	2.5	6.0	2.0	8.5	2.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHZ2}	Propagation Delay /Data-Output A to B	2.5	6.0	2.0	7.5	2.0	7.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZL2}	Propagation Delay /Data-Output A to B	2.5	8.5	2.0	10.5	2.0	10.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZH2}	Propagation Delay /Data-Output A to B	2.5	5.7	2.0	8.0	2.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.

NOTES:
1. V_{IN} pulse has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR = 1.0 MHz.
2. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
3. Voltage measurements are to be made with respect to network ground terminal.
4. $R_1 = R_2$ = 500 Ω ± 5.0%.
5. Terminal condition (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).