

1:9 Differential Clock Driver

The MC10E100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all \bar{Q} outputs HIGH.

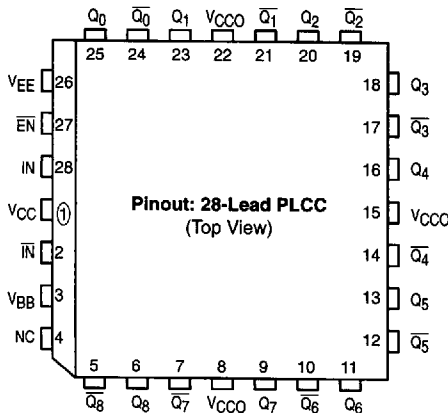
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} Output
- Enable
- Extended 100E V_{EE} Range of -4.2 to $-5.46V$
- 75k Ω Input Pulldown Resistors

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω , even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CC0}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

PIN NAMES

Pin	Function
IN, \bar{IN}	Differential Input Pair
EN	Enable
$Q_0, \bar{Q}_0 - Q_8, \bar{Q}_8$	Differential Outputs
V_{BB}	V_{BB} Output



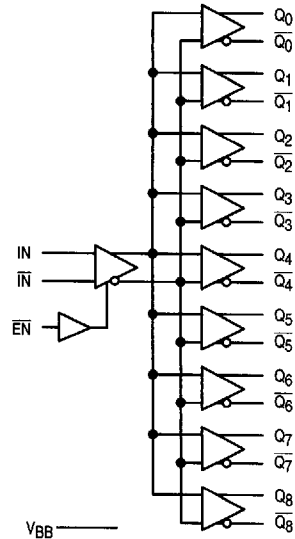
MC10E111
MC100E111

**1:9 DIFFERENTIAL
CLOCK DRIVER**



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

LOGIC SYMBOL



MC10E111 MC100E111

DC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V _{BB}	Output Reference Voltage	10E	-1.43	-1.30	-1.38	-1.27	-1.35	-1.25	-1.31	-1.19				V	
		100E	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26			
I _{IH}	Input HIGH Current			150			150			150			150	μA	
I _{EE}	Power Supply Current	10E	48	60	48	60	48	60	48	60	48	60		mA	
		100E	48	60	48	60	48	60	48	60	55	69			
V _{pp(DC)}	Input Sensitivity	50			50			50			50			mV	1
V _{CMR}	Common Mode Range	-1.6	-0.4		-1.6	-0.4		-1.6	-0.4		-1.6	-0.4		V	2

- Differential input voltage required to obtain a full ECL swing on the outputs.
- V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{pp(min)}.

AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	Cond	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay to Output													ps	1 2 3 3	
	IN (Diff)	380		680	460	560	480		580	510		610				
	IN (SE)	280		780	410	610	430		630	460		660				
	Enable Disable	400 400		900 900	450 450	850 850	450 450		850 850	450 450		850 850				
t _s	Setup Time	EN to IN	250	0	200	0	200	0	200	0	200	0		ps	5	
t _H	Hold Time	IN to EN	50	-200	0	-200	0	-200	0	-200	0	-200		ps	6	
t _R	Release Time	EN to IN	350	100	300	100	300	100	300	100	300	100		ps	7	
t _{skew}	Within-Device Skew		25	75	25	50	25	50	25	50	25	50		ps	4	
V _{pp(AC)}	Minimum Input Swing		250		250		250		250		250			mV	8	
t _r , t _f	Rise/Fall Time		250	450	650	275	375	600	275	375	600	275	375	600	ps	

- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1-12) of the Motorola High Performance ECL Data Book (DL140/D).
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1-12) of the Motorola High Performance ECL Data Book (DL140/D).
- Enable is defined as the propagation delay from the 50% point of a **negative** transition on EN to the 50% point of a **positive** transition on Q (or a negative transition on Q̄). Disable is defined as the propagation delay from the 50% point of a **positive** transition on EN to the 50% point of a **negative** transition on Q (or a positive transition on Q̄).
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
- The setup time is the minimum time that EN must be asserted prior to the next transition of IN/IN̄ to prevent an output response greater than ±75 mV to that IN/IN̄ transition (see Figure 1).
- The hold time is the minimum time that EN must remain asserted after a negative going IN or a positive going IN̄ to prevent an output response greater than ±75 mV to that IN/IN̄ transition (see Figure 2).
- The release time is the minimum time that EN must be deasserted prior to the next IN/IN̄ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
- V_{pp(min)} is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{pp(min)} is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.

6367252 0099099 T79

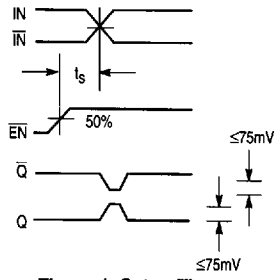


Figure 1. Setup Time

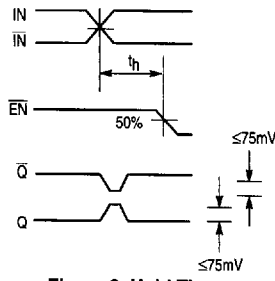


Figure 2. Hold Time

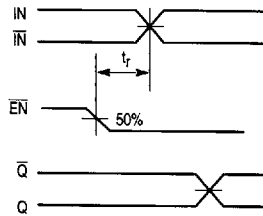


Figure 3. Release Time

6367252 0099100 510