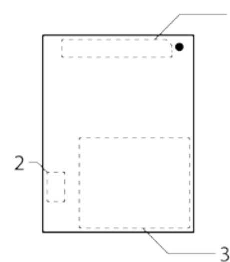
TELEDYNE e2V
HIREL ELECTRONICS
Everywhereyoulook™

TDG650E15BEP
Bottom-side cooled 650 V E-mode GaN FET
Product Specification

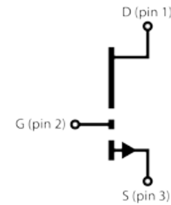
Features

- 650 V Enhancement mode power transistor
- Bottom-side cooled configuration
- RDS(on) = 100 mΩ
- IDS(max) = 15 A
- Ultra-low FOM Island Technology® die
- Low inductance GaNPX® package
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20V/+10V)
- Very high switching frequency (> 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 5.0 x 6.6 mm^2 PCB footprint
- RoHS 6 compliant

Package Outline



Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Solar and Wind Power
- Fast Battery Charging
- dc-dc converters
- On Board Battery Chargers

Description

The TDG650E15BEP is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. Teledyne e2v implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The TDG650E15BEP is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high-power applications. These features combine to provide very high efficiency power switching.

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Table 1 Absolute Maximum Ratings (Tcase = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Drain-to-Source Voltage - transient (note 1)	V_{DS} (transient)	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	V_{GS} (transient)	-20 to +10	V
Step Stress Gate-to-Source Voltage (Tj=175°C,12h) [4]	$STSV_{gs}$	8	V
Continuous Drain Current (T_{case}= 25 °C) (note 2)	I_{DS}	15	A
Continuous Drain Current (T_{case}= 100 °C) (note 2)	I_{DS}	12.5	A
Pulse Drain Current (Pulse width 50 µs, VGS = 6 V) (Note 2)	I_{DS} Pulse	30	A

(1) Pulse ≤ 1 µs
(2) Limited by saturation
(3) Defined by product design and characterization. Value is not tested to full current in production.
(4) Please contact Teledyne for additional Information regarding Step Stress

Table 2 Thermal Characteristics (Typical values unless otherwise noted.)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$	1.0	°C /W
Thermal Resistance (junction-to-ambient) (note 5)	$R_{\Theta JA}$	28	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(5) Device mounted on 1.6 mm thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal via under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Table 3 Ordering Information

Ordering code	Package type	Packing method	Qty	Part Marking	Origin	ECCN
TDG650E15BEP	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	TDG615BE	US	EAR99
TDG650E15BEPF	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	TDG615BF	EU	EU

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Table 4 Electrical Characteristics

Typical values at TJ = 25 °C, VGS = 6 V. Unless otherwise noted, Min/Max values are specified over the full temperature range from TJ = -55 °C to TJ = 150 °C based on Teledyne Dynamic Burn-In after 15 k cycles.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0V, I_{DSS}=25µA
Drain-to-Source On Resistance	$R_{DS(on)}$		100	130	mΩ	V_{GS}=6V,TJ=25°C, I_{DS}=4.5A
Drain-to-Source On Resistance	$R_{DS(on)}$			180	mΩ	Based on Life Testing at Max Conditions, Reading @ Tj=25°C
Drain-to-Source On Resistance	$R_{DS(on)}$		258		mΩ	V_{GS}=6V TJ=150°C, I_{DS}=4.5A
Dynamic Drain-to-Source On Resistance Shift	$DR_{DS(ON)}$		15	30	%	V_{GS}=6V I_{DS}=4.5A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS}=V_{GS} I_{DS}=3.5 mA
Gate-to-Source Current	I_{GS}		80		µA	V_{GS}=6V,V_{DS}=0V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS}=400V, I_{DS}=15A
Drain-to-Source Leakage Current	I_{DSS}		1	25	µA	V_{DS}=650V, V_{GS}= 0V T_J= 25 °C
Drain-to-Source Leakage Current	I_{DSS}		200		µA	V_{DS}=650V, V_{GS}=0V T_J= 150 °C
Internal Gate Resistance	R_G		1.4		Ω	f=1 MHz,open drain
Input Capacitance	C_{ISS}		120		pF	V_{DS}=400V, V_{GS}=0V f=1 MHz
Output Capacitance	C_{OSS}		31		pF	
Reverse Transfer Capacitance	C_{RSS}		1.1		pF	
Effective Output Capacitance, Energy Related (Note 6)	$C_{O(ER)}$		47		pF	V_{GS}=0V V_{DS}=0 to 400V
Effective Output Capacitance, Time Related (Note 7)	$C_{O(TR)}$		75		pF	
Total Gate Charge	Q_G		3.3		nC	V_{GS}=0 to 6V V_{DS}=400V
Gate-to-Source Charge	Q_{GS}		0.9		nC	
Gate-to-Drain Charge	Q_{GD}		1.4		nC	
Output Charge	Q_{OSS}		30		nC	V_{GS}=0V V_{DS}=400V
Reverse Recovery Charge	Q_{RR}		0		nC	

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Table 4 Electrical Characteristics (continued)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Capacitance Stored Energy	E_{OSS}		3.8		µJ	V_{DS} = 400 V, V_{GS} = 0 V_f = 100 kHz

(6) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while VDS is rising from 0 V to the stated V_{DS}.

(7) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while VDS is rising from 0 V to the stated V_{DS}.

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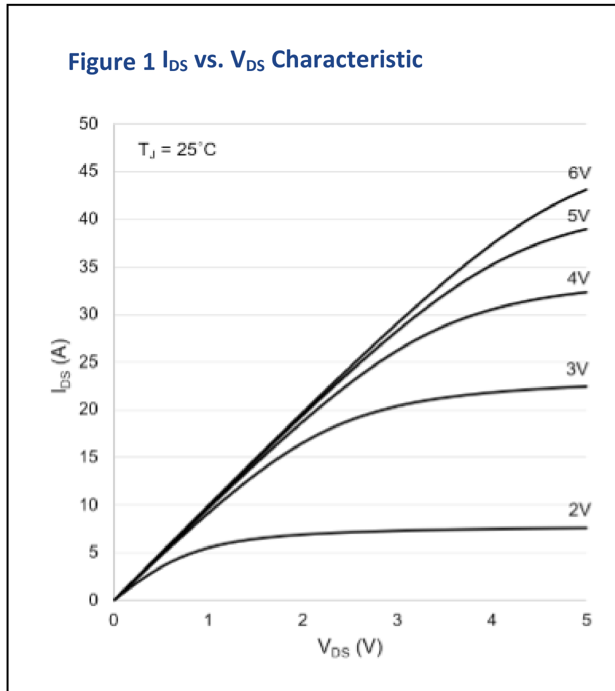
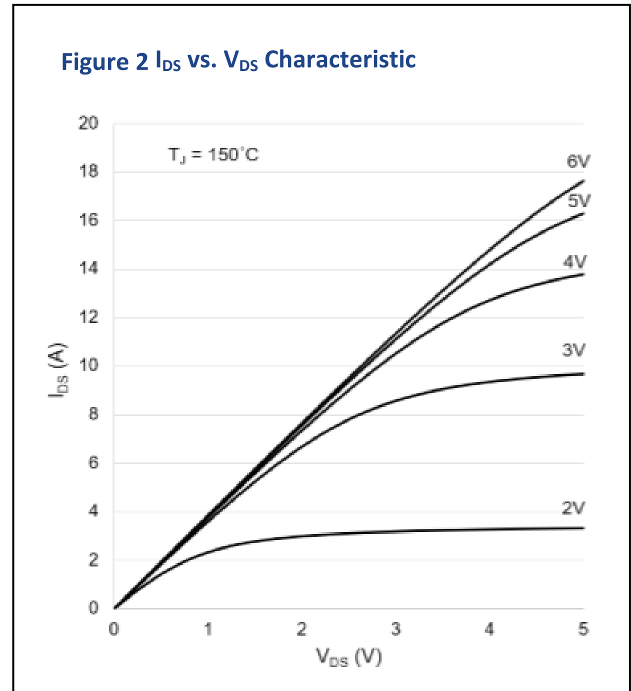
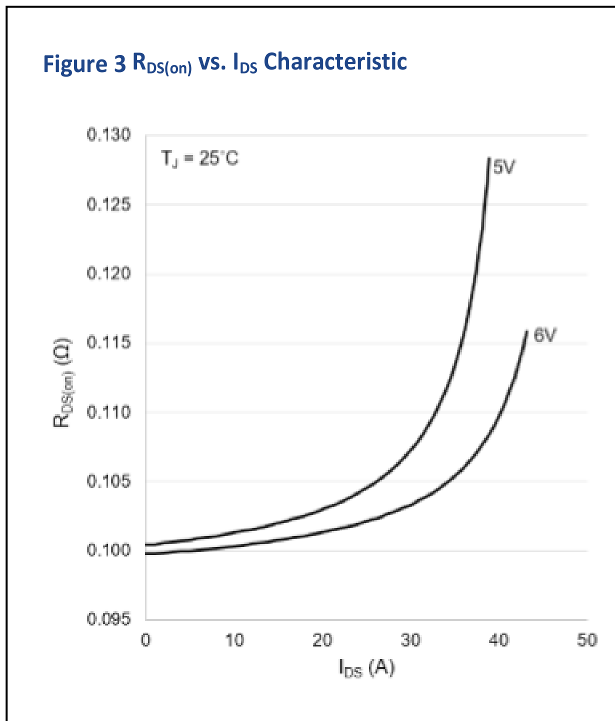
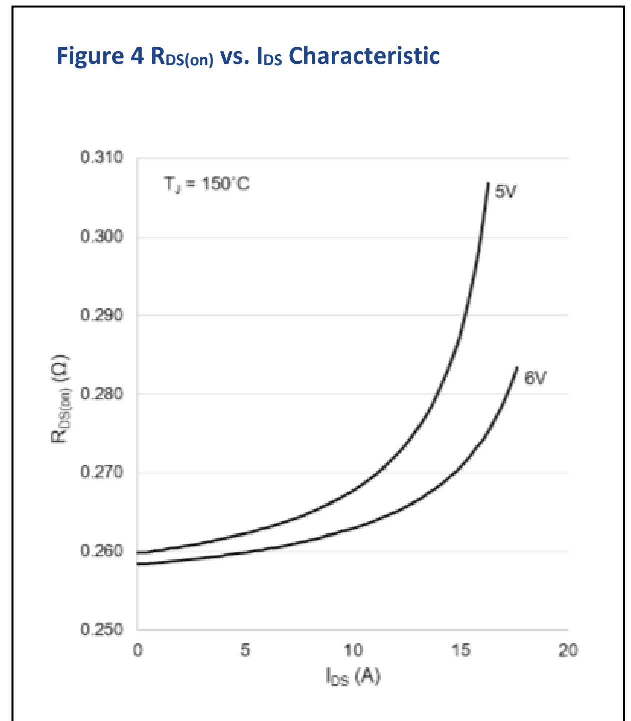
Electrical Performance Graphs









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Electrical Performance Graphs (continued)

Figure 5 I_{DS} vs. V_{DS} , T_J dependence

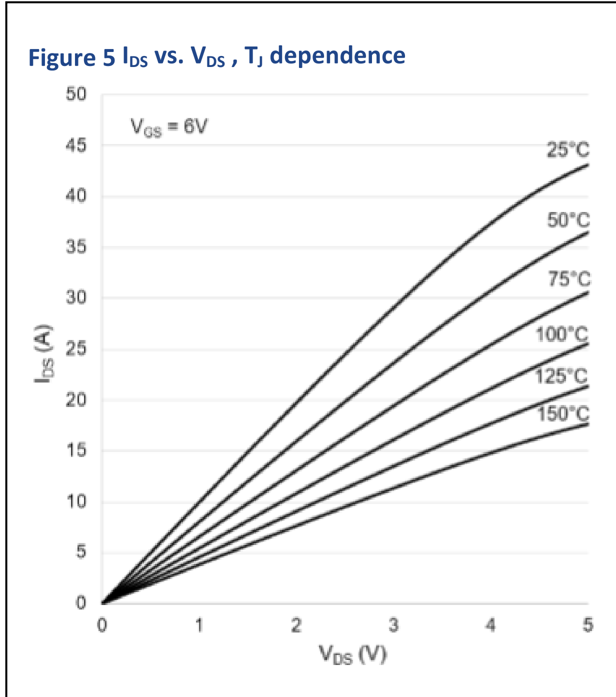


Figure 6 Gate Charge, Q_G Characteristic

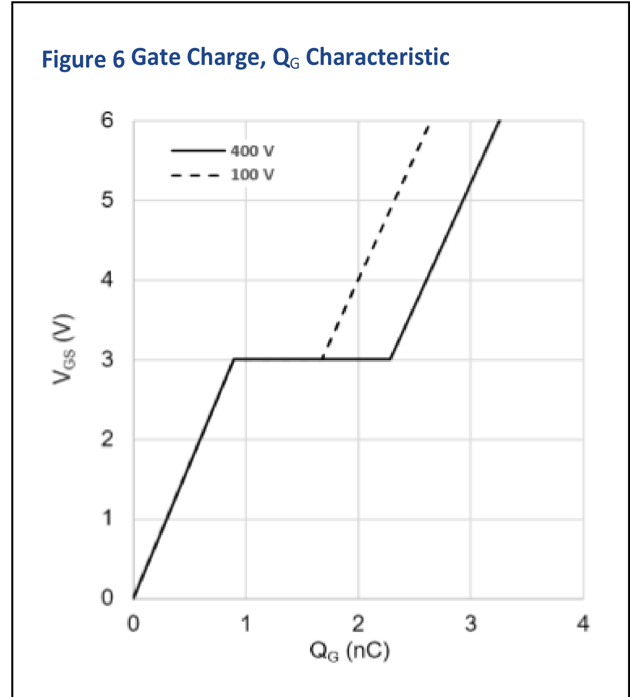


Figure 7 Capacitance Characteristics

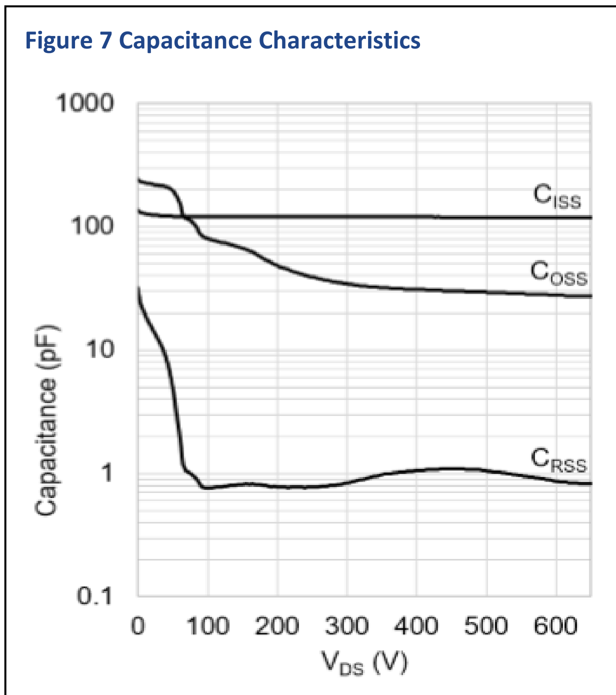
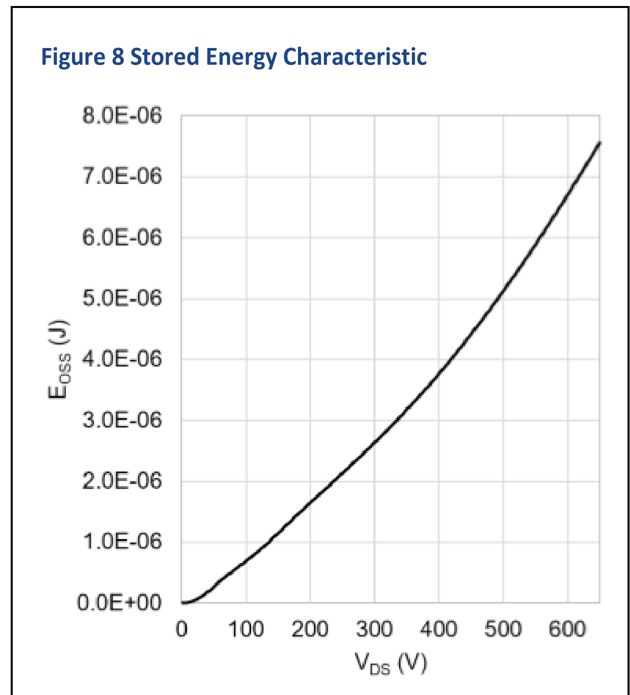


Figure 8 Stored Energy Characteristic



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Electrical Performance Graphs (continued)

Figure 9 Reverse Conduction

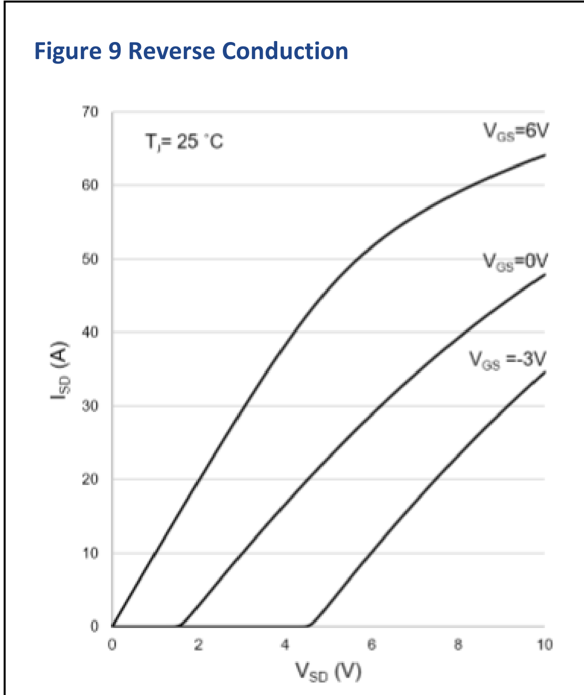


Figure 10 Reverse Conduction

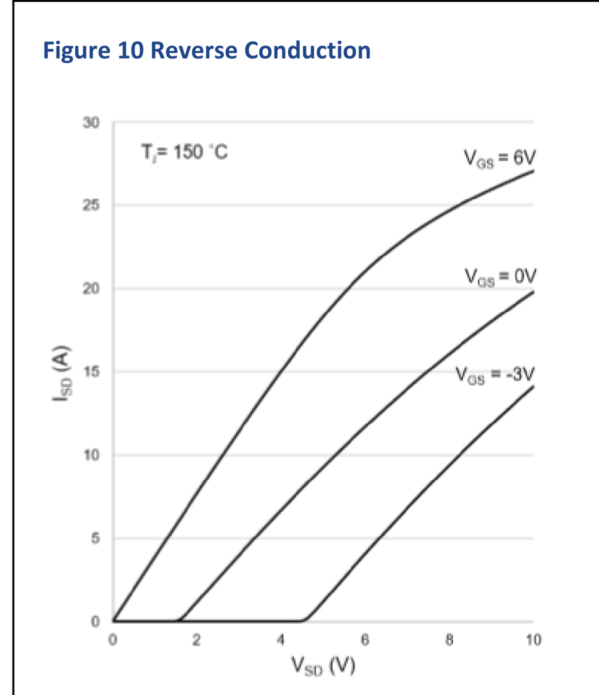


Figure 11 I_{DS} vs. V_{GS} Characteristic

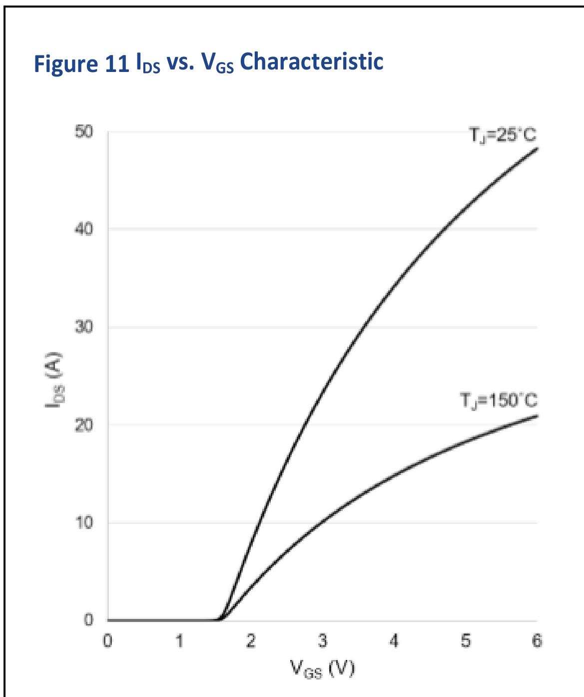
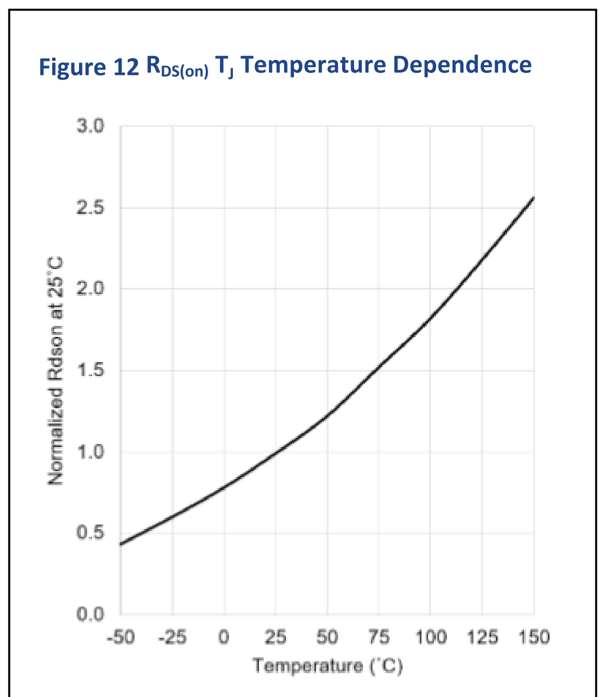


Figure 12 $R_{DS(on)}$ T_J Temperature Dependence



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Thermal Performance Graphs

Figure 13 I_{DS} - V_{DS} Safe Operating Area (T_{case} = 25°C)

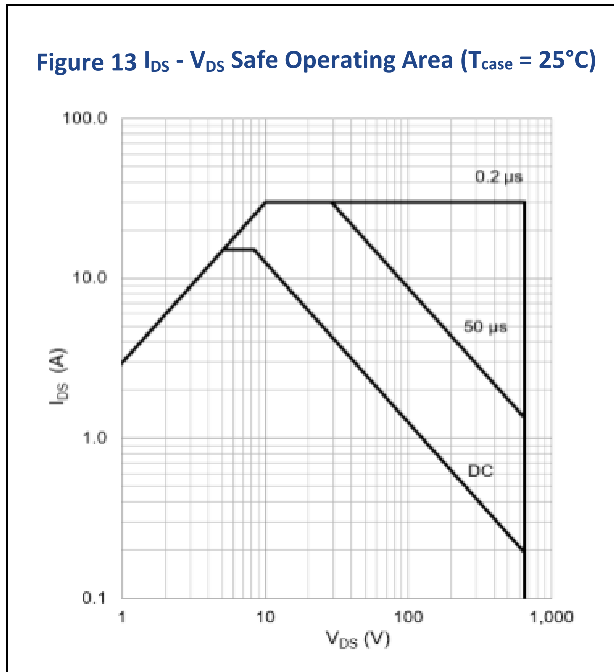


Figure 14 I_{DS} - V_{DS} Safe Operating Area (T_{case}=125°C)

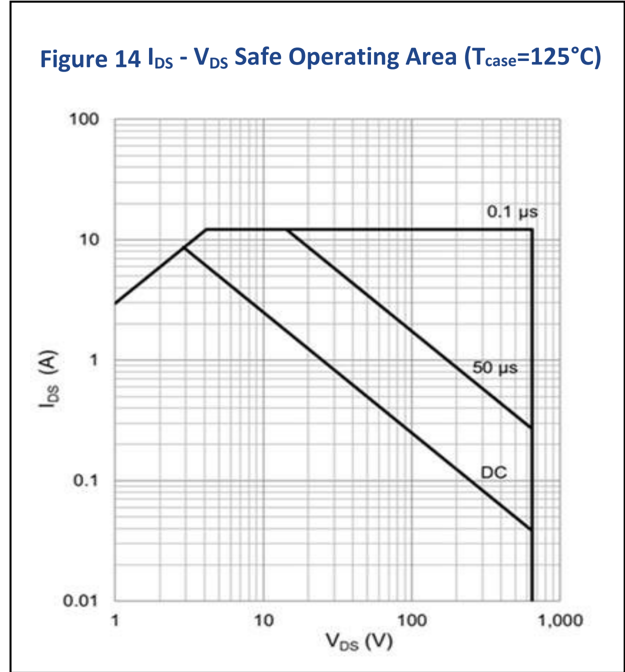


Figure 15 Power Dissipation – Temperature Derating

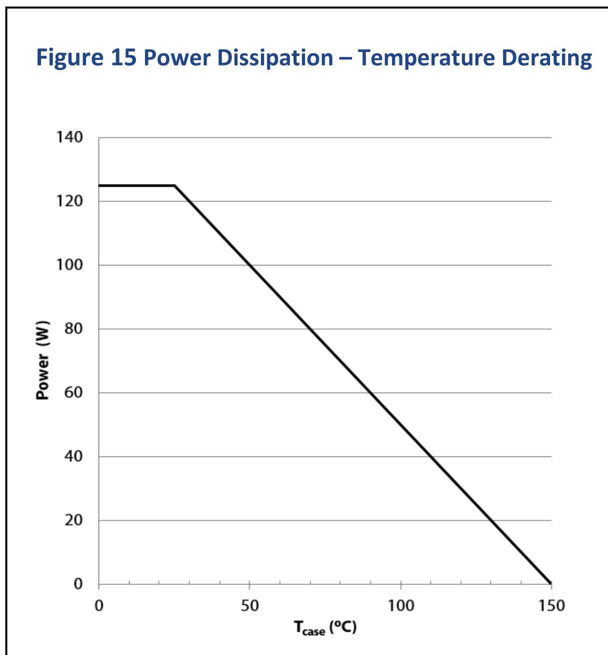
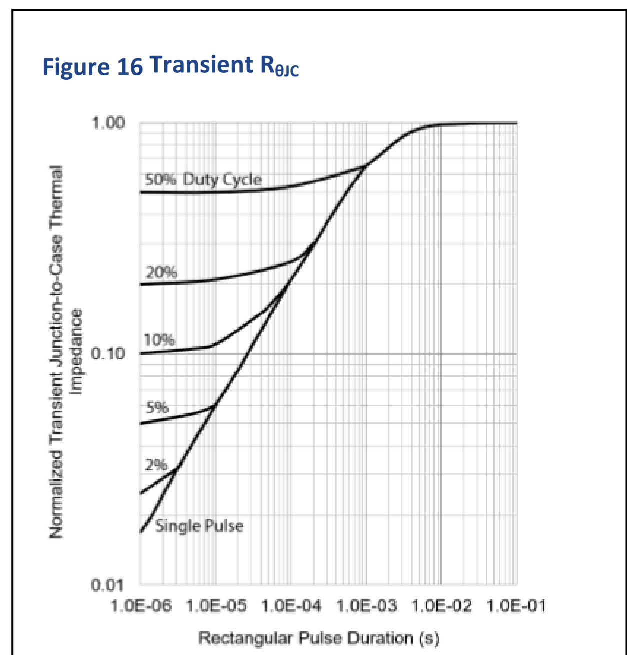


Figure 16 Transient $R_{\theta JC}$



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Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT does not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate; however it increases the reverse conduction loss. For more details, please refer to the gate driver application note GN001, Application Guide – Design with GaN Enhancement Mode HEMT" www.gansystems.com

Similar to silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under- voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight enough tolerance on the gate voltage. Therefore, special care should be taken when you select and use half bridge drivers. Please see the gate driver application note, (GN001), for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very high speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate's parasitic oscillation.

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Source Sensing

Although the TDG650E15BEP does not have a dedicated source sense pin, the GaNPX® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance

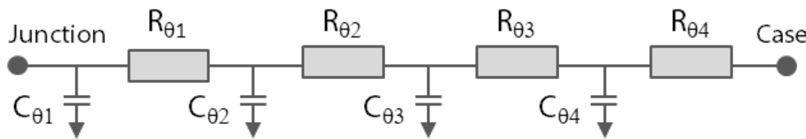
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the TDG650E15BEP. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under the Drain pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

TDG650E15BEP RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.03	$C_{\theta 1}$ = 4.0E-05
$R_{\theta 2}$ = 0.46	$C_{\theta 2}$ = 3.7E-04
$R_{\theta 3}$ = 0.48	$C_{\theta 3}$ = 3.25E-03
$R_{\theta 4}$ = 0.03	$C_{\theta 4}$ = 1E-03

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

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Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (VGS = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and exhibits a channel resistance, RDS(on), similar to forward conduction operation. Off-state condition (VGS ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, VGD, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher VF and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than VGS(th)+VGS(off) in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "VF" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, BVDS, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BVDS. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E- HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the TDG650E60 device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1

(March 2008) The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. Tmin = 150 °C, Tmax = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues. For more details, please refer to the soldering application note "GN011-Soldering-Recommendations- for-GaNPX®-Packaged-Devices" at www.gansystems.com.

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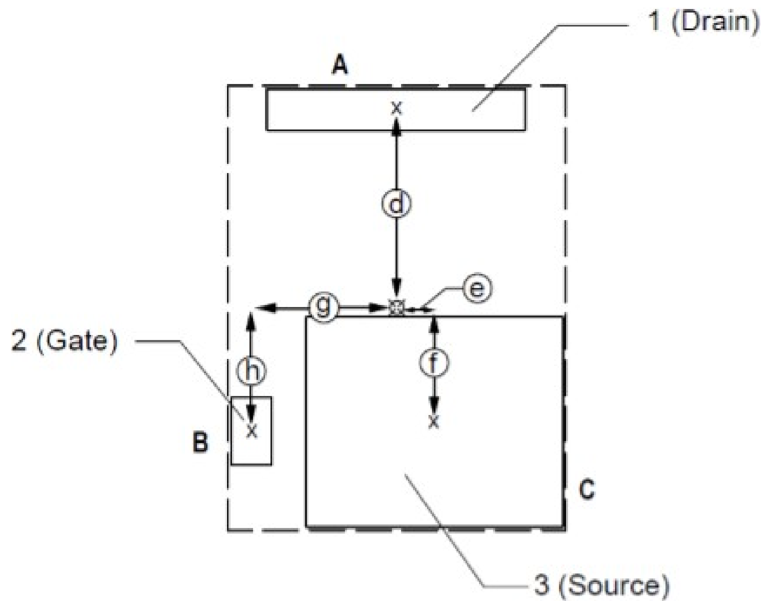
Recommended PCB Footprint for TDG650E15BEP



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.76	0.60	0.148	0.024
B	0.60	1.00	0.024	0.039
C	3.76	3.07	0.148	0.121

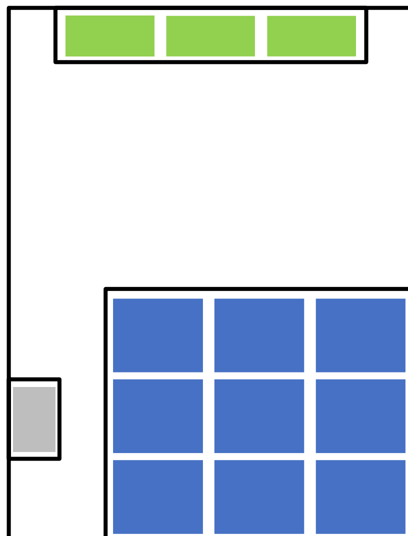
Dimensions

	mm	Inches
d	2.91	0.115
e	0.55	0.022
f	1.67	0.066
g	2.13	0.084
h	1.81	0.071

PCB pad openings

Package outline

Recommended Solder Stencil for Bottom-side Cooled PCB Footprint



Dimension of the Stencil Aperture

1.05 x 0.5 mm

0.5 x 0.84 mm

0.9 x 1.0 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

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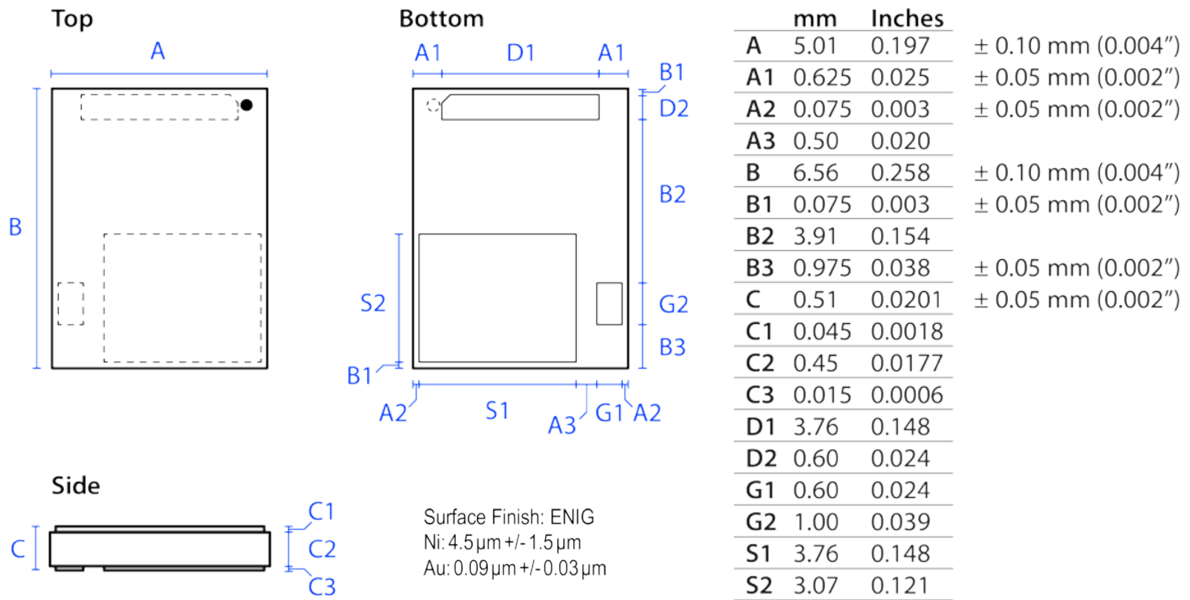
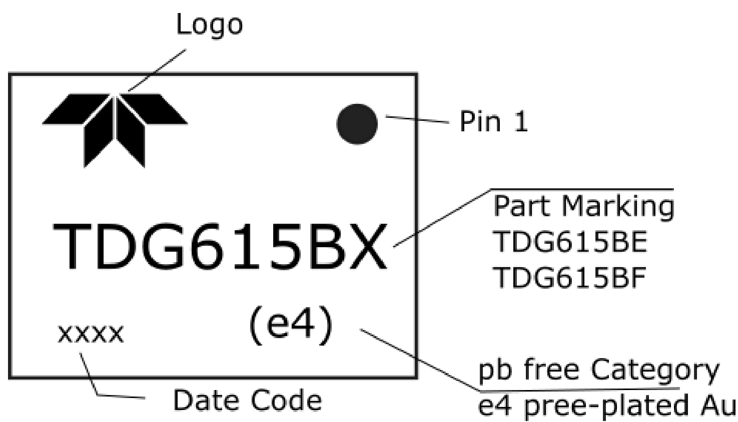
Package Dimensions



	mm	Inches	
A	5.01	0.197	± 0.10 mm (0.004″)
A1	0.625	0.025	± 0.05 mm (0.002″)
A2	0.075	0.003	± 0.05 mm (0.002″)
A3	0.50	0.020	
B	6.56	0.258	± 0.10 mm (0.004″)
B1	0.075	0.003	± 0.05 mm (0.002″)
B2	3.91	0.154	
B3	0.975	0.038	± 0.05 mm (0.002″)
C	0.51	0.0201	± 0.05 mm (0.002″)
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	3.76	0.148	
D2	0.60	0.024	
G1	0.60	0.024	
G2	1.00	0.039	
S1	3.76	0.148	
S2	3.07	0.121	

Note: Inch measurements are approximate values

GaNPX® Part Marking



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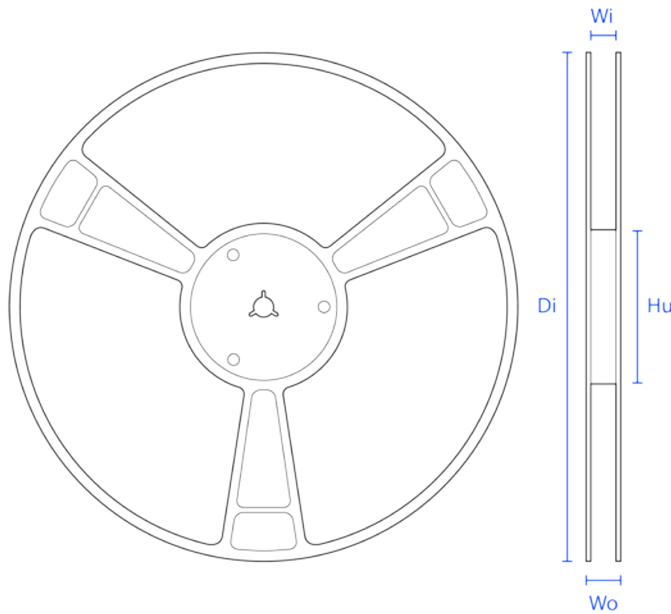
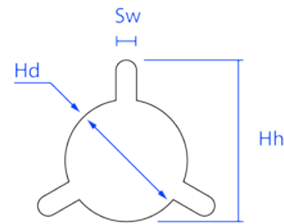
TDG650E15BEGaNPX® Tape and Reel Information

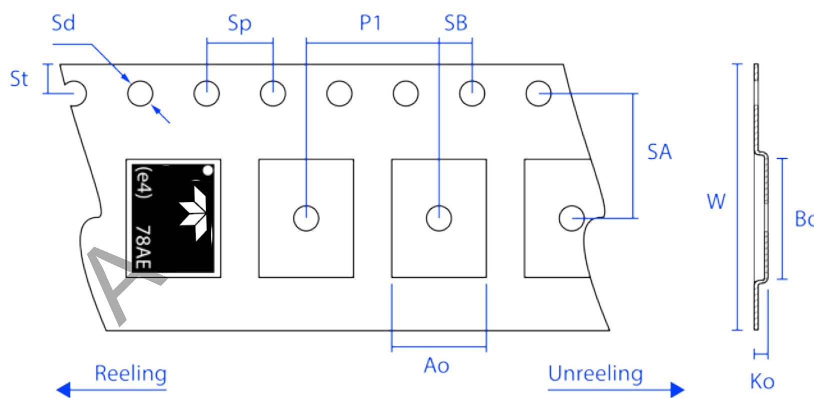


Dimensions (mm)

	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	180.0	+1.5 / - 2.0
Wo	22.4	MAX	22.4	MAX
Wi	16.4	+ 2.0 / - 0.0	16.4	+ 2.0 / - 0.1
Hu	100.0	+/- 1.5	60.0	+ 2.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.8
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.1	+/- 0.3



Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	8.00	+/- 0.1
W	16.00	+ 0.3 / - 0.1
Ko	0.70	+/- 0.1
Ao	5.70	+/- 0.1
Bo	7.10	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	7.50	+/- 0.1
SB	2.00	+/- 0.1

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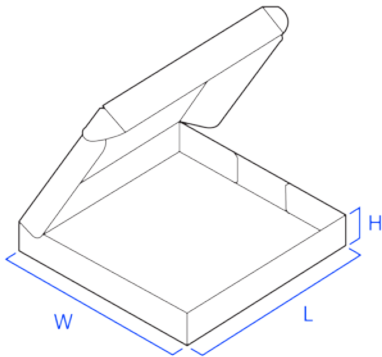
Tape and Reel Box Dimensions



Outside dimensions (mm)

	7″ mini-reel	13″ tape-reel
W	197	342
L	204	355
H	32	53

Document Categories:

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, Email us at: **tdemarketing@teledyne.com ~ www.tdehirel.com**

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