

Features

- Fast Read Access Time – 90 ns
- Automatic Page Write Operation
 - Internal Address and Data Latches for 64 Bytes
 - Internal Control Timer
- Fast Write Cycle Times
 - Page Write Cycle Time: 3 ms Maximum
 - 1 to 64-byte Page Write Operation
- Low Power Dissipation: 300 μ A Standby Current (CMOS)
- Hardware and Software Data Protection
- DATA Polling for End of Write Detection
- High Reliability CMOS Technology
 - Endurance: 10^5 Cycles
 - Data Retention: 10 Years
- Single 5V \pm 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout

Description

The AT28HC256N is a high-performance electrically erasable and programmable read only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256N offers access times to 90 ns with power dissipation of just 440 mW. When the AT28HC256N is deselected, the standby current is less than 3 mA.

The AT28HC256N is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA Polling of I/O₇. Once the end of a write cycle has been detected a new access for a read or write can begin.

Atmel's AT28HC256N has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

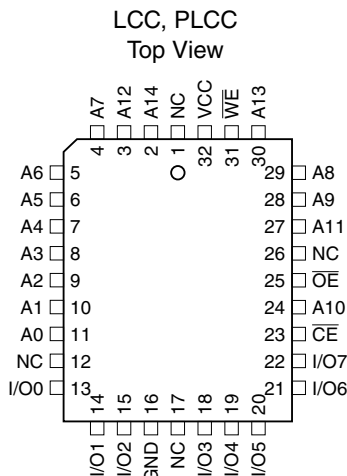


256 (32K x 8) High-speed Parallel EEPROM

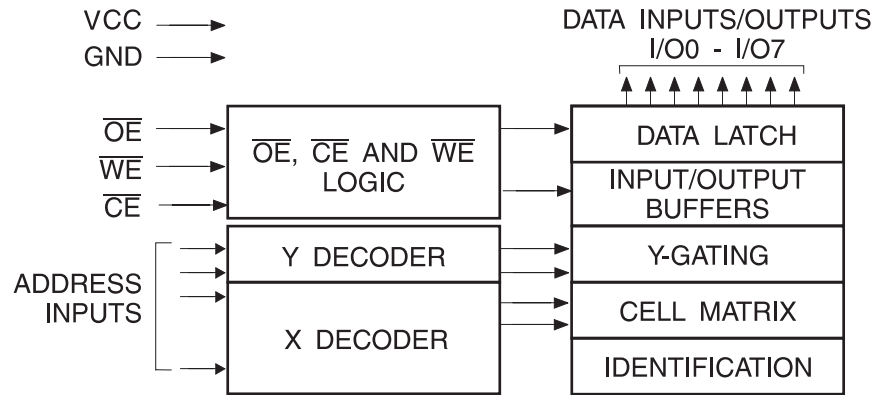
AT28HC256N

Pin Configurations

| Pin Name | Function |
|------------------------|---------------------|
| A0 - A14 | Addresses |
| $\overline{\text{CE}}$ | Chip Enable |
| $\overline{\text{OE}}$ | Output Enable |
| $\overline{\text{WE}}$ | Write Enable |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |



Block Diagram



Absolute Maximum Ratings*

| | |
|---|--------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CC} + 0.6V$ |
| Voltage on \overline{OE} and A9 with Respect to Ground | -0.6V to +13.5V |

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28HC256N is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE: A low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high initiates a write cycle. The address is latched on the falling edge of \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28HC256N allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within $150 \mu s$ (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28HC256N will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. That is, for each \overline{WE} high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28HC256N features \overline{DATA} Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O₇. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. \overline{DATA} Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to \overline{DATA} Polling the AT28HC256N provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O₆ toggling between one and zero. Once the write has completed, I/O₆ will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may occur during transition of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28HC256N in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit – holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28HC256N. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256N is shipped from Atmel with SDP disabled.



SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to “Software Data Protection” algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28HC256N will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28HC256N. This is done by preceding the data to be written by the same 3-byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256N during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC} , read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to $12V \pm 0.5V$ and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software code. Please see “Software Chip Erase” application note for details.

DC and AC Operating Range

| | AT28HC256N-90 | AT28HC256N-12 |
|---|---------------|---------------|
| Operating Industrial Temperature (Case) | -40°C - 85°C | -40°C - 85°C |
| V _{CC} Power Supply | 5V ±10% | 5V ±10% |

Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O |
|-----------------------|-----------------|-------------------------------|-----------------|------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} |
| Write ⁽²⁾ | V _{IL} | V _{IH} | V _{IL} | D _{IN} |
| Standby/Write Inhibit | V _{IH} | X ⁽¹⁾ | X | High Z |
| Write Inhibit | X | X | V _{IH} | |
| Write Inhibit | X | V _{IL} | X | |
| Output Disable | X | V _{IH} | X | High Z |
| Chip Erase | V _{IL} | V _H ⁽³⁾ | V _{IL} | High Z |

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC programming waveforms.
 3. V_H = 12.0V ±0.5V.

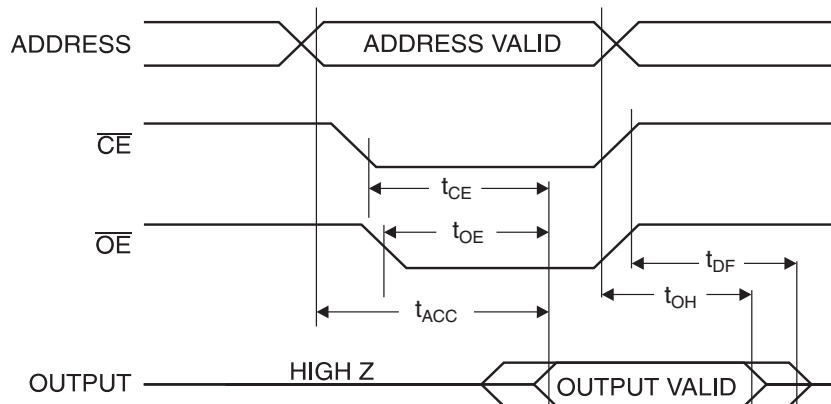
DC Characteristics

| Symbol | Parameter | Condition | Min | Max | Units |
|------------------|--------------------------------------|--|-----|------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} + 1V | | 10 | μA |
| I _{LO} | Output Leakage Current | V _{I/O} = 0V to V _{CC} | | 10 | μA |
| I _{SB1} | V _{CC} Standby Current TTL | $\overline{CE} = 2.0V$ to V _{CC} | | 3 | mA |
| I _{SB2} | V _{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V _{CC} | | 300 | μA |
| I _{CC} | V _{CC} Active Current | f = 5 MHz; I _{OUT} = 0 mA | | 30 | mA |
| V _{IL} | Input Low Voltage | | | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 6.0 mA | | 0.45 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4 mA | 2.4 | | V |

AC Read Characteristics

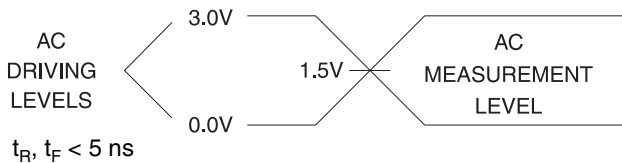
| Symbol | Parameter | AT28C256N-90 | | AT28HC256N-12 | | Units |
|-------------------|---|--------------|-----|---------------|-----|-------|
| | | Min | Max | Min | Max | |
| t_{ACC} | Address to Output Delay | | 90 | | 120 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 90 | | 120 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 40 | 0 | 50 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 40 | 0 | 50 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | 0 | | ns |

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

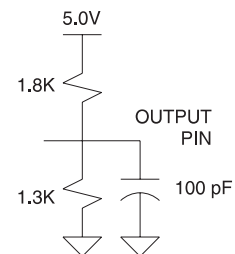


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5 \text{ pF}$).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}^{(1)}$

| Symbol | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|-----------------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0\text{V}$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0\text{V}$ |

- Note: 1. This parameter is characterized and is not 100% tested.

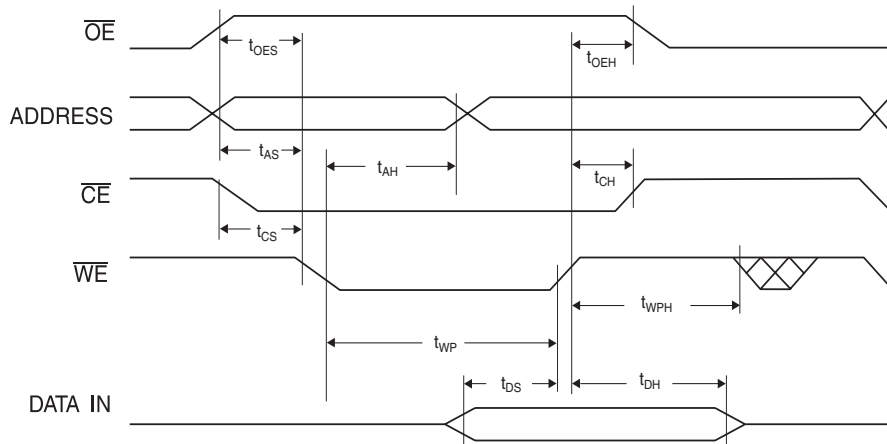
AC Write Characteristics

| Symbol | Parameter | Min | Max | Units |
|-------------------|--|-------------------|-----|-------|
| t_{AS}, t_{OES} | Address, \overline{OE} Setup Time | 0 | | ns |
| t_{AH} | Address Hold Time | 50 | | ns |
| t_{CS} | Chip Select Setup Time | 0 | | ns |
| t_{CH} | Chip Select Hold Time | 0 | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 100 | | ns |
| t_{DS} | Data Setup Time | 50 | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 0 | | ns |
| t_{DV} | Time to Data Valid | NR ⁽¹⁾ | | |

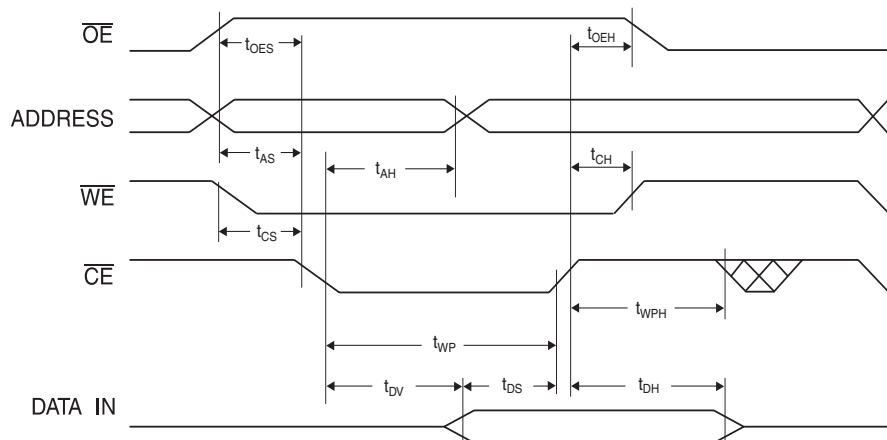
Notes: 1. NR = No Restriction.

AC Write Waveforms

\overline{WE} Controlled



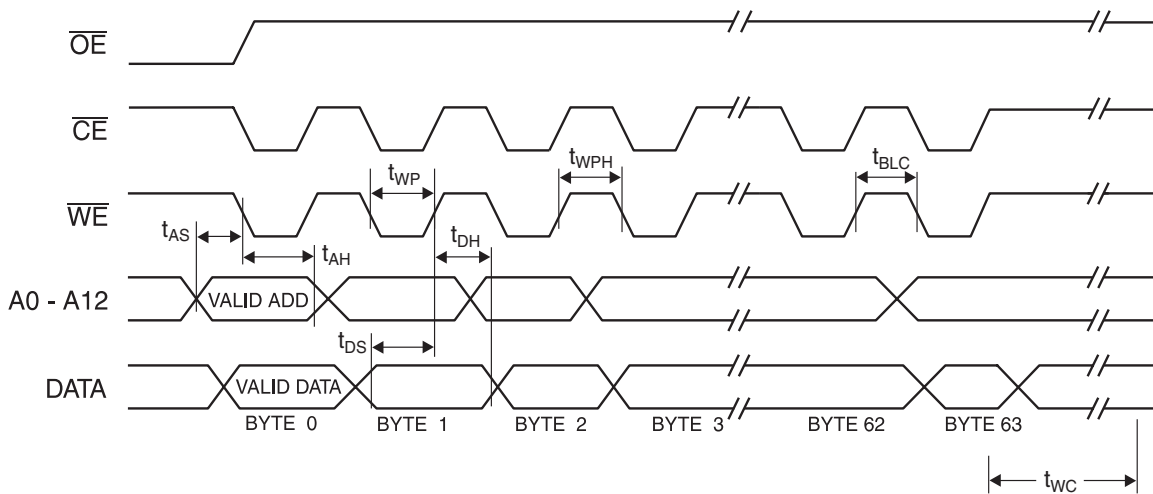
\overline{CE} Controlled



Page Mode Write Characteristics

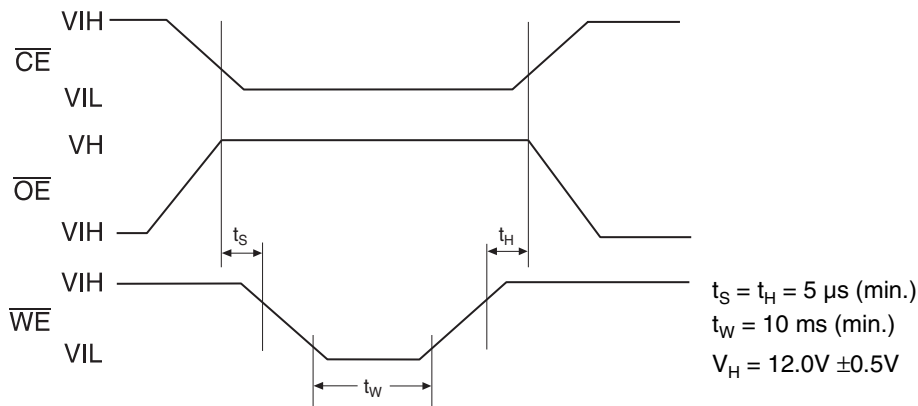
| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|---------|
| t_{WC} | Write Cycle Time | | | 3 | ms |
| t_{AS} | Address Setup Time | 0 | | | ns |
| t_{AH} | Address Hold Time | 50 | | | ns |
| t_{DS} | Data Setup Time | 50 | | | ns |
| t_{DH} | Data Hold Time | 0 | | | ns |
| t_{WP} | Write Pulse Width | 100 | | | ns |
| t_{BLC} | Byte Load Cycle Time | | | 150 | μ s |
| t_{WPH} | Write Pulse Width High | 50 | | | ns |

Page Mode Write Waveforms⁽¹⁾⁽²⁾

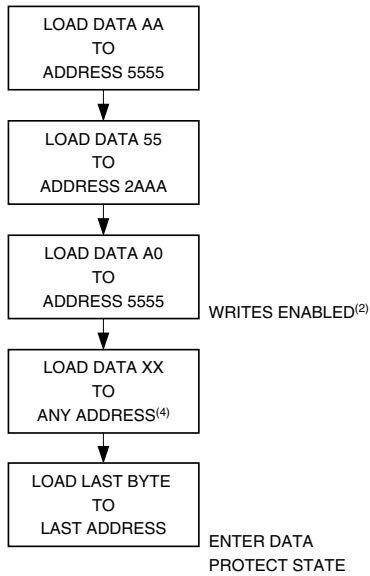


- Notes:
1. A6 through A14 must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}).
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

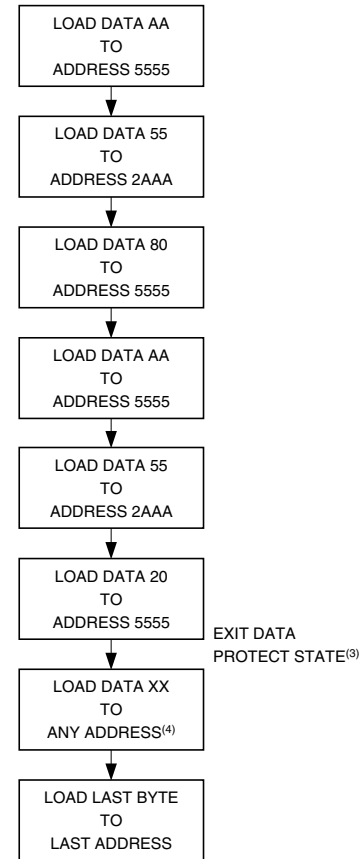
Chip Erase Waveforms



Software Data Protection Enable Algorithm⁽¹⁾

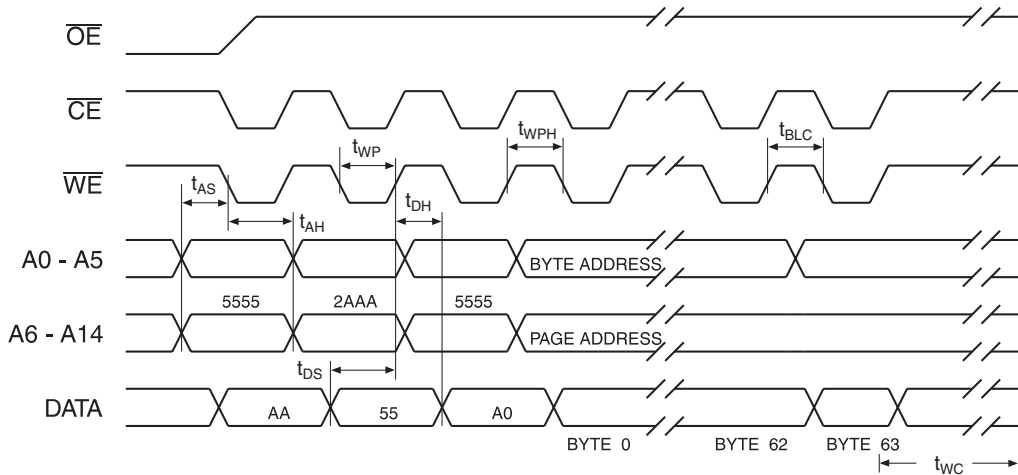


Software Data Protection Disable Algorithm⁽¹⁾



- Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex).
 2. Write Protect state will be activated at end of write even if no other data is loaded.
 3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
 4. 1 to 64 bytes of data are loaded.

Software Protected Write Cycle Waveforms⁽¹⁾⁽²⁾



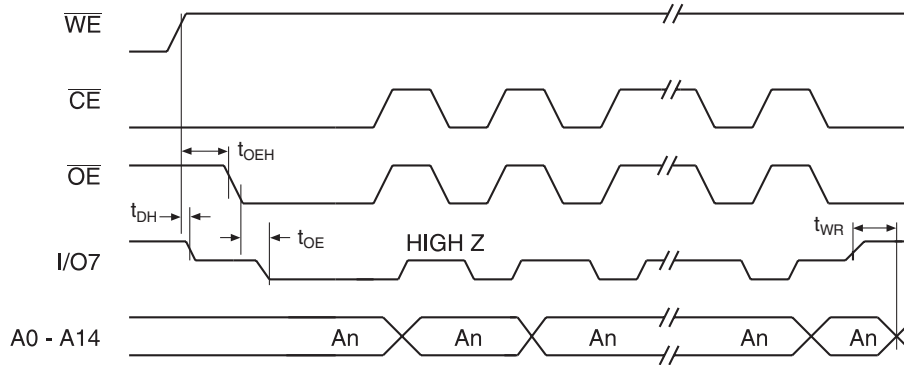
- Notes:
1. A6 through A14 must specify the same page address during each high to low transition of \overline{WE} (or \overline{CE}) after the software code has been entered.
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.

Data Polling Characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 0 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 0 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
2. See "AC Read Characteristics" on page 6.

Data Polling Waveforms

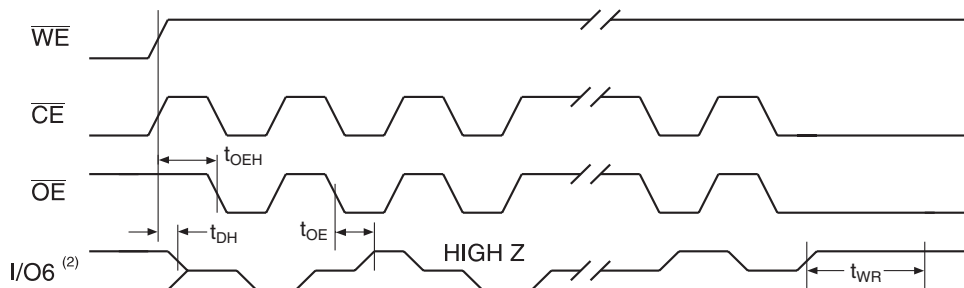


Toggle Bit Characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{OEHP} | \overline{OE} High Pulse | 150 | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
2. See "AC Read Characteristics" on page 6.

Toggle Bit Waveforms



Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information⁽¹⁾

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|-----------------|---------|-------------------------------|
| | Active | Standby | | | |
| 90 | 30 | 0.3 | AT28HC256N-90JI | 32J | Industrial (-40°C to 85°C) |
| 120 | 30 | 0.3 | AT28HC256N-12JI | 32J | Industrial (-40°C to 85°C) |

Note: 1. See "Valid Part Numbers" table below.

| Package Type | |
|--------------|---|
| 32J | 32-lead, Plastic J-leaded Chip Carrier (PLCC) |

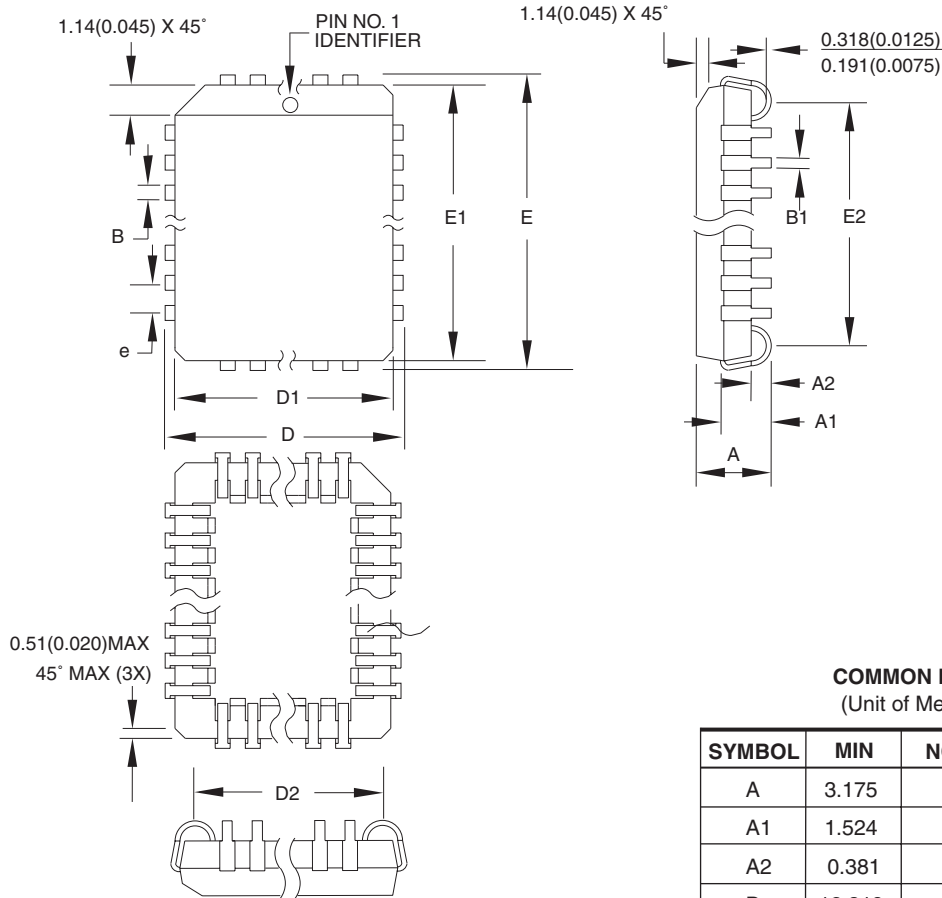
Valid Part Numbers

The following table lists standard Atmel products that can be ordered:

| Device Numbers | Speed | Package and Temperature Combinations |
|----------------|-------|--------------------------------------|
| AT28HC256N | 90 | JI |
| AT28HC256N | 12 | JI |

Packaging Information

32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 3.175 | – | 3.556 | |
| A1 | 1.524 | – | 2.413 | |
| A2 | 0.381 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.354 | – | 11.506 | Note 2 |
| D2 | 9.906 | – | 10.922 | |
| E | 14.859 | – | 15.113 | |
| E1 | 13.894 | – | 14.046 | Note 2 |
| E2 | 12.471 | – | 13.487 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE
32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

| | |
|--------------------|-------------|
| DRAWING NO. | REV. |
| 32J | B |



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests

www.atmel.com/literature

Disclaimer: Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

© Atmel Corporation 2004. All rights reserved. Atmel® and combinations thereof, are the registered trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be the trademarks of others.



Printed on recycled paper.

3446B-PEEPR-4/04