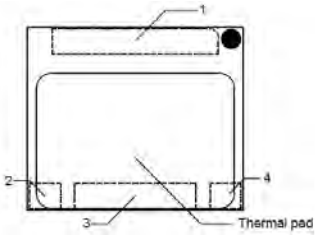
TDG650E60TEP
Top-side cooled 650 V E-mode GaN transistor
Product Specification

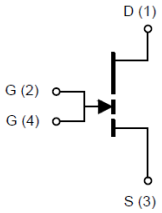
Features

- 650 V enhancement mode power transistor
- Top-side cooled configuration
- RDS(on) = 25 mΩ
- IDS(max) = 60 A
- Ultra-low FOM die
- Low inductance GaNPX® package
- Simple drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 9.0 x 7.6 mm^2 PCB footprint
- Dual gate pads for optimal board layout
- RoHS 3 (6+4) compliant
- HiRel qualification flow
- Obsolescence support

Package Outline



Circuit Symbol



The thermal pad is internally connected to Source (S pin 3) and substrate

Applications

- High efficiency power conversion
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- dc-dc Converters
- On Board Battery Chargers
- E-Switch

Description

The TDG650E60TEP is an enhancement mode GaN-on-silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** and **GaN*PX*®** packaging**. Island Technology®** cell layout realizes high-current die and high yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The TDG650E60TEP is a top-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	T_{DS}	650	V
Transient Drain-to-Source Voltage [1]	V_{DS}(transient)	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Step Stress Gate-to-Source Voltage (T_J = 175 °C 12h) [2]	$STSV_{GS}$	8	V
Gate-to-Source Voltage - transient [1]	V_{GS}(transient)	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C)	I_{DS}	60	A
Continuous Drain Current (T_{case} = 100 °C)	I_{DS}	47	A
Pulse Drain Current [2]	I_{DS} Pulse	120	A

(1) For ≤ 1 µs
(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – top side	$R_{\Theta JC}$	0.27	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

Ordering Information

Ordering code	Package type	Packing method[3]	Qty	Part Marking	Origin	ECCN
TDG650E60TEP	GaN*PX*® Top-side Cooled	Mini-Reel	250	T60TE	US	EAR99
TDG650E60TEPF	GaN*PX*® Top-side Cooled	Mini-Reel	250	T60TF	EU	EU

(3) See page 19 for tape and reel information.

Electrical Characteristics

Typical values at TJ = 25 °C, VGS = 6 V. Unless otherwise noted, Min/Max values are specified over the full temperature range from TJ = -55 °C to TJ = 150 °C based on Teledyne Dynamic Burn-In[6] after 15k Cycles.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V, I_{DSS} = 100 µA T_J = 25 °C
Drain-to-Source On Resistance	$R_{DS(on)}$	11	25	60	mΩ	V_{GS} = 6 V I_{DS} = 18 A
Dynamic Drain-to-Source On Resistance Shift	$D_{RDS(on)}$		19		%	V_{GS} = 6 V I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 14 mA
Gate-to-Source Current	I_{GS}		0.320	12	mA	V_{GS} = 6 V, V_{DS} = 0 V
Gate-to-Source Current	I_{GS}			31	µA	V_{GS} = 6 V, V_{DS} = 0 V, T_J = -55 °C
Gate Plateau Voltage	V_{plat}		3.0		V	V_{DS} = 400 V, I_{DS} = 60 A
Drain-to-Source Leakage Current	I_{DSS}		4	80	µA	V_{DS} = 650 V, V_{GS} = 0 V
Drain-to-Source Leakage Current	I_{DSS}			1.2	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_J = -55 °C
Internal Gate Resistance	R_G		0.3		Ω	f = 25 MHz, open drain
Input Capacitance	C_{ISS}		518		pF	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		126		pF	
Reverse Transfer Capacitance	C_{RSS}		5.9		pF	
Effective Output Capacitance Energy Related[4]	$C_{O(ER)}$		207		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related[5]	$C_{O(TR)}$		335		pF	
Total Gate Charge	Q_G		14.2		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		3.8		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.
(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.
(6) For more details over the dynamic Burn-In, please contact Teledyne e2v HiRel.

Electrical Characteristics <continued> (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Gate-to-Drain Charge	Q_{GD}		5.4		nC	
Output Charge	Q_{OSS}		134		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	
Turn-On Delay	$t_{D(on)}$		4.6		ns	V_{DD}= 400 V V_{GS} = 0 - 6 V I_D = 16 A, $R_{G(ext)}$ = 5 Ω T_J= 25 °C[7]
Rise Time	t_R		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	t_F		22		ns	
Output Capacitance Stored Energy	E_{OSS}		17		µJ	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Switching Energy during turn-on	E_{on}		134		µJ	V_{DS} = 400 V, I_{DS} = 20 A V_{GS} = 0-6 V, $R_{G(on)}$ = 10 Ω $R_{G(off)}$ = 1 Ω L = 120 µH L_P = 2 nH [8, 9]
Switching Energy during turn-off	E_{off}		17		µJ	

(7) See Figure 21 and Figure 22 for timing test circuit diagram and definition waveforms.
(8) LP is the switching circuit parasitic inductance.
(9) See Figure 23 for switching test circuit.

Electrical Performance Graphs

I_{DS} vs. V_{DS} Characteristic

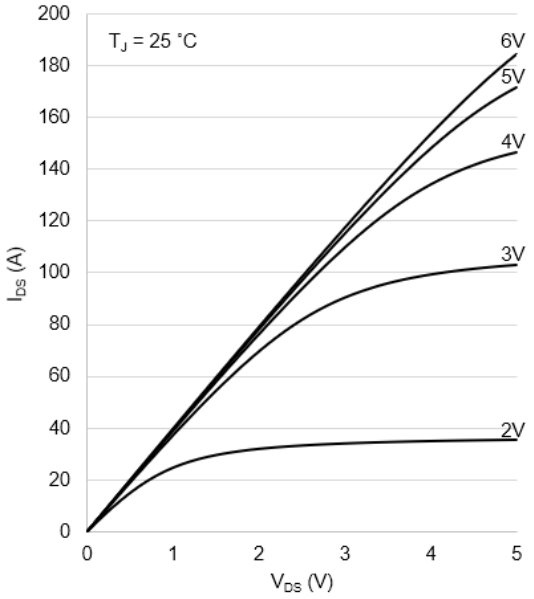


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 ºC

I_{DS} vs. V_{DS} Characteristic

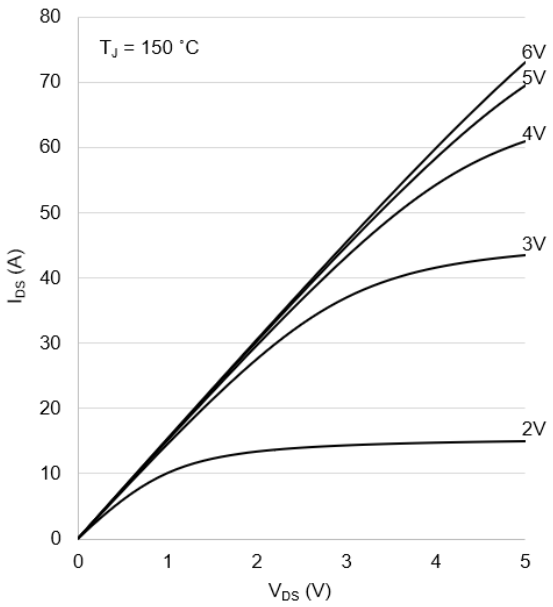


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 ºC

$R_{DS(on)}$ vs. I_{DS} Characteristic

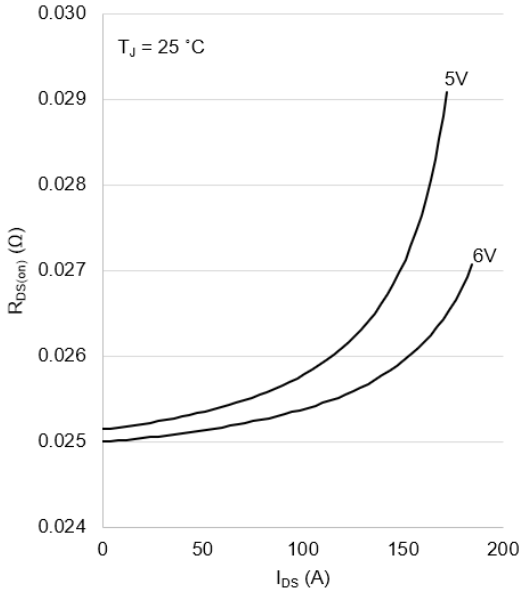


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 ºC

$R_{DS(on)}$ vs. I_{DS} Characteristic

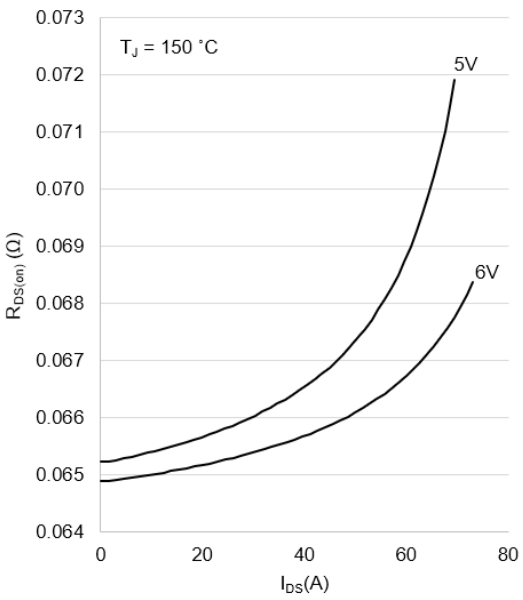


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150ºC

Electrical Performance Graphs

I_{DS} vs. V_{DS}, T_J Dependence

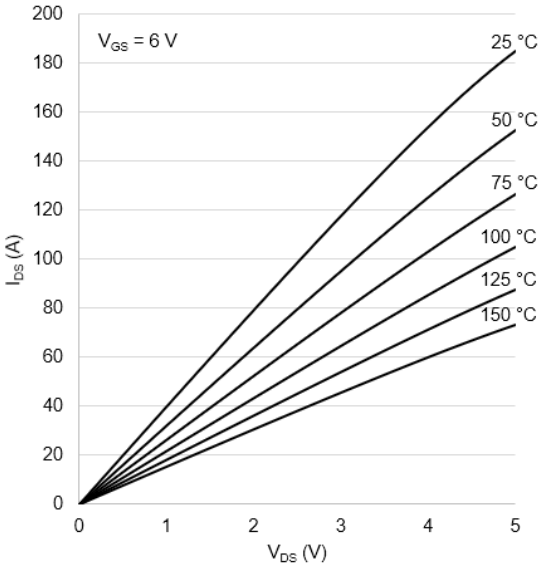


Figure 5: Typical IDS vs. VDS @ VGS = 6 V

Gate Charge, Q_G Characteristic

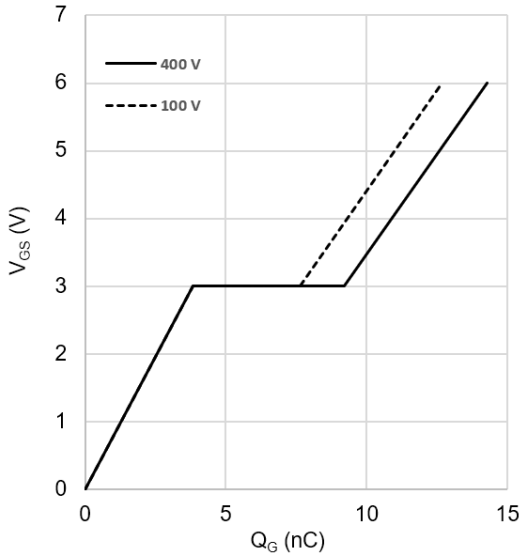


Figure 6: Typical VGS vs. QG @ VDS = 100, 400 V

Capacitance Characteristics

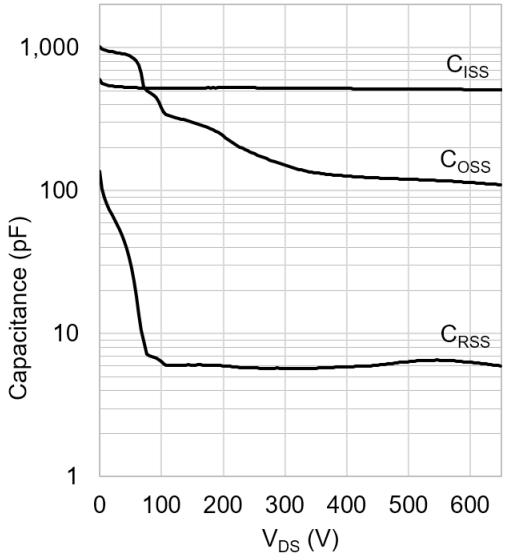


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

Stored Energy Characteristic

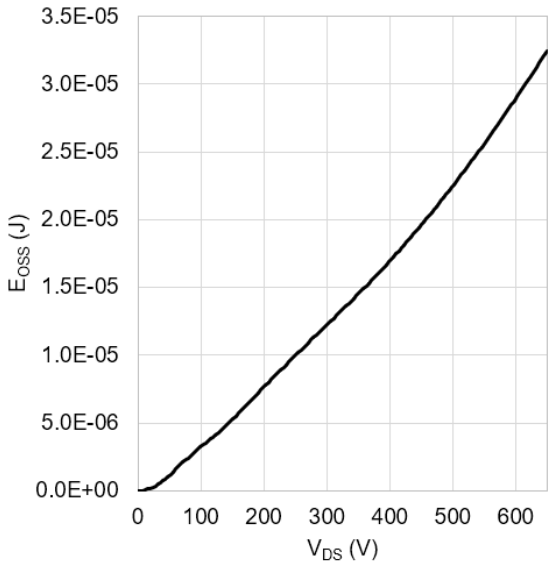


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

Reverse Conduction Characteristics

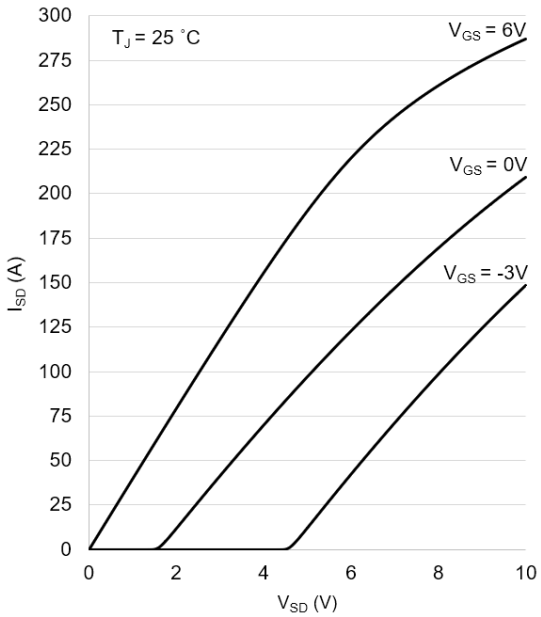


Figure 9: Typical I_{SD} vs. V_{SD} (T_J= 25 °C)

Reverse Conduction Characteristics

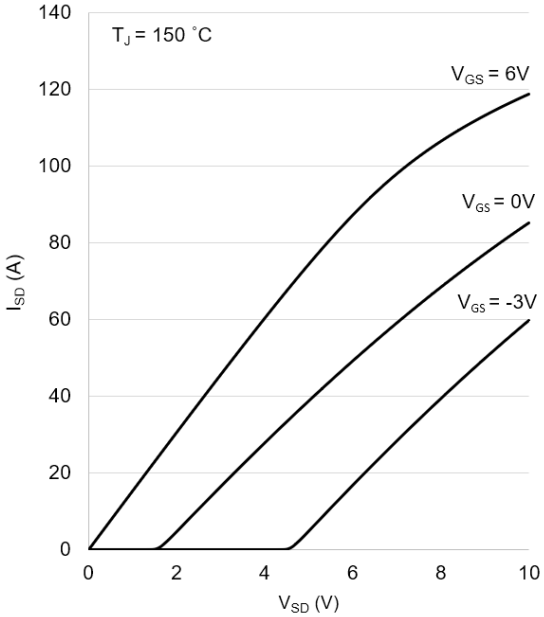


Figure 10: Typical I_{SD} vs. V_{SD} (T_J= 150 °C)

I_{DS} vs. V_{GS} Characteristic

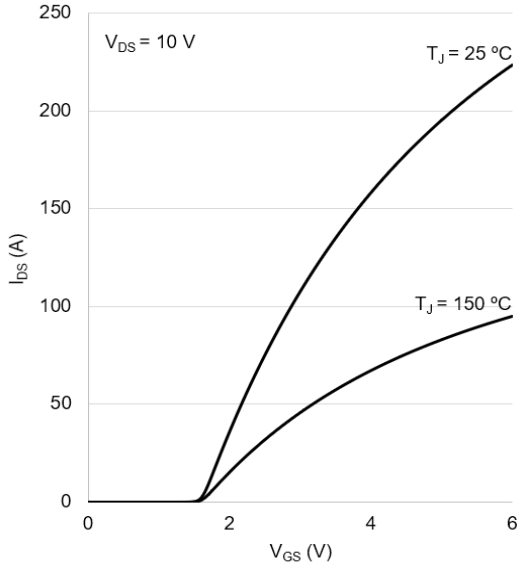


Figure 11: Typical I_{DS} vs. V_{GS}

Normalized $R_{DS(on)}$ vs T_J

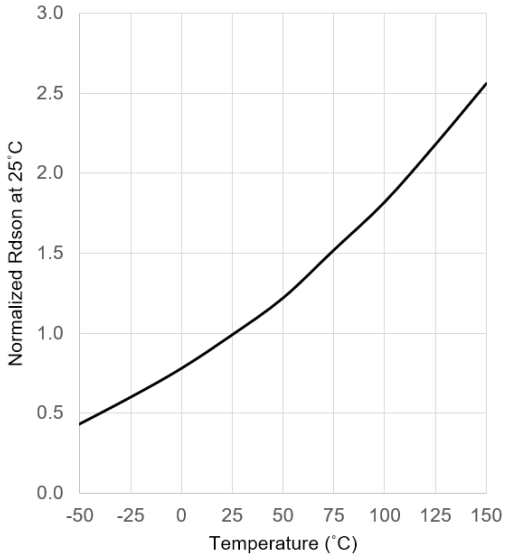


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Electrical Performance Graphs

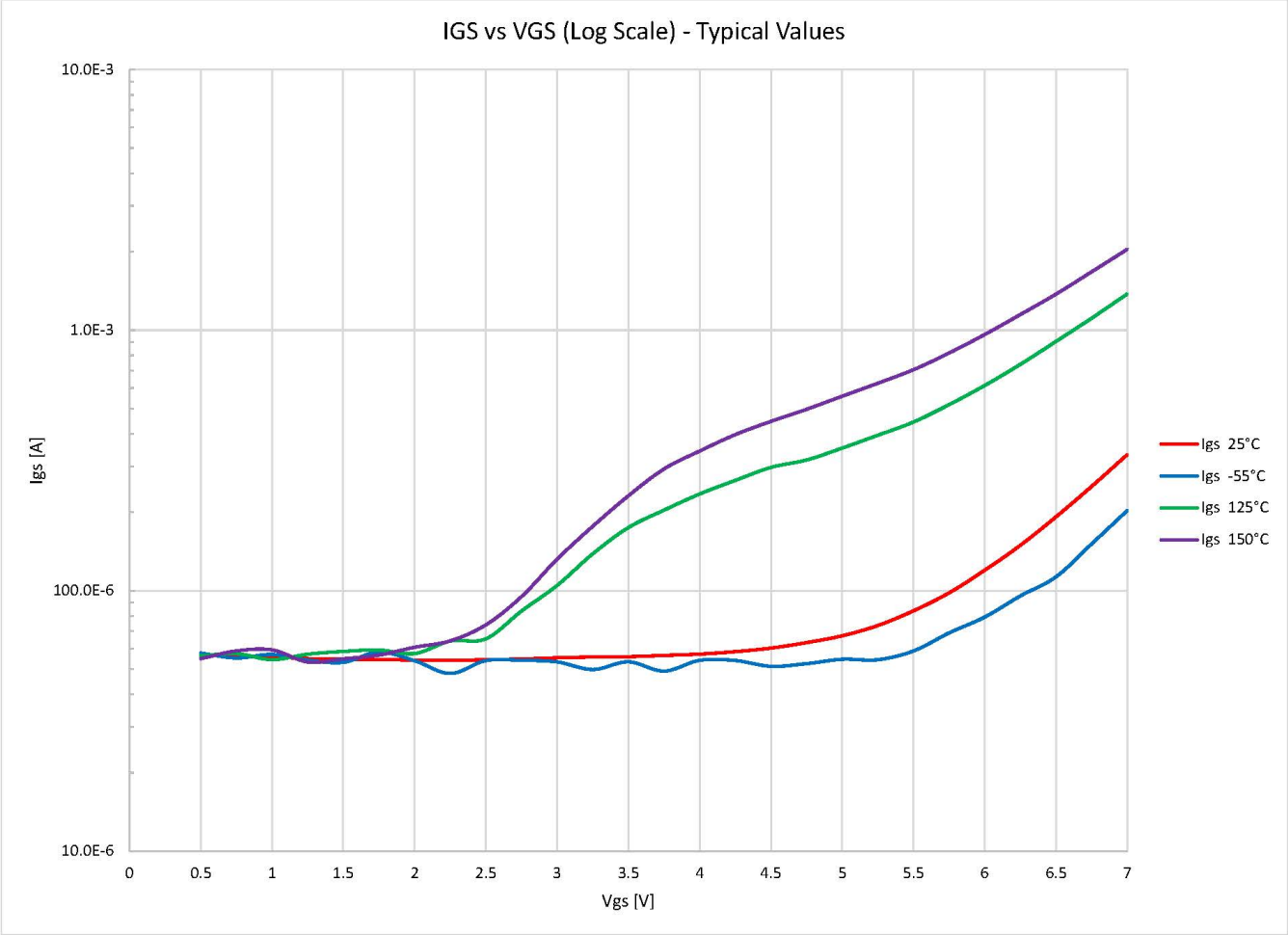


Figure 13: Typical I_{GS} vs V_{GS}

Electrical Performance Graphs

I_{DS} vs V_{DS} SOA

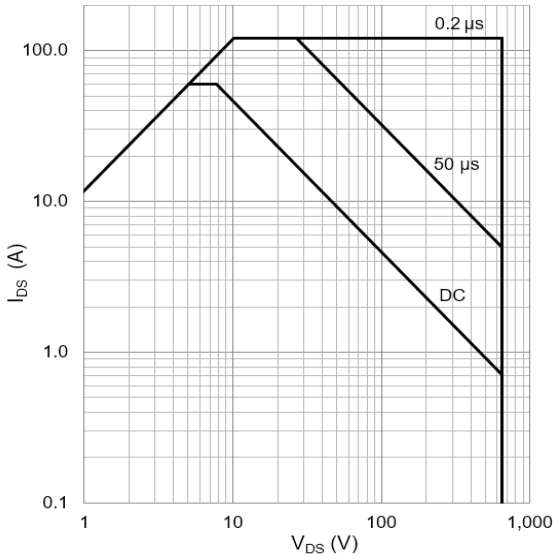


Figure 14: Safe Operating Area, T_{case} = 25 °C

I_{DS} vs V_{DS} SOA

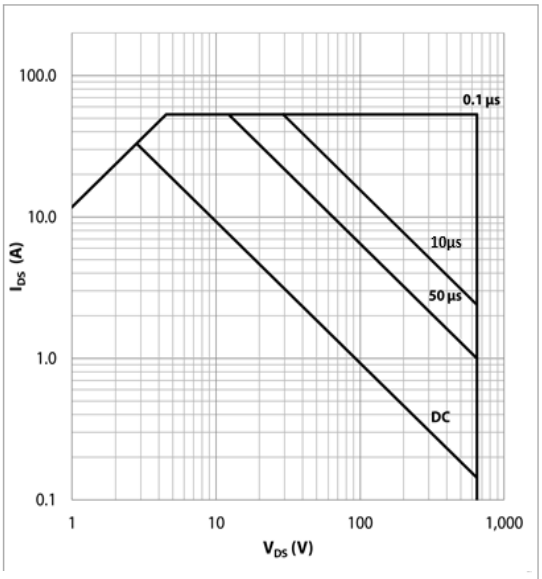


Figure 15: Safe Operating Area, Tcase = 125 °C

Transient RθJC

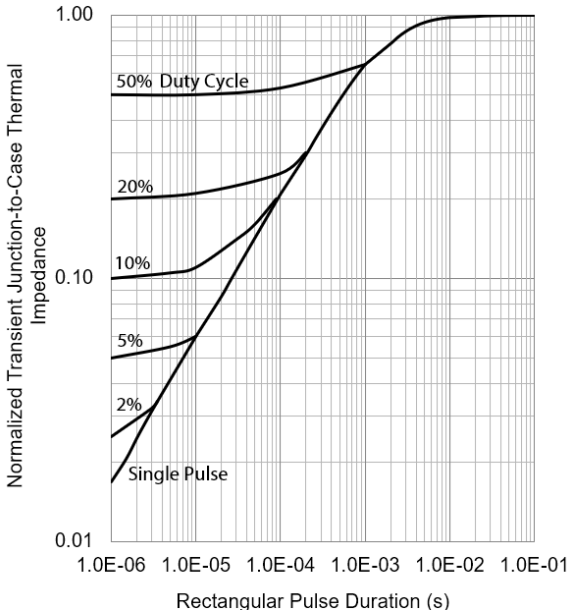


Figure 16: Transient Thermal Impedance
(1.00 = Nominal dc thermal impedance)

Power Dissipation Temperature Derating

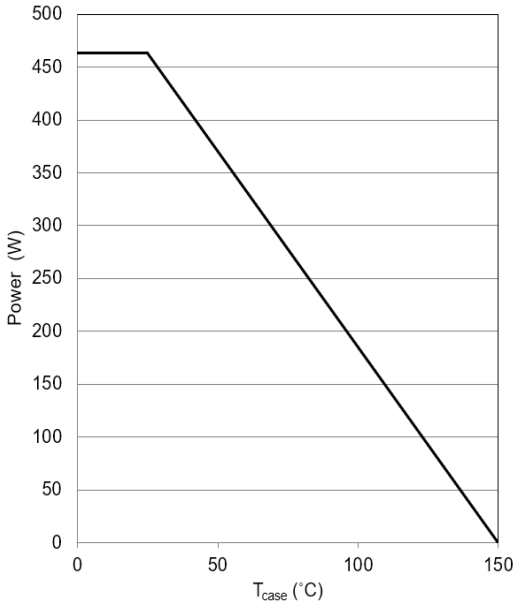


Figure 17: Derating vs. Case Temperature

Electrical Performance Graphs

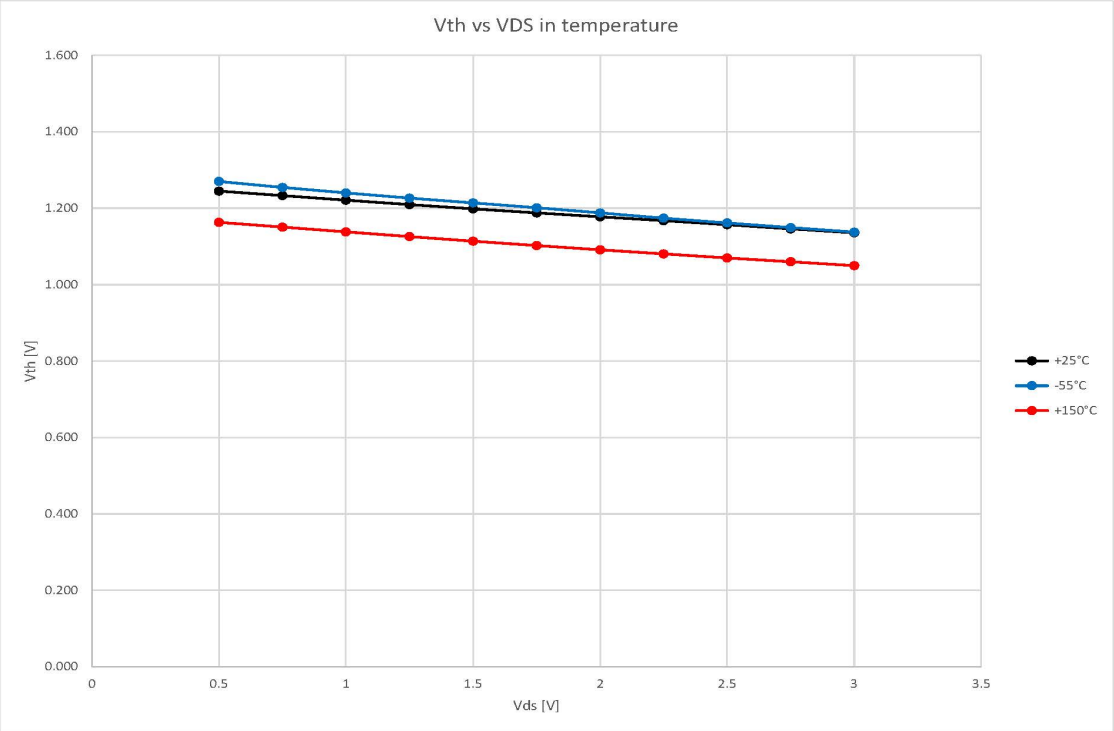


Figure 18: V_{TH} vs V_{DS}

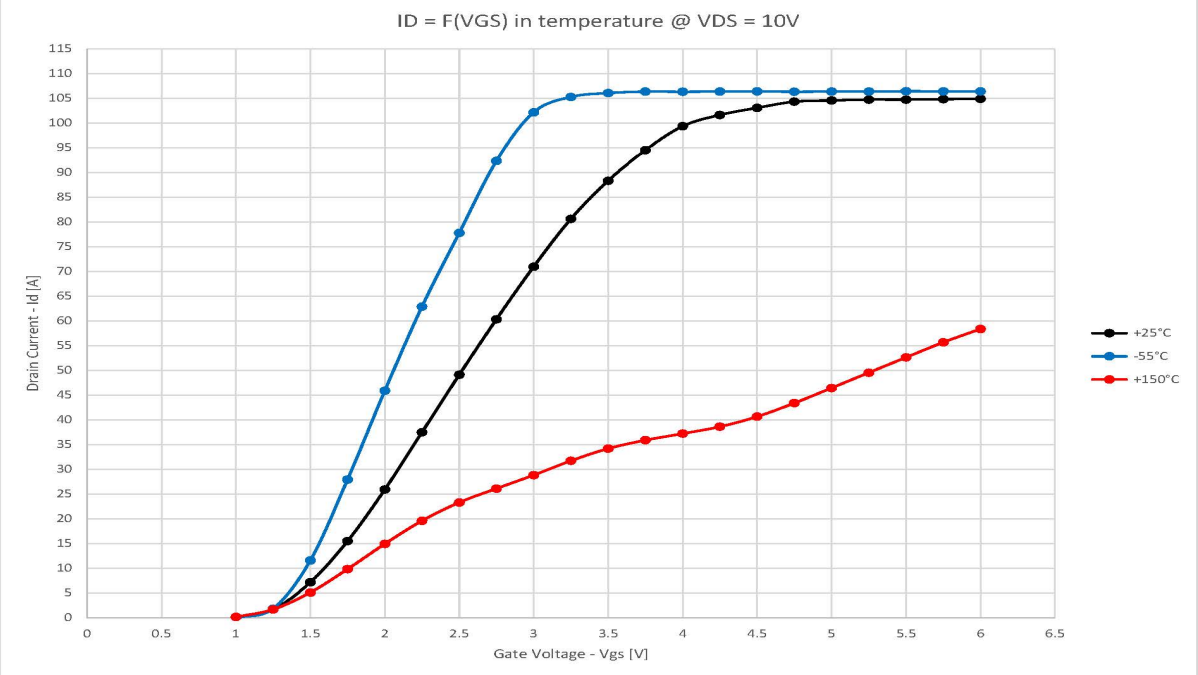


Figure 19: I_D vs V_{GS}

Electrical Performance Graphs

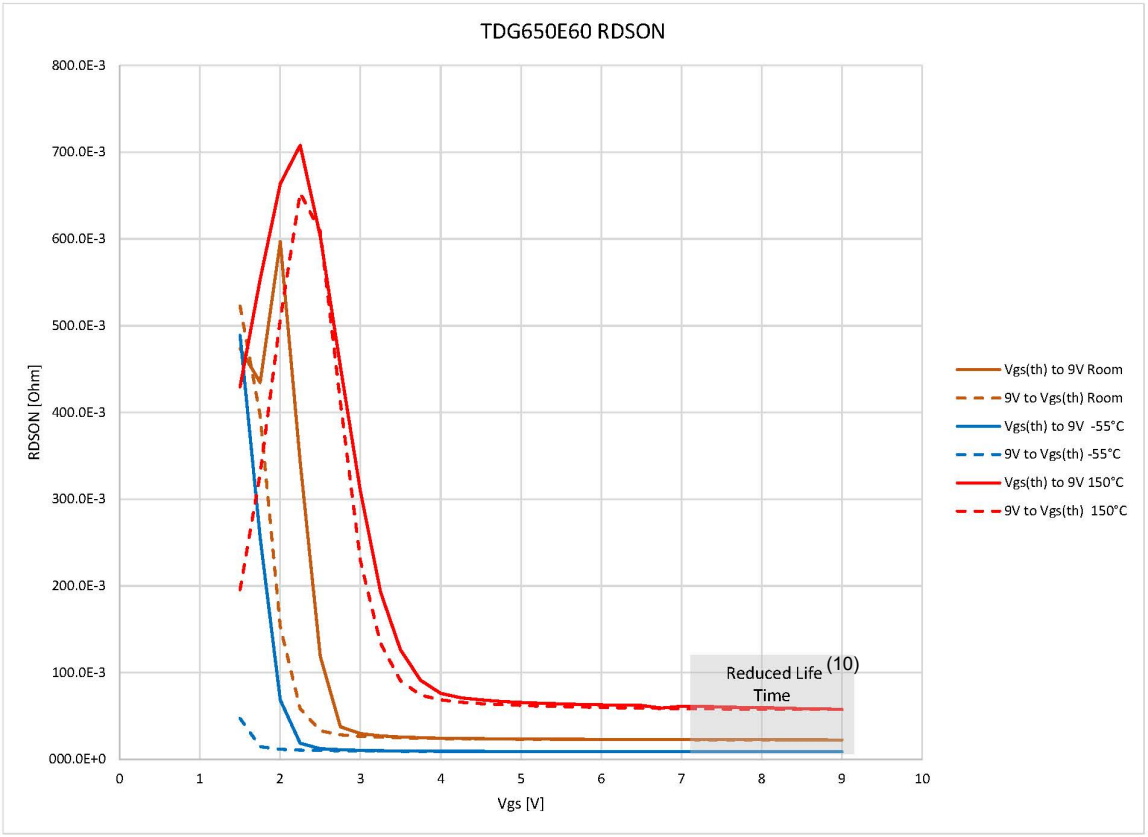


Figure 20: $R_{DS(ON)}$ vs V_{GS} vs Temp

(10) Contact manufacturer for more information.

Test Circuits

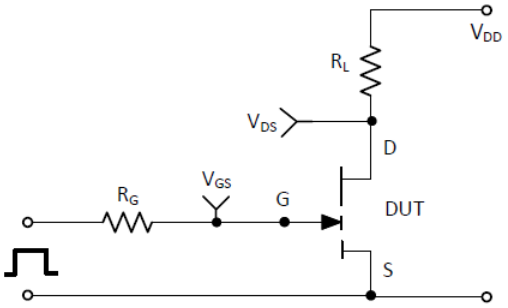


Figure 21: switching time test circuit

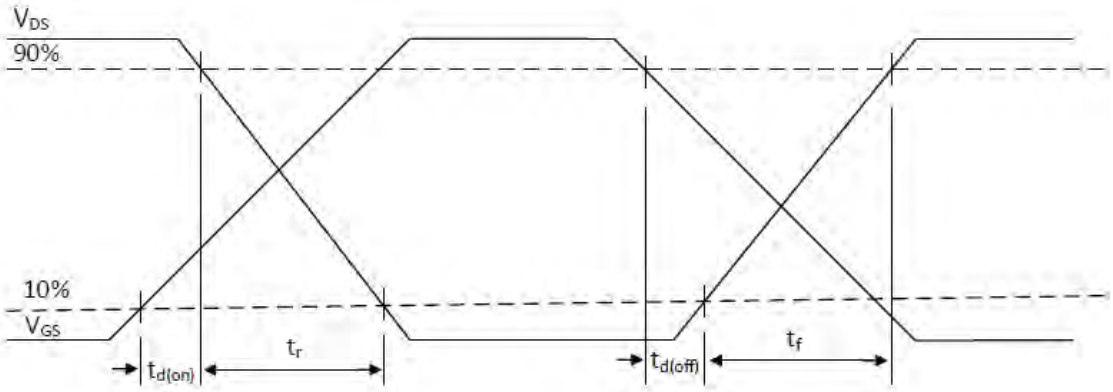


Figure 22: switching time waveforms

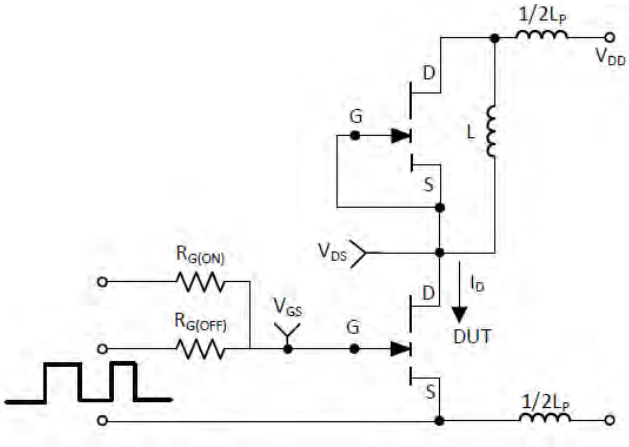


Figure 23: Switching Loss Test Circuit

Application Information

Gate Drive

The recommended gate drive voltage range, V_{GS}, is 0 V to + 6 V for optimal $R_{DS(on)}$ performance. Also, the repetitive gate to source voltage, maximum rating, $V_{GS(AC)}$, is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically V_{GS} = -3 V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at www.gansystems.com

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

The dual gate drive pins are used to achieve balanced gate drive, especially useful in parallel GaN transistors operation. Both gate drive pins are internally connected to the gate, so only one needs to be connected. Connecting both may lead to timing improvements at very high frequencies. The two gates on the top-side cooled device are not designed to be used as a signal pass-through. When multiple devices are used in parallel, it is not recommended to use one gate connection to the other (on the same transistor) as a signal path for the gate drive to the next device. Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

Although the device does not have a dedicated source sense pin, the GaN*PX*® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection on the PCB to the Source pad in a kelvin configuration, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

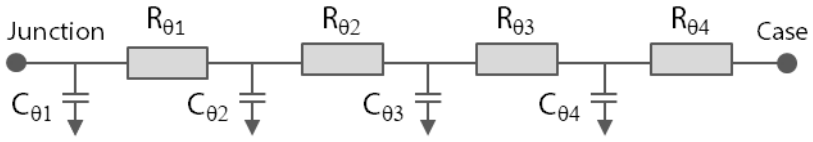
Thermal

The substrate is internally connected to the thermal pad on the top-side and to the source pin on the bottom side of the package. The transistor is designed to be cooled using a heat sink on the top of the device. The Drain and Source pads are not as thermally conductive as a thermal pad. However, adding more copper under these two pads will improve thermal performance by reducing the packaging temperature.

Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This thermal model can be extended to the system level by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model:



RC breakdown of RΘJC

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.008	$C_{\theta 1}$ = 1.48E-04
$R_{\theta 2}$ = 0.124	$C_{\theta 2}$ = 1.37E-03
$R_{\theta 3}$ = 0.130	$C_{\theta 3}$ = 12.0E-03
$R_{\theta 4}$ = 0.008	$C_{\theta 4}$ = 3.7E-03

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*® Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-state are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (V_{GD}) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop “V_F” and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $V_{(BL)DSS}$, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated $V_{(BL)DSS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and does not change with negative gate voltage. GaN Systems tests devices in production with a 750V Drain-to-source voltage pulse to insure blocking voltage margin.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

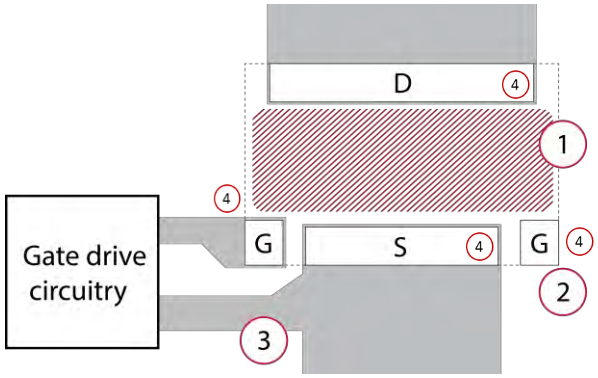
Using “No-Clean” soldering paste and operating at high temperatures may cause a reactivation of the “No-Clean” flux residues. In extreme conditions, unwanted conduction paths may be created.

Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "No-Clean" paste residues.

Avoid placing printed circuit board traces with high differential voltage to the source or drain directly underneath the top-cooled package on the PCB to avoid potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.

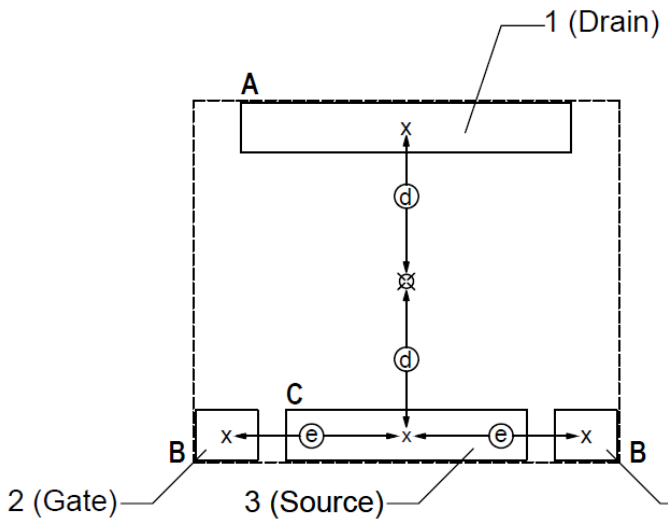
Routing Guidelines

The following layout recommendations are highlighted. Additional detail is provided in Application Note GN001 at www.gansystems.com.



1. Keep out area: Avoid placing traces or vias on the top layer of the PCB, directly underneath the package. This is to prevent potential electro-migration and solder mask isolation issues during high temperature or/and voltage operation.
2. Symmetrical dual gates are provided for flexible layout and easy paralleling. Either gate drive can be used. If the second gate is not used, it should be left floating.
3. A separate Source Sense pin is not provided on our top-side products because of the ultra-low inductance of our GaN*PX*® packaging. The Source Sense pin functionality can be implemented simply by routing a Kelvin connection at the side of the Source pad. This can be done at either side of the source pad for layout optimization.
4. Do not route vias within the Gate pad as it may affect long term solder joint reliability. For other pads, it is recommended to implement filled vias for better solder joint reliability.

Recommended Minimum Footprint for Printed Circuit Board



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	6.94	1.05	0.273	0.041
B	1.30	1.05	0.051	0.041
C	5.07	1.05	0.200	0.041

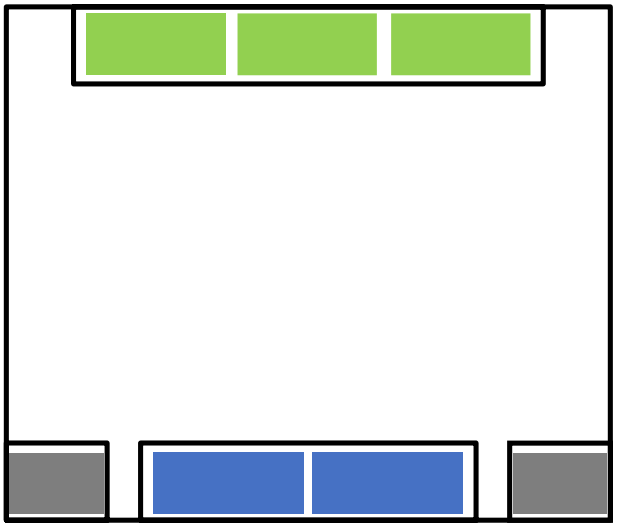
Dimensions

	mm	Inches
d	3.22	0.127
e	3.77	0.149

PCB pad openings

Package outline

Recommended Solder Stencil for Top-side Cooled PCB Footprint



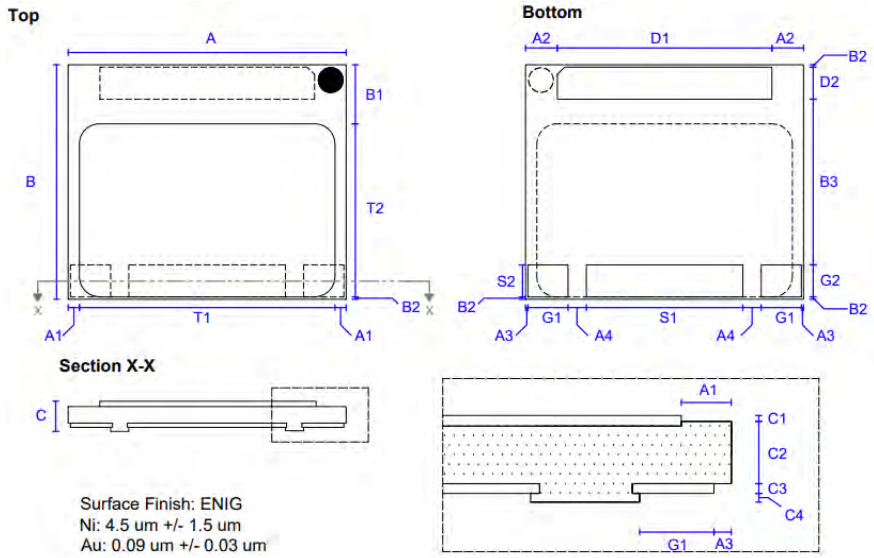
Dimension of stencil aperture

1.3 x 0.9 mm
2.32 x 0.9 mm
2.1 x 0.9 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

The TDG650E60T offers top-side thermal transfer through a heat-sink attached directly to the device. The top-side cooling interface offers advantages such as keeping the thermal transfer path outside the PCB, but care must be taken with the mechanical interface between the heat sink and package to prevent damage to the device. For more details, please refer to the thermal design guide application note " GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices" at www.gansystems.com

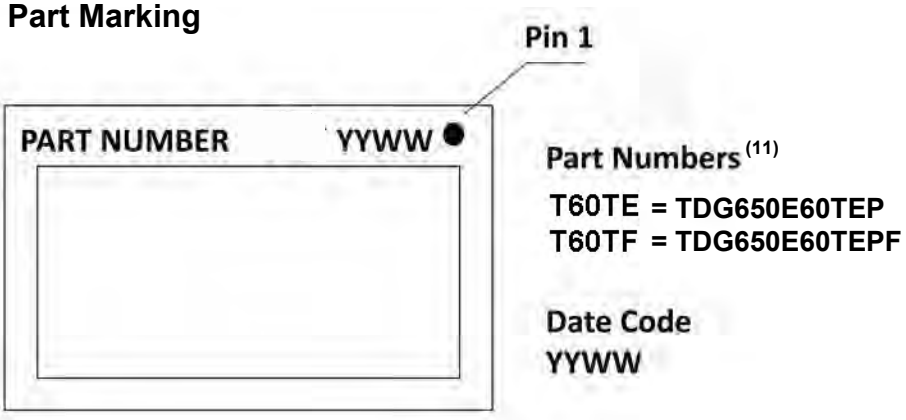
Package Dimensions



	mm	Inches*	
A	9.00	0.354	+/- 0.100 mm (0.004")
A1	0.37	0.015	+/- 0.050 mm (0.002")
A2	1.03	0.041	+/- 0.050 mm (0.002")
A3	0.08	0.003	+/- 0.050 mm (0.002")
A4	0.59	0.023	
B	7.64	0.301	+/- 0.100 mm (0.004")
B1	1.93	0.076	+/- 0.050 mm (0.002")
B2	0.08	0.003	+/- 0.050 mm (0.002")
B3	5.39	0.212	
C	0.54	0.022	+/- 0.081 mm (0.003")
C1	0.04	0.002	
C2	0.38	0.015	
C3	0.07	0.003	
C4	0.05	0.002	
D1	6.94	0.273	
D2	1.05	0.041	
G1	1.30	0.051	
G2	1.05	0.041	
S1	5.07	0.200	
S2	1.05	0.041	
T1	8.27	0.326	
T2	5.64	0.222	

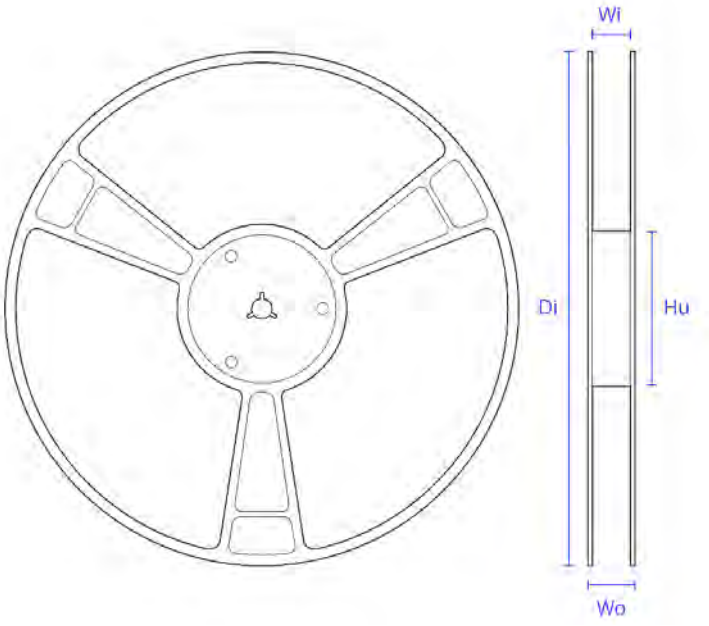
*Inch measurements are approximate values

Part Marking



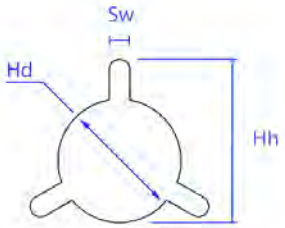
(11) Reference Ordering Information on Page 2.

Tape and Reel Information

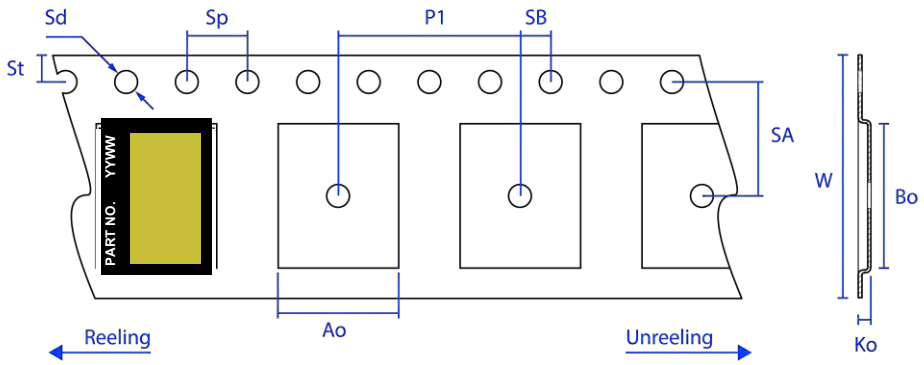


Dimensions (mm)

13 inch reel	Min	Max	7 inch reel	Min	Max
Di	328.5	331.5	Di	178.0	180.0
Wo		30.4	Wo	26.4	28.7
Wi	24.4	26.4	Wi	25.0	26.0
Hu	98.5	104.0	Hu	60.0	61.0
Hh	16.45	17.4	Hh	16.5	17.5
Sw	1.5	2.5	Sw	1.5	2.5
Hd	12.8	13.5	Hd	12.8	13.2



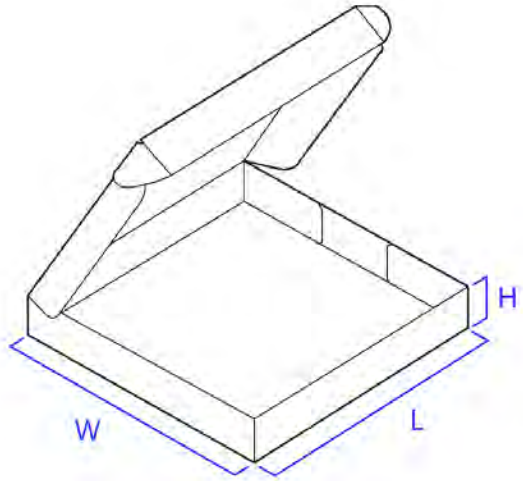
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	12.00	+/- 0.1
W	16.00	+/- 0.3
Ko	0.80	+/- 0.1
Ao	7.95	+/- 0.1
Bo	9.50	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	7.50	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



Outside dimensions (mm)

13 inch reel			7 inch reel		
	Min	Max		Min	Max
W	197.0	203.5	W	337.0	342.0
L	204.0	218.5	L		355.0
H		32.0	H	50.0	53.0

Document Revision History:

Document No.	Description	Date
TDG650E60 Rev 180725d_1	Initial Release	12/17/2019
TDG650E60 04_2020 Rev1	• Updated Absolute Maximum Ratings table • Updated Electrical Characteristics table • Updated Electrical Performance Graphs • Added Recommended Solder Stencil	4/8/2020
TDG650E60TEP 11_05_2021 Rev2	• Split data sheet = Initial Release of the stand-alone, top-side cooled data sheet • Thermal Resistance Changed • Tolerance Thickness of the package changed • Additional Information (Plots) • Internal gate resistance changed	11/05/2021
TDG650E60TEP 12_07_2021 Rev3	• Page 3: Drain-to-Source Blocking Voltage Changed from 650 V Typical to 650 V Minimum • Page 11: Fig. 20 Reduced Life Time shaded portion of graph changed from a minimum of 6 V to ~7 V.	12/07/2021
TDG650E60TEP 03_13_2023 Rev4	• Updated Igs and Idss specifications/page 3/remove Mins and Typs and added Max	03/13/2023

Document Categories

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Teledyne e2v HiRel Electronics reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Teledyne e2v HiRel Electronics decides to change the specifications, Teledyne e2v HiRel Electronics will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

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