TDG100E90BSP
Bottom-side cooled, 100V E-mode GaN transistor
Product Specification

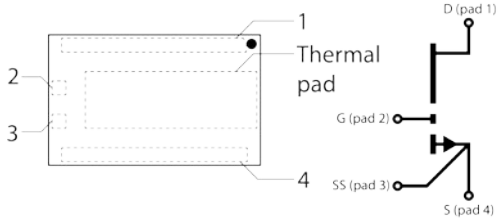
Features

- 100 V enhancement mode GaN power switch
- Bottom-side cooled configuration
- RDS(on) = 7 mΩ
- IDS(max) = 90 A
- Ultra-low FOM Island Technology® die
- Low inductance GaNPX® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 100 MHz)
- Reverse current capability
- Zero reverse recovery loss
- Small 7.6 x 4.6 mm2 PCB footprint
- Source Sense (SS) pin for optimized gate drive
- Single diffusion lot available
- RoHS compliant
- Enhanced wafer level reliability
- HiRel qualification flow
- Class one / Level one Production Screening
- Lot Acceptance Test options available
- Obsolescence support

Applications

- High efficiency power conversio
- High density power conversion
- ac-dc Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half & Full Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Space Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- dc-dc Converters
- On Board Battery Chargers
- E-Switch

Package Outline **Circuit Symbol**



The thermal pad must be connected to Source, S (pad 4), for best performance

Description

The TDG100E90BSP is an enhancement mode GaN-on-silicon power transistor based on GaN Systems Technology. The properties of GaN ensure high current, high voltage breakdown combined with high switching frequency. GaN Systems implements patented Island Technology® cell layout for high-current performance.

GaNPX® packaging is designed for very low parasitic inductance in the smallest possible footprint. The TDG100E90BSP is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combined provide very high efficiency power switching. The high performance of the TDG650E30BSP makes it ideal for satellite applications.

These parts go through NASA Level 1 or ESA Class 1 screening flow and can be brought up to full Level 1 conformance with extra qualification testing, if desired. Each device is available with options for EAR99 or European sourcing.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Drain-to-Source Voltage - transient (note 1)	$V_{DS(transient)}$	120	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case} = 25 °C)	I_{DS}	90	A
Continuous Drain Current (T_{case} = 100 °C)	I_{DS}	65	A
Pulse Drain Current (Pulse width 50 µs, VGS = 6 V)	IDS Pulse	140	A

(1) Pulse ≤1 µs

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case)	$R_{\Theta JC}$	0.55	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	7	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	23	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(2) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Electrical Characteristics

Typical values at TJ = 25 °C, VGS = 6 V. Unless otherwise noted, Min/Max values are specified over the full temperature range from TJ = -55 °C to TJ = 150 °C based on Teledyne Dynamic Burn-In[5] after 15k Cycles.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	100			V	V_{GS} = 0 V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$	6	7	9.5	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 27 A
Drain-to-Source On Resistance	$R_{DS(on)}$	12.1	17.5	20	mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 27 A
Dynamic Drain-to-Source On Resistance Shift	$DR_{DS(on)}$		8.1		%	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 27 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 7 mA
Gate-to-Source Current	I_{GS}		0.20	6	mA	V_{GS} = 6 V, V_{DS} = 0 V TJ = 150 °C
Gate Plateau Voltage	V_{plat}		3.5		V	V_{DS} = 100 V, I_{DS} = 90 A
Drain-to-Source Leakage Current	I_{DSS}		0.5	50	µA	V_{DS} = 100 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		100	265	µA	V_{DS} = 100 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		0.77		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		600		pF	V_{DS} = 50 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		250		pF	
Reverse Transfer Capacitance	C_{RSS}		12		pF	
Effective Output Capacitance, Energy Related (Note 4)	$C_{O(ER)}$		351		pF	V_{GS} = 0 V V_{DS} = 0 to 50 V
Effective Output Capacitance, Time Related (Note 5)	$C_{O(TR)}$		433		pF	
Total Gate Charge	Q_G		8		nC	V_{GS} = 0 to 6 V V_{DS} = 50 V I_{DS} = 90A
Gate-to-Source Charge	Q_{GS}		3.5		nC	
Gate threshold charge	$Q_{G(th)}$		1.9		nC	
Gate switching charge	$Q_{G(sw)}$		4.1		nC	
Gate-to-Drain Charge	Q_{GD}		1.7		nC	
Output Charge	Q_{OSS}		21.3		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	

Electrical Characteristics (Continued)

Output Capacitance Stored Energy	E_{OSS}		0.39		µJ	VDS = 50 V VGS = 0 V f = 100 kHz
Switching Energy during turn-on	E_{on}		2.8		µJ	VDS = 50 V, IDS = 20 A VGS = -3 - 6 V, RG(on) = 4.7 Ω, RG(off) = 1 Ω L = 28 µH LP = 3.8 nH (notes 5, 6)
Switching Energy during turn -off	E_{off}		1.6		µJ	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated VDS

(4) CO(TR) is the fixed capacitance that would give the same charging time as COSS while VDS is rising from 0 V to the stated VDS.

(5) LP is the switching circuit parasitic inductance.

(6) See Figure 20 for switching loss test circuit.

Electrical Performance Graphs

TDG100E90BSP I_{DS} vs. V_{DS} Characteristic

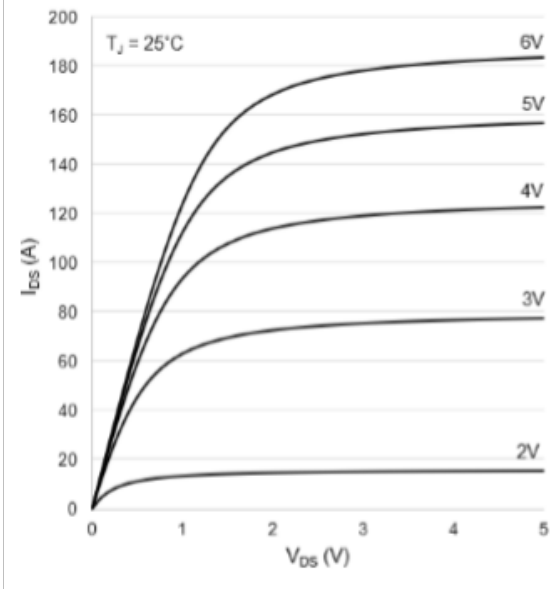


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

TDG100E90BSP I_{DS} vs. V_{DS} Characteristic

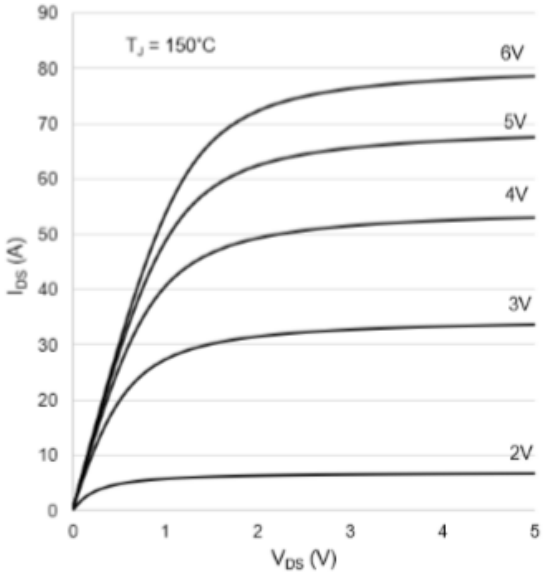


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

TDG100E90BSP $R_{DS(on)}$ vs. I_{DS} Characteristic

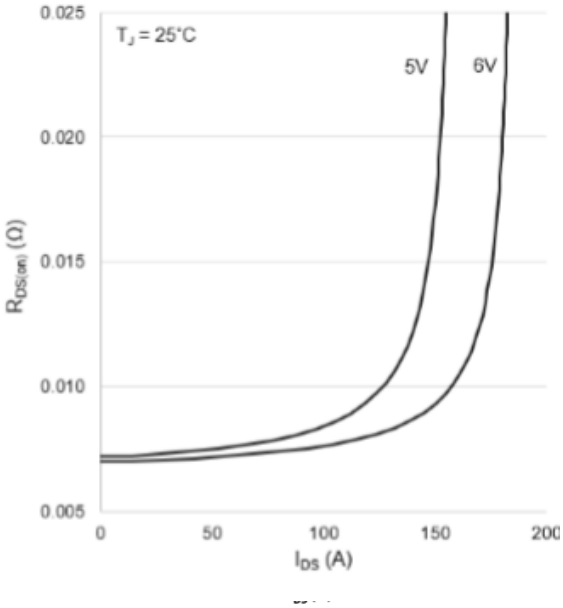


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

TDG100E90BSP $R_{DS(on)}$ vs. I_{DS} Characteristic

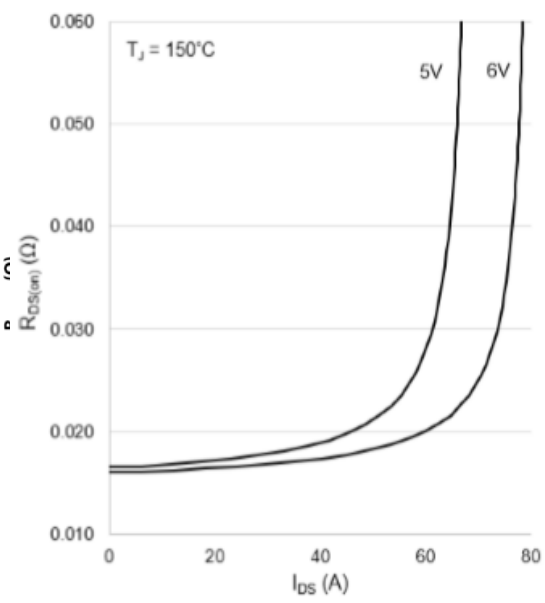


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs (continued)

TDG100E90BSP I_{DS} vs. V_{DS}, T_J dependence

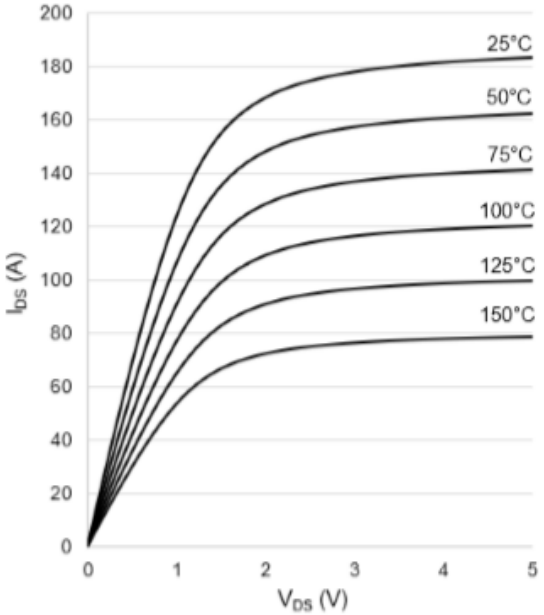


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

TDG100E90BSP Gate Charge, Q_G Characteristic

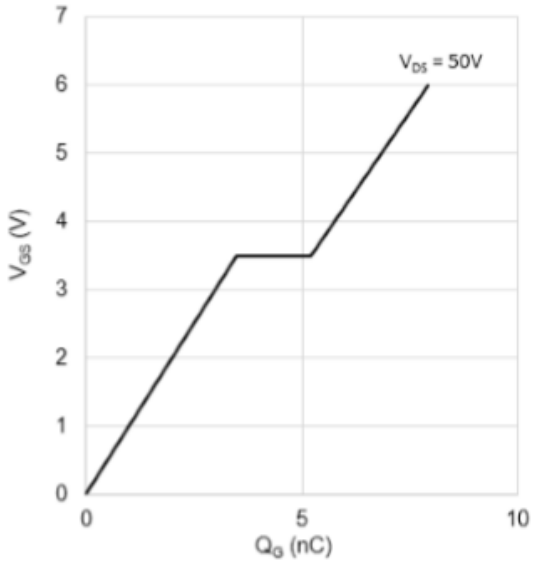


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 50V

TDG100E90BSP Capacitance Characteristics

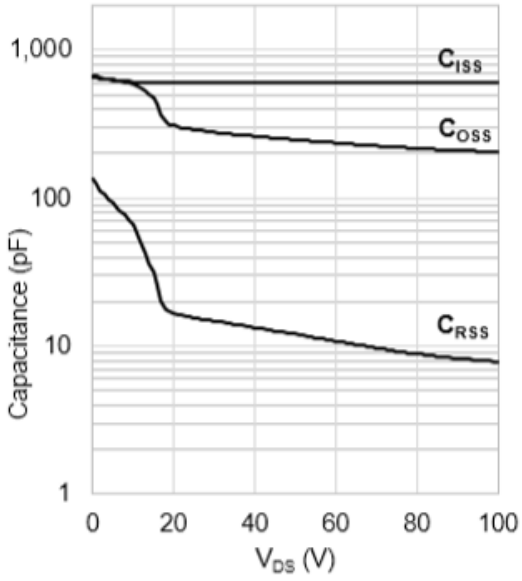


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

TDG100E90BSP Stored Energy Characteristic

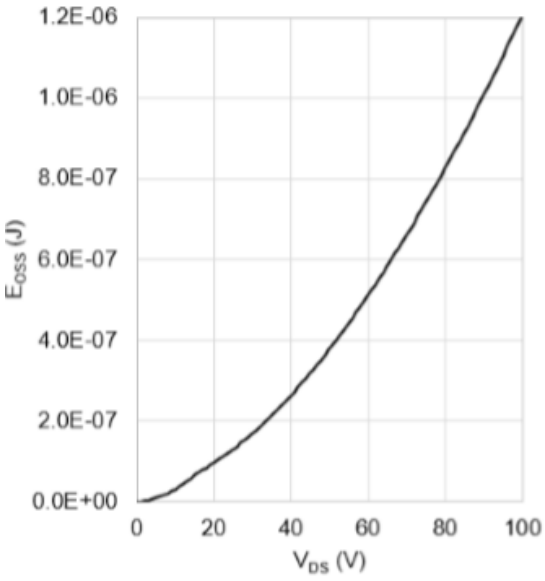


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs (continued)

TDG100E90BSP Reverse Conduction Characteristics

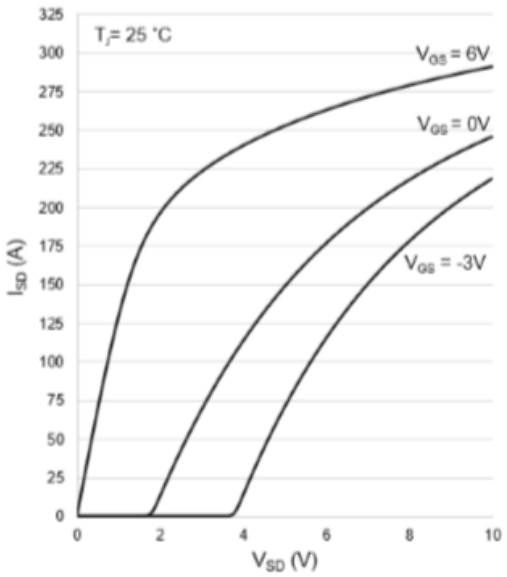


Figure 9: Typical I_{SD} vs. V_{SD} at T_J = 25°C

TDG100E90BSP Reverse Conduction Characteristics

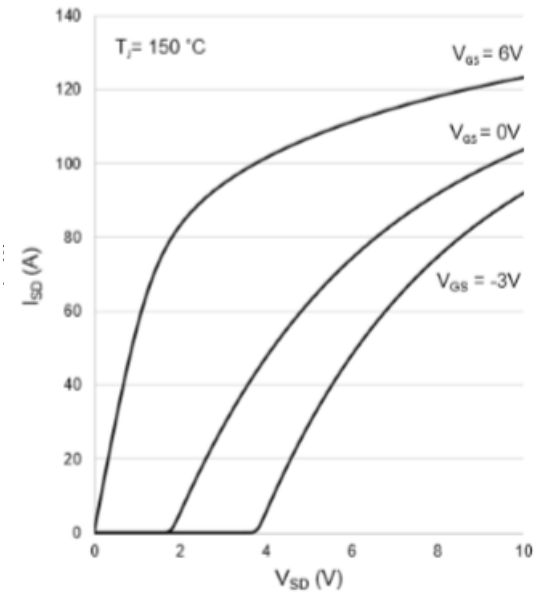


Figure 10: Typical I_{SD} vs. V_{SD} at T_J = 150°C

TDG100E90BSP I_{DS} vs. V_{GS} Characteristic

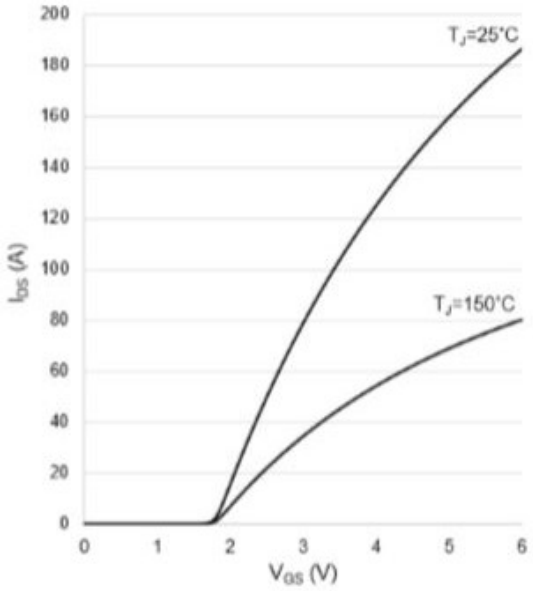


Figure 11: Typical I_{DS} vs. V_{GS}

TDG100E90BSP $R_{DS(on)}$ Temperature Dependence

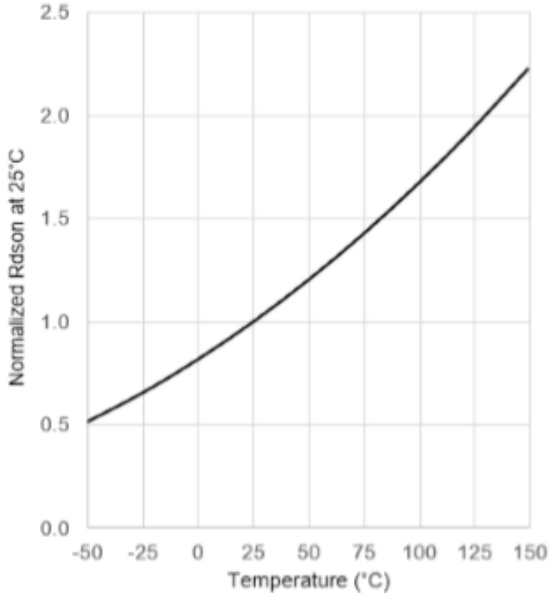


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

Electrical Performance Graphs (continued)

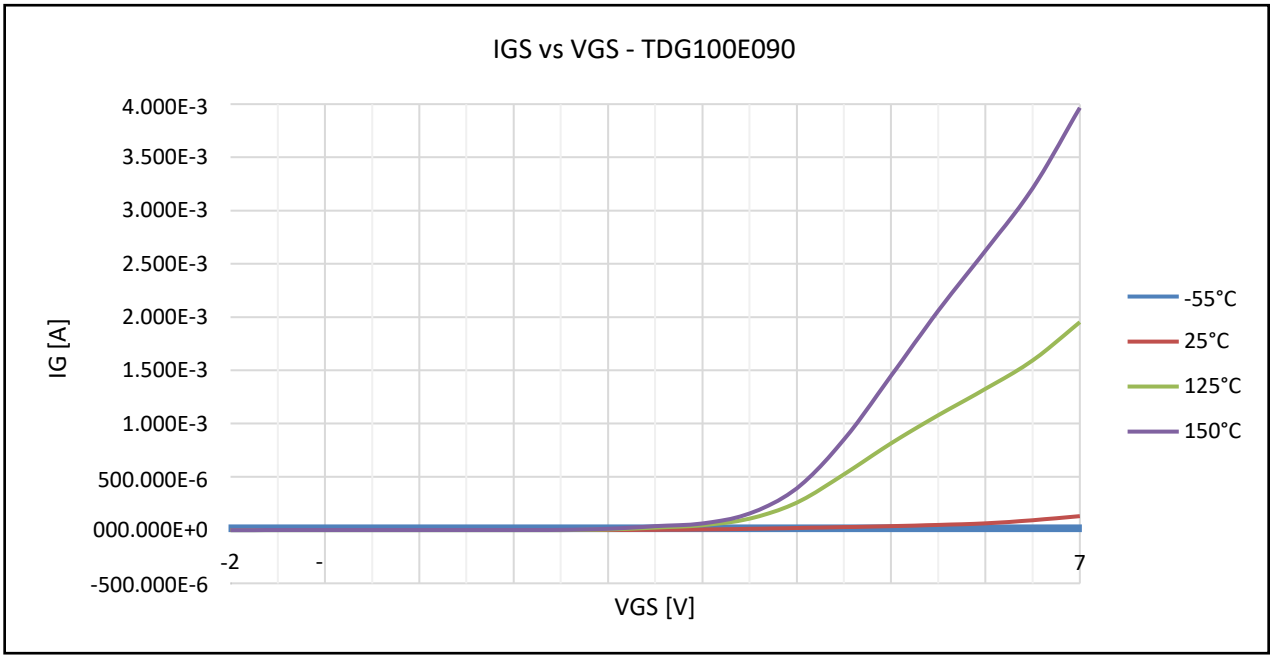


Figure 13: IGS vs VGS - Typical Values

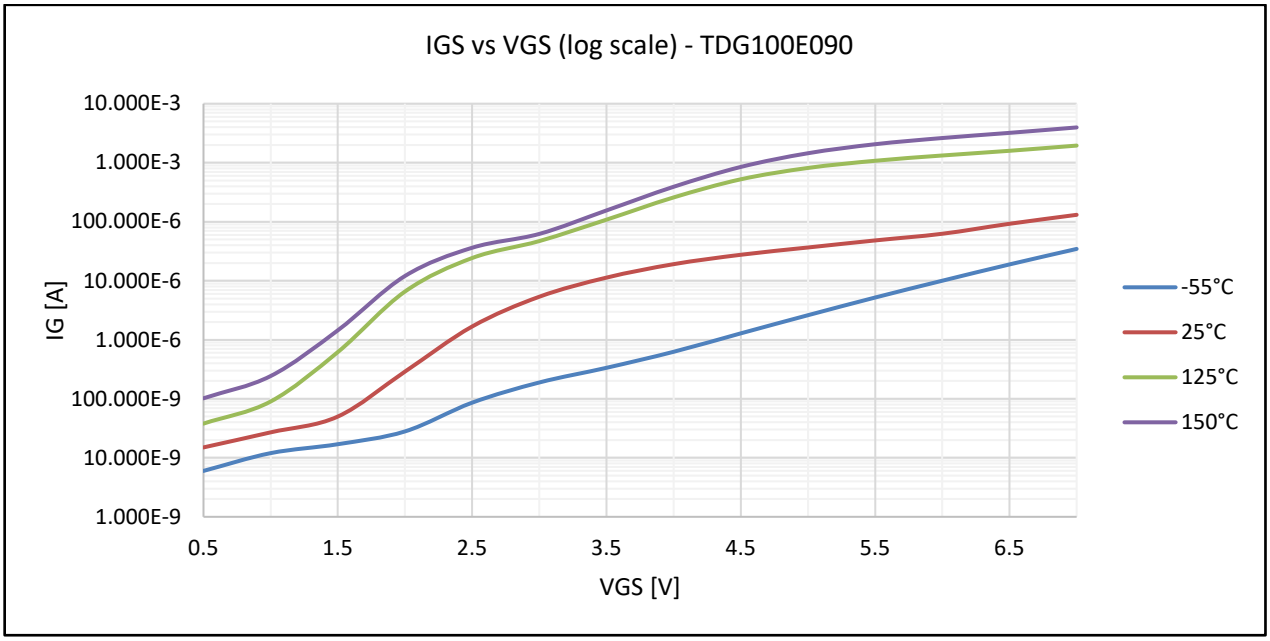


Figure 14: IG vs VGS (log scale) - Typical Values

Electrical Performance Graphs (continued)

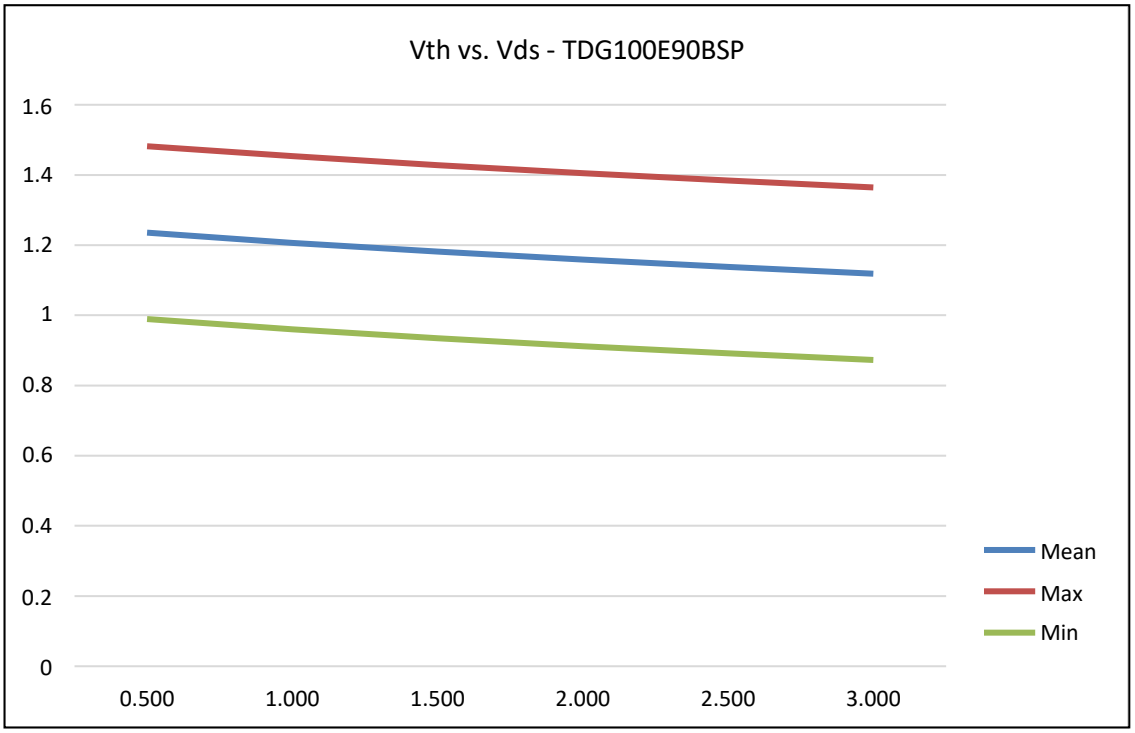


Figure 15: Vth vs. Vds Voltages

Thermal Performance Graphs

TDG100E90BSP I_{DS} - V_{DS} SOA

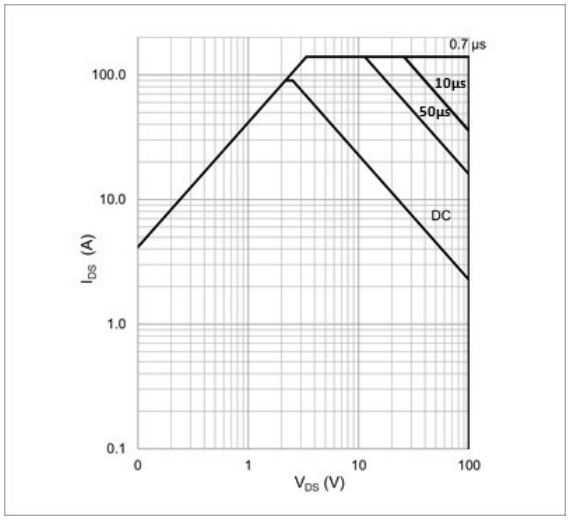


Figure 16: Safe Operating Area @ T_{case} = 25 °C

TDG100E90BSP IDS - VDS SOA

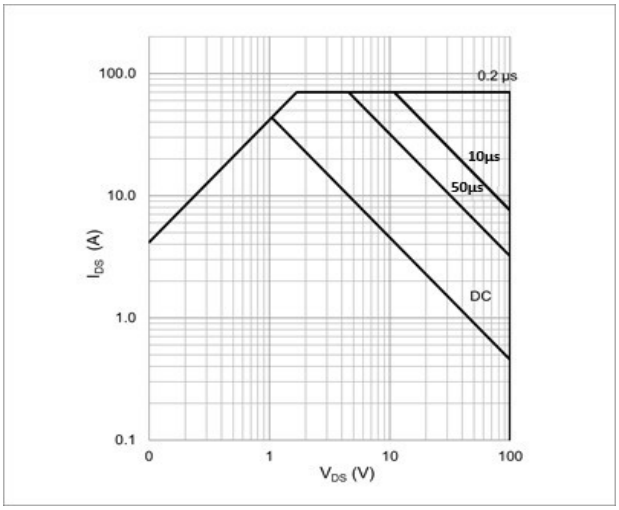


Figure 17: Safe Operating Area @ Tcase = 125 °C

TDG100E90BSP Power Dissipation – Temperature Derating

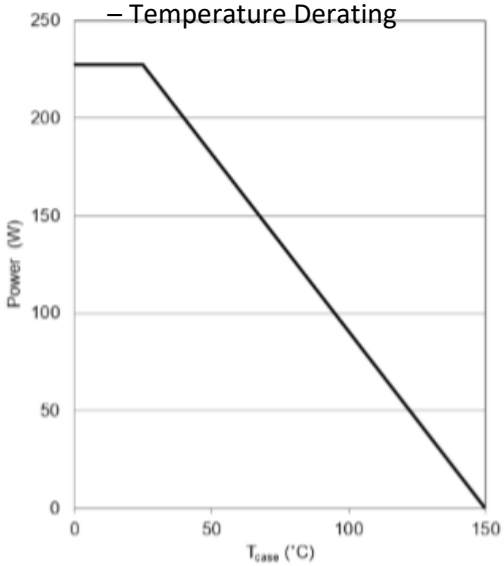


Figure 18: Power Derating vs. T_{case}

TDG100E90BSP Transient $R_{\theta JC}$

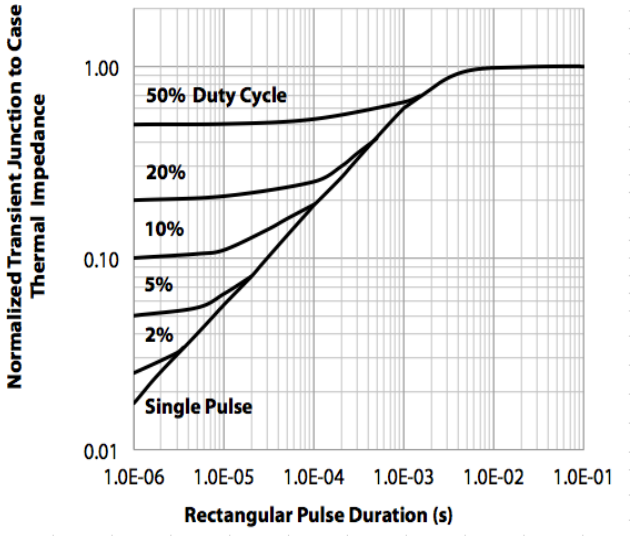


Figure 19: Transient Thermal Impedance

Test Circuit

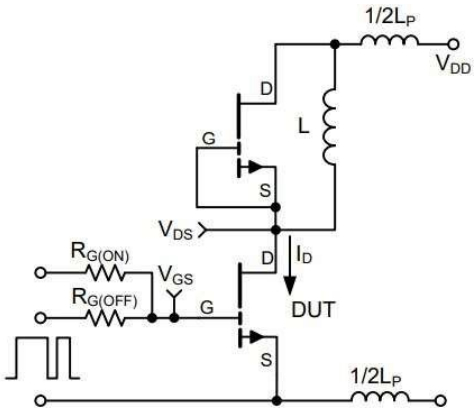


Figure 20: TDG100E90BSP Switching Loss Test Circuit

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate. However, it increases the reverse conduction loss. Negative gate bias operation helps to reduce dynamic rDSON increases due to trapped charges. Operating at a zero gate bias can result in up to 30% shift in dynamic rDSON. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at www.gansystems.com.

Similar to a silicon MOSFET, the external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing

The TDG100E90BSP has a dedicated source sense pin. The GaN*PX*® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved connecting the gate drive signal from the driver to the gate pad on the TDG100E90BSP and returning from the source sense pad on the TDG100E90BSP to the driver ground reference.

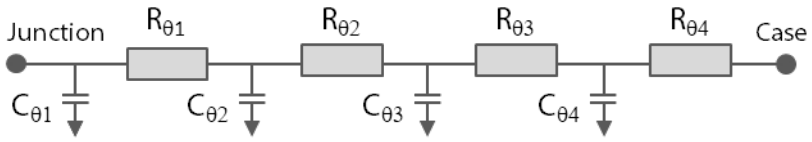
Thermal

The substrate is internally connected to the thermal pad on the bottom-side of the TDG100E90BSP. The source pad must be electrically connected to the thermal pad for optimal performance. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

The RC elements are assigned to the internal layers of the TDG100E90BSP as follows



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.024	$C_{\theta 1}$ = 3.92E-05
$R_{\theta 2}$ = 0.372	$C_{\theta 2}$ = 2.73E-03
$R_{\theta 3}$ = 0.128	$C_{\theta 3}$ = 6.14E-04
$R_{\theta 4}$ = 0.026	$C_{\theta 4}$ = 9.30E-04

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaN*PX*® Using RC Thermal SPICE Models” available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not need an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 100 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 130 V for 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the TDG100E90BSP device to be specified to 150 °C (Tj). The device can handle at least 3 reflow cycles.

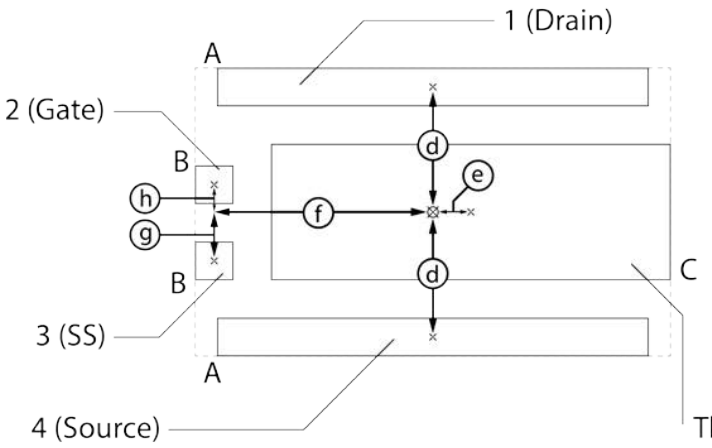
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues. For more details, please refer to the soldering application note "GN011-Soldering-Recommendations- for-GaNPX®-Packaged-Devices" at www.gansystems.com

Recommended PCB Footprint for TDG100E90BSP



NOTE: Thermal pad must be connected to Source (pad 4) for best performance

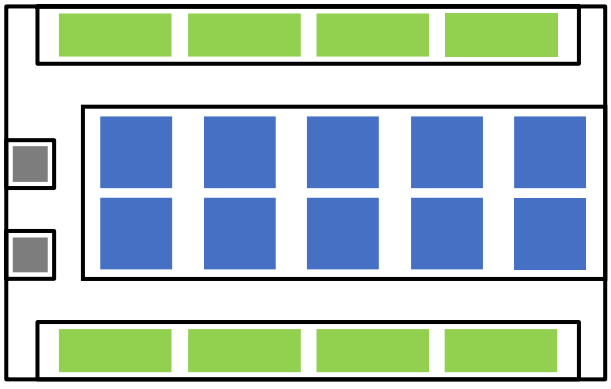
Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	6.80	0.60	0.268	0.024
B	0.60	0.60	0.024	0.024
C	6.30	2.14	0.248	0.084

Dimensions

	mm	Inches
d	1.97	0.078
e	0.60	0.024
f	3.45	0.136
g	0.77	0.030
h	0.43	0.017

Recommended Solder Stencil for TDG100E90BSP PCB Footprint

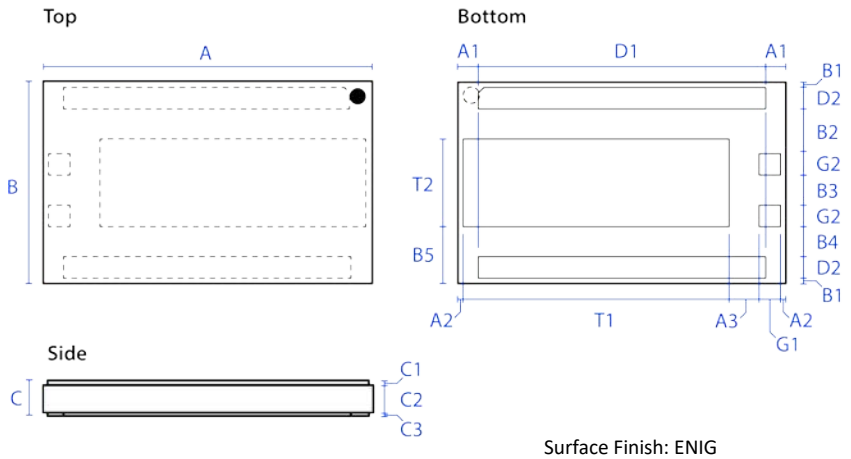


Dimension of stencil aperture

0.5 x 0.5 mm
1.43 x 0.5 mm
0.97 x 0.97 mm

- Thickness of stencil: 100 µm
- Solder paste coverage: 70%

Package Dimensions

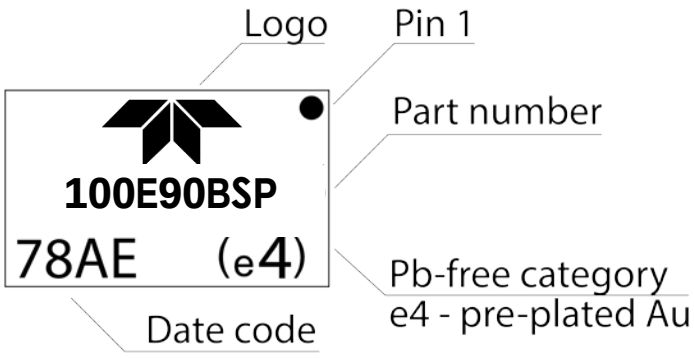


Note: Inch measurements are approximate values

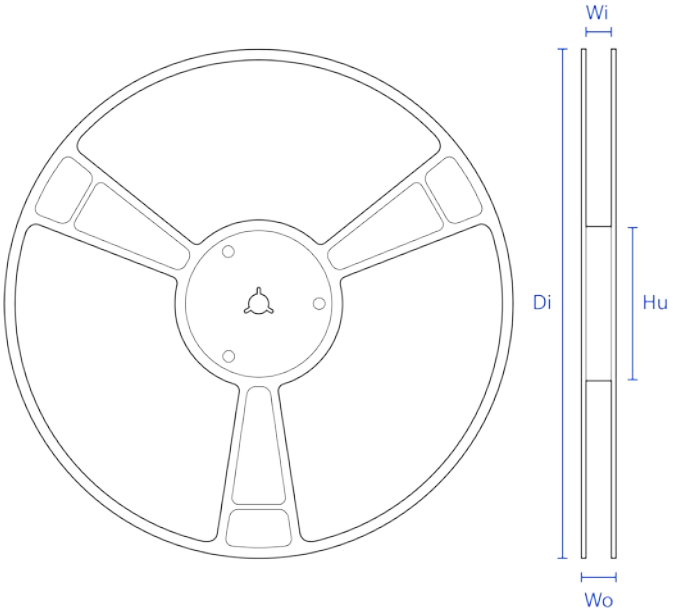
Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

	mm	Inches	
A	7.55	0.297	± 0.10 mm (0.004″)
A1	0.425	0.017	± 0.05 mm (0.002″)
A2	0.075	0.003	± 0.05 mm (0.002″)
A3	0.70	0.028	
B	4.59	0.181	± 0.10 mm (0.004″)
B1	0.075	0.003	± 0.05 mm (0.002″)
B2	1.04	0.041	
B3	0.70	0.028	
B4	0.70	0.028	
B5	1.275	0.050	± 0.05 mm (0.002″)
C	0.51	0.0201	± 0.05 mm (0.002″)
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	6.70	0.264	
D2	0.50	0.020	
G1	0.50	0.020	
G2	0.50	0.020	
T1	6.20	0.244	
T2	2.04	0.080	

GaN*PX*® Part Marking

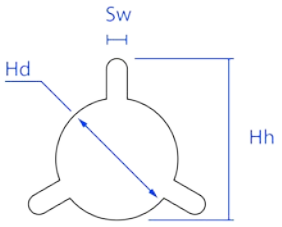


TDG100E90BSP GaN*PX*® Tape and Reel Information

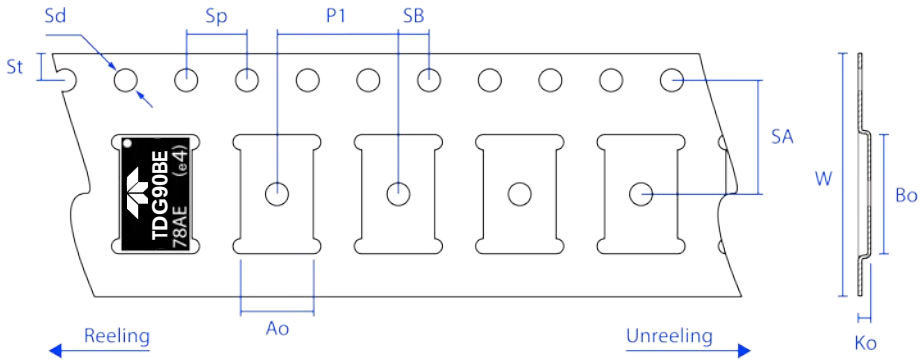


Dimensions (mm)

	13" reel (330 mm)		7" mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	180.0	+1.5 / - 2.0
Wo	22.4	MAX	22.4	MAX
Wi	16.4	+ 2.0 / - 0.0	16.4	+ 2.0 / - 0.1
Hu	100.0	+/- 1.5	60.0	+ 2.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.8
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.1	+/- 0.3



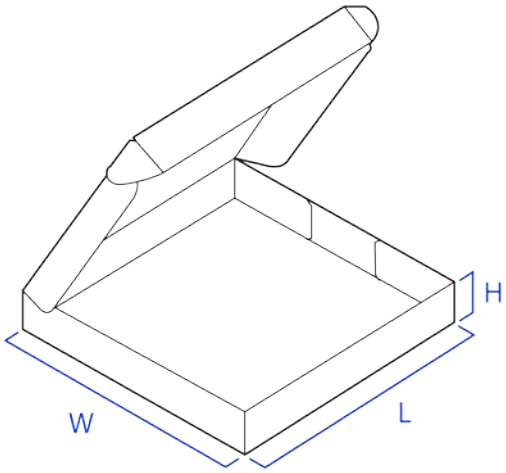
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	8.00	+/- 0.1
W	16.00	+ 0.3 / - 0.1
Ko	1.20	+/- 0.1
Ao	4.80	+/- 0.1
Bo	7.85	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	7.50	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



Outside dimensions (mm)

	7" mini-reel	13" tape-reel
W	197	342
L	204	355
H	32	53

Ordering Information

Ordering Code	Package Type/Part Marking	Packing Method	Qty	Reel Diameter	Reel Width	Origin	ECCN
TDG100E90BSP	GaN*PX*® bottom cooled / TDG90BE	Mini-Reel	250	7" (180 mm)	16mm	US	EAR99
TDG100E90BSPF	GaN*PX*® bottom cooled / TDG90BF	Mini-Reel	250	7" (180 mm)	16mm	EU	EU

Document Definitions and Categories

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